Fpga implementation of Design and verification Synchronous serial port(S-PORT)

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Abstract*: Synchronous serial ports, or S-Ports, support a variety of serial data communication protocols.They provide a direct interconnection between processors in a multiprocessor system.Bidirectional functions provide flexibility for serial Communication.Serial Communication Ports can operate at half the full clock rate at the processor,at a maximum data rate of n/2 Mbps,where n-equals the processor core clock frequency. The most common use of S-PORT is to interconnect two processors in a multiprocessor system.These interface devices can be operated in the synchronous mode. S-PORT can transfer a frame of data with three or thirty two bits per transmission. For serial communications there are different types of cables used such as UARTS, RS232 cable, I2C bus but the time required to transmit and receive through these cables takes a lot of time like 11kbps but these days the the speed is the most important in every aspect. So this project is based on the device or cables that can be used to increase the speed for the serial communication between two devices. So to overcome the problem of less speed, the SPORT is used which has a very high speed of 100mbps. The RTL code is written for each and every block using Verilog.The code thus written is simulated using XILINX ISE 12.4 tool.The verification for the SPORT core is done by developing verification IP in System Verilog. The main application is in the present day Avionics application systems in Defence, Multiprocessor communication, ADC & DAC, Video codec applications.

Key words: S-PORT,

I. INTRODUCTION

Serial data transmission is widely used in communications over long distances. Parallel communication requires many wires to be laid between the two communicating points.

Hence, usually data is converted to serial format and sent over fewer numbers of wires to the destination. To interface a microcomputer with serial data lines, the data must be converted to and from serial form. A parallel-in-serial-out shift register and a serial-in-parallel-out shift register can be used to do this. Also needed of some cases of serial data transfer data is hand-shaking circuitry to make sure that a transmitter does not send data faster than it can be read in by the receiving system. A device which can be programmed to do synchronous communication is often called as synchronous serial peripheral port or S-PORT. For serial communications there are different types of cables used such as UARTS, RS232 cable,I2C bus but the time required to transmit and receive through these cables takes a lot of time like 11kbps but these days the speed is the most important in every aspect. So this paper is based on the device or cables that can be used to increase the speed for the serial communication between two devices. So to overcome the problem of less speed, the S-PORT is used which has a very high speed of 100mbps. Many microprocessor devices have a built in S-PORT and it is one of the commonly used serial interface peripherals. As a peripheral device of a microcomputer system, the S-PORT receives parallel data from the C.P.U and performs parallel to serial conversion at the transmitter end and serial to parallel conversion at the receiver end. The most common use of S-PORT is to interconnect two processors in a multiprocessor system. Serial Communication Ports can operate at half the full clock rate at the processor, at a maximum data rate of n/2 Mbps, where n-equals the processor core clock frequency's-PORT can transfer a frame of data with three or thirty two bits per transmission.

Each SPORT has a five-pin interface:

Table 1 Sport external interface

SCLK	Serial clock
RFS	Receive frame synchronization
TFS	Transmit frame synchronization
DR	Serial data receive
DT	Serial data transmit

The figure.1.shows a simplified block diagram of a S-PORT.A S-PORT receives serial data on its DR input and transmits serial data on its DT output. It can receive and transmit simultaneously,for full duplex operation.The data bits are synchronous to the serial clock SCLK,which is an output if the processor generates this clock or an input if the clock is generated synchronization signals RFS and TFS are used to indicate the start of a serial data word or stream of serial words.Data to be transmitted is written from an internal processor register to TX FIFO via processor bus interface.This data is then transferred to the transmit shift register. The bits in the shift register are shifted out on the S-PORT's DT pin, MSB first, synchronous to the serial clock.The receive portion of the S-PORT externally. Frame accepts data from the DR pin, synchronous to the serial clock.When an entire word is received, the data is written to RX FIFO, where it is available to the processor.

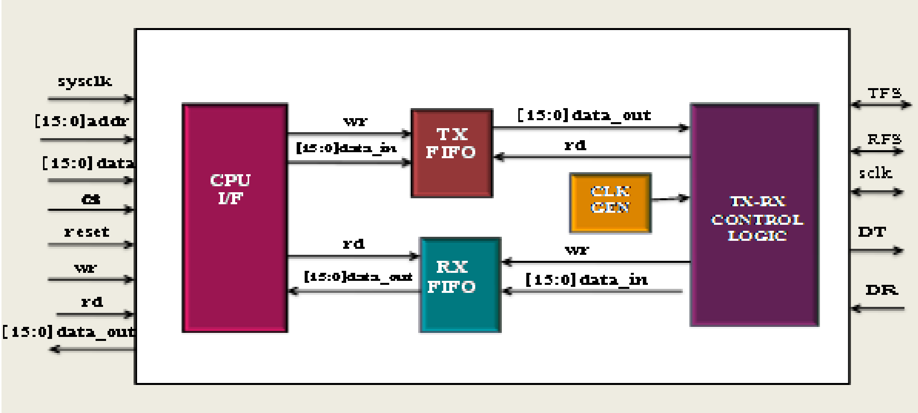


Figure 1 Block diagram of s-port

II. WORKING OF S-PORT

A. Operation

Writing to a SPORT's TX register readies the SPORT for transmission; the TFS signal initiates the transmission of serial data. Once transmission has begun, each value written to the TX register is transferred to the internal transmit shift register and subsequently the bits are sent, MSB first. Each bit is shifted out on the rising edge of SCLK. After the first bit (MSB) of a word has been transferred, the SPORT generates the transmit interrupt. The TX register is now available for the next data word, even though the transmission of the first word is ongoing.Enabling the SPORT Tx and writing to the TX FIFO, readies the SPORT for transmission.The TFS signal initiates the transmission of serial data.Once transmission has begun, each value written to the TX register is transferred to the internal transmit shift register and subsequently the bits are sent, MSB first. Each bit is shifted out on the rising edge of SCLK. In the receiving section, bits accumulate as they are received in an internal receive register.When a complete word has been received, it is written to the RX FIFO and the receive interrupt for that SPORT is generated.

B. Need and Significance of Serial Data Transmission

Serial data transmission (SDT) is the simplest, most economical and easiest method used for transferring digital information from one point to another. Extremely high data rates are possible. The reductions in costs and installation effort as well as user-friendliness favor serial data transmission. Serial transmission technology is increasingly used for the transmission of digital data. A large number of up-to-date communications networks apply serial transmission.Significance of SDT has grown with its application in internet.

The numerous applications include computer networks for office communications, field bus systems in process, building and manufacturing automation, Internet and, finally, ISDN.Hence SDT is very essential for efficient lossless communication.

Features of S-Port

Serial ports offer the following features and capabilities:

A. Bidirectional
B. Double-buffered:
C. Clocking
D. Word length
E. Framing

A. Bidirectional

Each SPORT has independent transmit and receive sections. Two bi-directional channels per serial port, configurable as either transmitters or receivers. Each serial port can be configured as two receivers or two transmitters, permitting two unidirectional streams into or out of the same serial port. This bi-directional functionality provides greater flexibility for serial communications. Two SPORTs can be combined to allow full-duplex, dual-stream communications.

B. Double-Buffered

Double-buffers data all serial data pins have programmable receive and transmit functions and thus have one transmit and one receive data buffer register and a bi-directional shift register associated with each serial data in. Double-buffering provides additional time to service the SPORT. Each SPORT section (both receive and transmit) has a data register for transferring data words to and from other parts of the processor and a register for shifting data in or out. The double-buffering provides additional time to service the SPORT.

C. Clocking

Provides internally-generated serial clock and frame sync signals in a wide range of frequencies, or accepts clock and frame sync input from an external source. Each SPORT can use an external serial clock or generate its own in a wide range of frequencies down to 0 Hz.

Sclk _frequency = sysclk / 2 x (sclkdiv + 1)

Sport Clk (Sclk)

SPORT operates on its own serial clock signal. The serial clock (SCLK) can be internally generated or received from an external source. The ISCLK bit, bit 3 in **sport_cntrl_reg1** register, determines the SCLK source for the SPORT. If this bit is a 0, the processor generates the SCLK signal; if it is a 1, the processor expects to receive an external clock signal on SCLK. At reset, ISCLK is cleared, sport generates SCLK internally. When ISCLK is reset, internal generation of the SCLK signal begins on the rising edge of **sysclk,** whether or not the corresponding SPORT is enabled. External serial clock frequencies may be as high as the processor’s cycle rate, up to a maximum of 13.824 MHz; internal clock frequencies may be as high as one-half the processor’s clock rate. The frequency of an internally generated clock is a function of the processor clock frequency and the value of the 16-bit serial clock divide modulus register.

Table 2 shows how some common SCLK frequencies correspond to values of SCLKDIV.

SCLKDIV	*SCLK Frequency*
20479	300 Hz
5119	1200 Hz
639	9600 Hz
95	64 kHz
3	1.536 MHz
2	2.048 MHz
0	6.144 MHz
(Assumes sysclk frequency of 12.288 MHz)	

If the value of SCLKDIV is changed while the internal serial clock is enabled, the change in SCLK frequency takes effect at the start of the next rising edge of SCLK.

D. Word Length

Each SPORT supports serial data word lengths from three to sixteen bits.128-channels TDM is supported in multichannel mode operation. Each SPORT independently handles words of 3 to 16 bits. The data is right-justified in the SPORT data registers if it is fewer than 16 bits long. The serial word length (SLEN) field in each SPORT Control register determines the word length according to this formula:

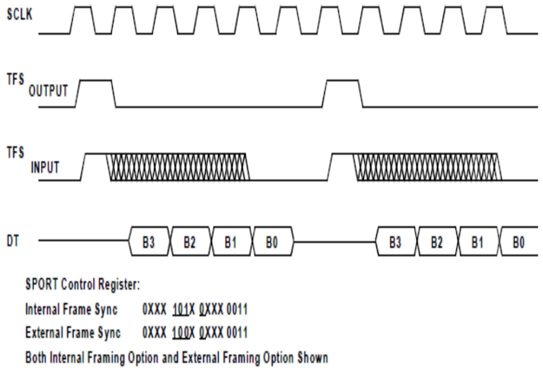
$$\text{Serial Word Length} - \text{SLEN} + 1$$

E. Framing

The SPORT outputs an internally generated transmit framing signal after data is loaded into the transmit (TX0 or TX1) register, at the time needed to ensure continuous data transmission, after the last bit of the current word is transmitted (the exact time depends on the framing mode being used; The occurrence of the transmit frame sync is a result of the availability of data in the transmit register. With an internally generated receive framing signal, the processor controls the timing of the receive data. The external data source must provide data to the serial port synchronized to the receive framing signal (the timing depends on the framing mode being used. The processor generates RFS periodically on a multiple of SCLK cycles, based on the value of the 16-bit receive frame sync divide modulus register.

Normal Framing

In the normal framing mode, the framing signal is checked at the falling edge of SCLK.If the framing signal is asserted, received data is latched on the next falling edge of SCLK and transmitted data is driven on the next rising edge of SCLK.The framing signal is not checked again until the word has been transmitted or received. If data transmission or reception is continuous ,i.e., the last bit of one word is followed without a break by the first bit of the next word, then the framing signal should occur in the same SCLK cycle as the last bit of each word.



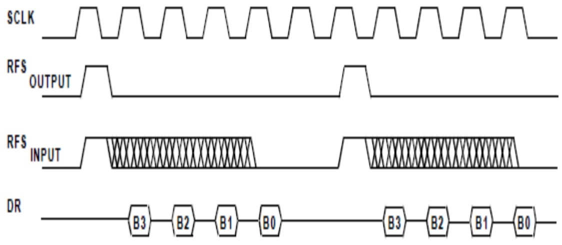
SPORT Control Register:

Internal Frame Sync 0XXX 101X 0XXX 0011

External Frame Sync 0XXX 100X 0XXX 0011

Both Internal Framing Option and External Framing Option Shown

Figure 2 SPORT Transmit, Normal Framing



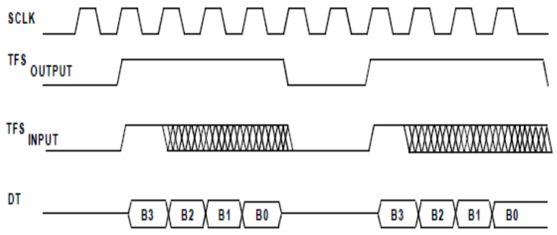
SPORT Control Register:
Internal Frame Sync 0X10 XXX1 X0XX 0011
External Frame Sync 0X10 XXX0 X0XX 0011
Both Internal Framing Option and External Framing Option Shown

Figure 3SPORT Receive, Normal Framing

Alternate Framing

In the alternate framing mode, the framing signal should be asserted in the same SCLK cycle as the first bit of a word. Received data bits are latched on the falling edge of SCLK and transmitted bits are driven on the rising edge of SCLK, but the framing signal is checked only on the first bit. Internally generated frame sync signals remain asserted for the length of the serial word. Externally generated frame sync signals are only checked during the first bit time.

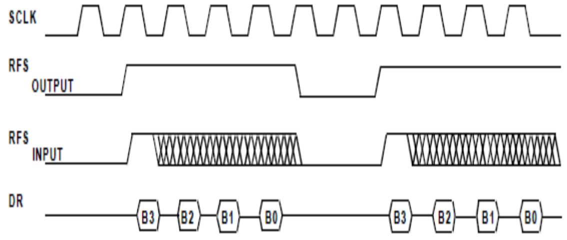
Framing modes for receiving and transmitting data are independent. If the receive frame sync width (RFSW) bit or transmit frame sync width (TFSW) bit in the SPORT Control register is a 0, normal framing is enabled. If the RFSW or TFSW bit is a 1, alternate framing is used. The RFSW bit is bit 12 in the SPORT Control register (0x3FF6 for SPORT0 and 0x3FF2 for SPORT1), and the TFSW bit is bit 10. These bits are both cleared at reset, so that normal framing in both directions is enabled.



SPORT Control Register:
Internal Frame Sync 0XXX 111X 0XXX 0011
External Frame Sync 0XXX 110X 0XXX 0011
Both Internal Framing Option and External Framing Option Shown

Note: There is an asynchronous delay between TFS input and DT. See the appropriate data sheet for specifications.

Figure 4 SPORT Transmit, Alternate Framing



SPORT Control Register:
Internal Frame Sync 0X11 XXX1 X0XX 0011
External Frame Sync 0X11 XXX0 X0XX 0011
Both Internal Framing Option and External Framing Option Shown

Figure 5 SPORT Receive, Alternate Framing

III. C.P.U INTERFACE SIGNALS

The C.P.U signals are given as input signals to the S-PORT. The S-PORT operation is mainly dependent on C.P.U.The following table shows the input signals which are connected to the S-PORT.

S-PORT input signals

S.No	Signal name	Input/ output	Description
1.	Reset	Input	Active high system reset
2.	Sysclk	Input	Input system clock
3.	cpu_addr	Input	16 bit input address from processor interface
4.	cpu_data_in	Input	16 bit input data from processor interface
5.	cpu_cs	Input	Active high chip select
6.	cpu_rd	Input	Active high read signal
7.	cpu_wr	Input	Active high write signal
8.	cpu_data_out	Output	16 bit data output to processor interface
9.	Rfs	Inout	Receive frame sync signal
10.	Tfs	Inout	Transmit frame sync signal
11.	rx_in	input	Serial data line input
12.	Sclk	Inout	Synchronous serial clock
13.	tx_out	Output	Serial data output

Each module is developed as individual verilog code files for respective functionalities is tested independently using a testbench.the functionality of test bench is to generate the various test vectors and stimulates the input of the modules**.**

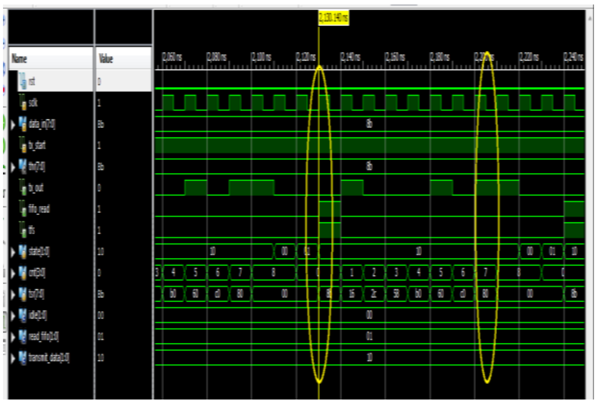


Figure 6 Simulati on Waveform o Transmitter

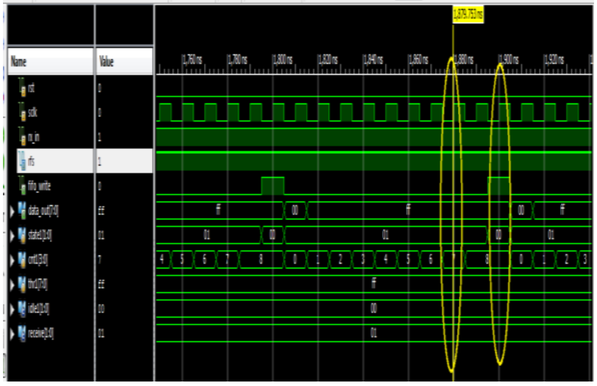


Figure 7 Simulation Waveform of Receiver

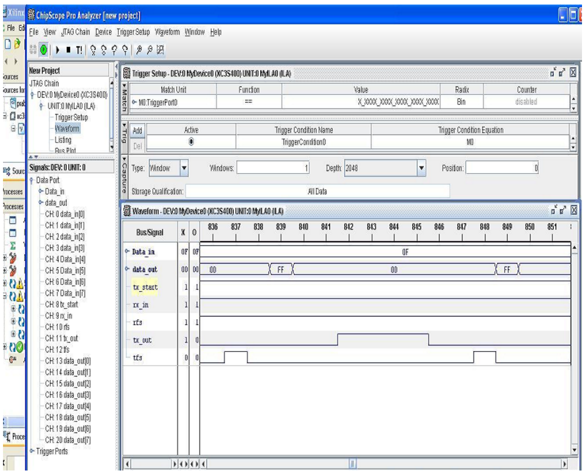


Figure 8 chip scope waveform

CONCLUSIONS

In this technical era,high speed data transfer over short distances plays a vital role.In order to couple speed with accuracy and economy, we opt for serial data communication.To interface a microcomputer with serial data lines, the data must be converted to and from serial format. Hence devices called Serial communication interface are used which can perform this function. These interface devices can be operated in the synchronous mode.In the communication system,there are many devices which operate at different speeds.In order to facilitate the data exchange between these devices there is a need for an effective interface. S-PORT is one such serial communication interface device in the synchronous mode that helps in achieving error free data transmission.It operates at double the speed of SPI.

Keeping in view these advantages, in this paper, the S-PORT has been designed using Verilog and implemented on FPGA Spatran 3 kit.

FUTURE SCOPE

In this paper, the S-PORT has been implemented in synchronous mode only. Even the design can be made more flexible by providing the programmable mode and command word registers that suit the requirements as per the application. The synchronous serial ports are mainly used in multiprocessor communication where the data transmission can takes place at a high speed within the system(i.e., for short distances).The code developed is even synthesizable and can be implemented on any of the programmable devices like FPGA or ASICs.

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