Design and Verification of Network Router

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***Abstract*— The focus of this Paper is the actual implementation of Network Router and verifies the functionality of the five port router for network on chip using the latest verification methodologies, Hardware Verification Languages and EDA tools and qualifies the Design for Synthesis and implementation. This Router design contains Four output ports and one input port, it is packet based Protocol. This Design consists of Registers, FSM and FIFO's,for Verification Systemverilog language used with different testcases,for 100% functional coverage constraint random test case used.**

***Index Terms*— FIFO, FSM, Network-On-Chip, Register blocks,Router Simulation,verification plan.**

I. INTRODUCTION

90% of ASIC respins are due to functional bugs. As the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the verification or simulation. In order to avoid the delay and meet the TTM, we use the latest verification methodologies and technologies and accelerate the verification process. This project helps one to understand the complete functional verification process of complex ASICs an SoC's and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

II. Why Would I Need a Router?

For most home users, they may want to set-up a LAN (local Area Network) or WLAN (wireless LAN) and connect all computers to the Internet without having to pay a full broadband subscription service to their ISP for each computer on the network. In many instances, an ISP will allow you to use a router and connect multiple computers to a single Internet connection and pay a nominal fee for each additional computer sharing the connection. This is when home users will want to look at smaller routers, often called broadband routers that enable two or more computers to share an Internet connection. Within a business or organization, you may need to connect multiple computers to the Internet, but also want to connect multiple private networks not all routers are created equal since their job will differ slightly from network to network. Additionally, you may look at a piece of hardware and not even realize it is a router.What defines a router is not its shape, color, size or manufacturer, but its job function of routing data packets between computers. A cable modem, which routes data between your PC and your ISP can be considered as a router. In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing). In this scenario, the computer that is connected to the Internet is acting as the router for the second computer to obtain its Internet connection. Going a step up from ICS, we have a category of hardware routers that are used to perform the same basic task as ICS, albeit with more features and functions often called broadband or Internet connection sharing routers, these routers allow you to share one Internet connection with multiple computers. Broadband or ICS routers will look a bit different depending on the manufacturer or brand, but wired routers are generally a small box-shaped hardware device with ports on the front or back into which you will plug each computer along with a port to plug in your broadband modem. These connection ports allow the router to do its job of routing the data packets between each of the computers and the data going to and from the Internet. These routers also support NAT (network address translation), which allows all of your computers to share a single IP address on the Internet.

III. ROUTER DESIGN PRINCIPLES

Given the strict contest deadline and the short implementation window we adopted a set of design principles to spend the available time as efficiently as possible. This document provides specifications for the Router is a packet based protocol. Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet. The router is a" Network Router" has a one input port from which the packet enters. It has four output ports where the packet is driven out. Packet contains 3 parts. They are Header, data and frame check sequence. Packet width is 8 bits and the length of the packet can be between 1 byte to 63 bytes. Packet header contains three fields DA and length. Destination address (DA) of the packet is of 8 bits. The switch drives the packet to respective ports based on this destination address of the packets. Each output port has 8- bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits and from 0 to 63. Length is measured in terms of bytes. Data should be in terms of bytes and can take anything. Frame check sequence contains the security check of the packet. It is calculated over the header and data. The communication on network on chip is carried out by means of router, so for implementing better NOC, the router should be efficiently design. This router supports four parallel connections at the same time. It uses store and forward type of flow control and FSM Controller deterministic routing which improves the performance of router. The switching mechanism used here is packet switching which is generally used on network on chip. In packet switching the data the data transfers in the form of packets between co-operating routers and Independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels. The arbiter is of rotating priority scheme so

that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides.

Features

- Full duplex synchronous serial data transfer.
- Variable length of transfer word up to 64 bytes.
- HEADER is the first data transfer.
- Rx and Tx on both rising or falling.
- Fully static synchronous design with one clock domain.
- Technology independent VERILOG .
- Fully synthesizable.

ROUTER is a Synchronous protocol. The clock signal is provided by the master to provide synchronization. The clock signal controls when data can change and when it is valid for reading. Since ROUTER is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocols do not use a clock pulse, but the data must be timed very accurately.

IV. OPERATION

The Five Port Router Design is done by using of the three blocks. The blocks are 8-Bit Register, Router Controller and output block. The router controller is design by using FSM design and the output block consists of four FIFO's combined together. The FIFO's store data packets and when you want to send data that time the data will read from the FIFO's. In this router design has four outputs i.e. 8-Bit size and one 8-bit data port. It is used to drive the data into router. we are using the global clock, reset signals, error signal and suspended data signals are the output's of the router. The FSM controller gives the error and SUSPENDED_DATA_IN signals. These functions are discussed clearly in below FSM description. The ROUTER can operate with a single master device and with one or more slave devices. If a single slave device is used, the RE (read enable) pin may be fixed to logic low if the slave permits it. Some slaves require the falling edge (HIGH→LOW transition) of the slave select to initiate an action such as the mobile operators, which starts conversion on said transition. With multiple slave devices, an independent RE signal is required from the master for each slave device.

a) figures

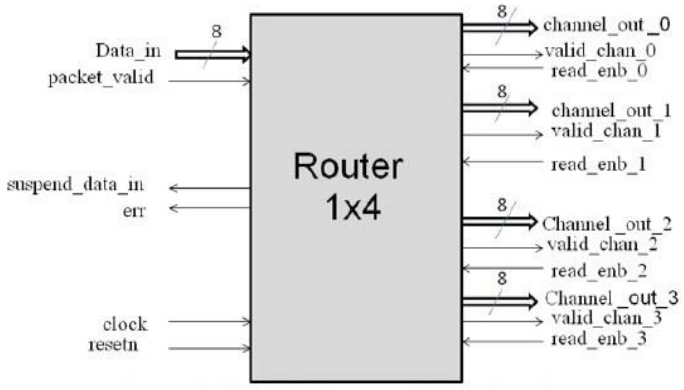


Figure 1: Block Diagram of Five Port Router

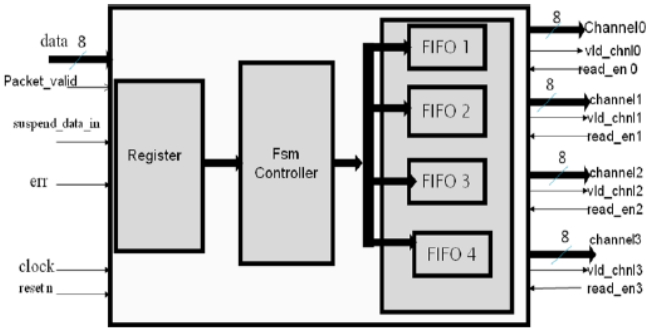


Figure 2: Internal Structure of Five Port Router

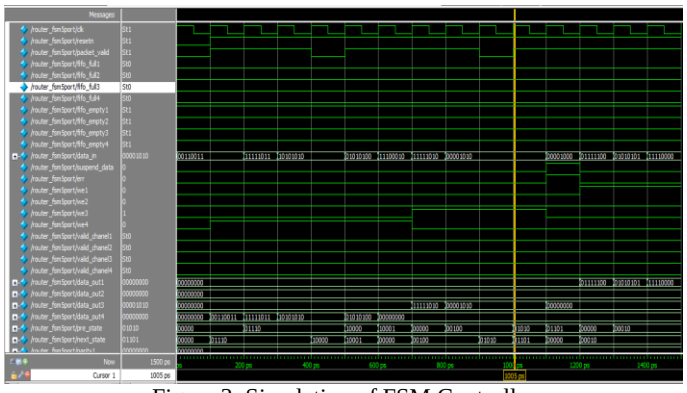


Figure 3: Simulation of FSM Controller

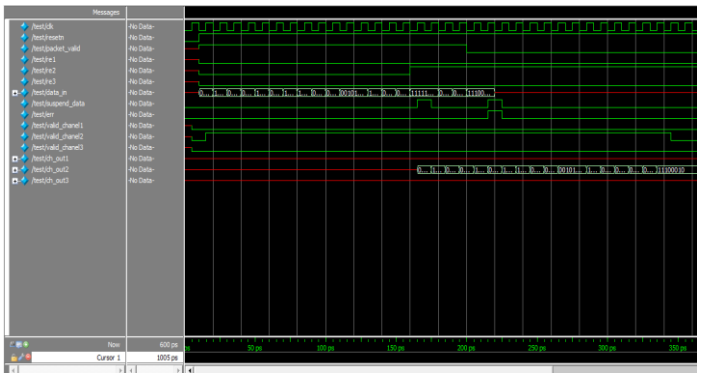


Figure 4: Simulation of Router(Top module)

V. VERIFICATION PLAN

The Verification Plan is the focal point for defining exactly what needs to be tested and it is used to determine the progress and completion of the verification phase of verification.It will functionally verify the design with all possible corner cases.In the plan err signal for parity mismatch and suspend_data are the inputs for the driver.QUEUE[$] is chosen as optimistic to generate random data based on the length in header.Valid_channel 1,2 & 3 are used for the inter-process communication.Read_enable 1,2 & 3 are outputs for the receiver block.Read_enable signals are made high based on the valid_channel's respectively.As per the verification plan Interface, package, top module, test and environment files are written.In the generator all rand variables in transaction are randomized in this block.In transaction as per the spec, an 8-bit value is assigned as header,it is a rand bit which will generate randomized value. It is further part sliced to derive the address of the channel and length of the packet.A mailbox from generator to driver is created.In driver Data received from the generator is driven to the DUT(Design Under Test).

When packet_valid is high, header and the payload are driven.Packet_valid is made low before driving the last byte i.e. parity byte in.Calculated parity in the transaction is further driven as input data to DUT based on the select signal.If sel signal is low, corrupted parity is sent to DUT, to check err signal.Furthermore, suspend_data and error signals are checked in the driver.Finally, the data to duv is sent to scoreboard with an id for further use.In receiver all outputs of the DUT are inputs for the receiver block Valid channel's are used to notify the receiver to start.Read_enable signal is made high based on the respective valid_channel. Data received is sent to scoreboard in a mailbox with an acknowledgement of id, for further use.In scoreboard the data from driver and receiver are compared in the scoreboard.Firstly, checks for the id match.Else, checks for the data mismatch, in the way it was sent & received from the DUV.Generates report based on the comparison of data packets.Stops the environment, when transaction is done by triggering the event.

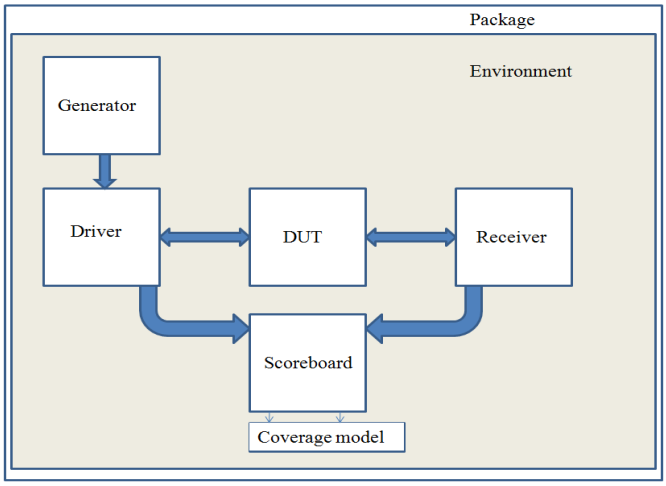
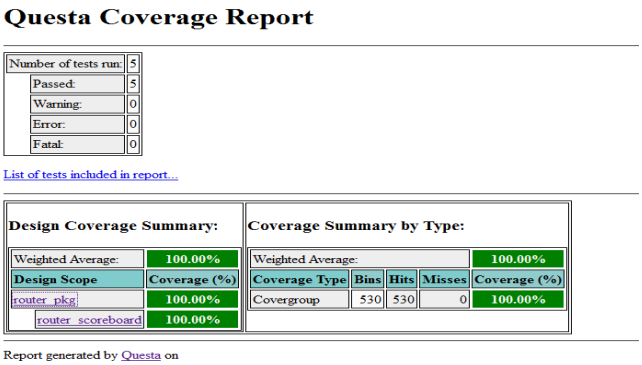


Figure5: Verification Plan



Questa Coverage Report

Number of tests run:	5
Passed:	5
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

Design Coverage Summary:

Weighted Average:	100.00%
Design Scope	**Coverage (%)**
router_pkg	100.00%
router_scoreboard	100.00%

Coverage Summary by Type:

Weighted Average:				100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Coverage (%)**
Covergroup	530	530	0	100.00%

Report generated by Questa on

Figure6:Coverage report

VI. APPLICATIONS

When multiple routers are used in interconnected networks, the routers exchange information about destination addresses, using a dynamic routing protocol. Each router builds up a table listing the preferred routes between any two systems on the interconnected networks. A router has interfaces for different physical types of network connections, (such as copper cables, fiber optic, or wireless transmission). It also contains firmware for different networking protocol standards. Each network interface uses this specialized computer software to enable data packets to be forwarded from one protocol transmission system to another. Routers may also be used to connect two or more logical groups of computer devices known as subnets, each with a different sub-network address. The subnet addresses recorded in the router do not necessarily to map directly to the physical interface connections

VII. EDA TOOLS AND METHODOLOGIES

HVL: System VERILOG.
HDL:VERILOG
Verification Methodology: Constrained Random Coverage Driven verification.
EDA Tools: Questa - A verification Platform from Mentor Graphics.

VIII. CONCLUSION

I have designed network ROUTER and I have verified the functionality of the ROUTER with the latest Verification methodology i.e. System VERILOG and observed the code coverage and functional coverage of ROUTER by using cover points and different test cases (like constrained, weighted and directed test cases). By using these test cases I had improved the functional coverage of the ROUTER. In this project I used one master and four slaves to monitor the ROUTER. Thus the functional coverage of the ROUTER was improved.

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