A Wide Tuning Range Gm-C Continuous-Time Analog Filter

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***Abstract*—A Wide Tuning Range Gm-C Continuous-Time Analog Filter is a CMOS operation nal transconductance amplifier for low-power and wide tuning range filter application is proposed. The transconductor can work from the weak inversion region to the strong inversion region to maximize the transconductance tuning range. The trasconductance can be tuned by changing its bias current. A fifth-order Elliptic low-pass filter implemented with the transconductors is proposed to be implemented in SPICE using CMOS. The filter can operate with the cutoff frequency of 250Hz to 1MHz. The wide tuning range filter would be suitable for multi-mode applications, especially under the consideration of saving chip areas. The third-order inter-modulation of -40dB was measured over the tuning range with two tone input signals. The power consumption is 0.8mW at 1MHz cutoff frequency and 1.8-V supply. Cost and power consumption are two most important factors for these products. For the power consumption, digital circuits can benefit from the supply voltage reduction, but analog circuits can not necessarily decrease the power consumption with the decrease of supply voltage. To meet different specifications for low power consumption, new basic analog building blocks should be re-designed. Many of the previously published papers made efforts on improving the speed, linearity, or dynamic range of transconductor circuits.**

***Key words*—Analog CMOS design, OTA, Gm-C Filter, Weak-inversion region, Strong inversion region.**

I. INTRODUCTION

The Filter is a critical and essential component in modern wireless communication systems. Analog CMOS Filters are demanded for these reasons: (1) low power consumption, (2) low noise, and (3) wide tuning range, in the multi-standard communication systems. The Filters typically result in low noise along with a relatively large tuning range. The large tuning range of the Filter results in the requirement for Filters with different bandwidths to cover a system. And small layout area is need. The current trend of the portable solutions tends to include multiple applications in a long-stand by system. Cost and power consumption are two most important factors for these products. Cost efficiency has been greatly increased with the emergence of CMOS technology in high performance VLSI implementations. Moreover, to save the silicon area in a multimedia system-on-chip solution, re-usable circuits can benefit from the supply voltage reduction, but analog circuits can not necessarily decrease the power consumption with the decrease of supply voltage. To meet different specifications for low power consumption, new basic analog building blocks should be re-designed.

II. CIRCUIT DESIGN

In the analog signal processing, the low-pass filter would be one of the most important circuits in the transciever architecture. There are different ways to implement low-pass filters by CMOS technology at the circuit level. The switched-capacitor (SC) technique which uses switches, capacitors, and operational amplifiers exhibits good linearity, but with the problems of larger power consumption. The active-RC techniques which uses operational amplifiers, resistors, and capacitors to implement integrators. The absence of the local feedback in the Gm-C analog filter technique performs good frequency responses of the signal transfer functions. Furthermore, Gm-C analog filters do not require extra processing steps, as compared with active-RC filters, and their frequency tuning is easily achieved using DC bias voltage or current. The performance of the transconductor will largely affect the Gm-C analog filters. Many of the previously published papers made efforts on improving the speed, linearity, or dynamic range of transconductor circuits.

III. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The Constant Drain-Source Transconductor

In many applications, the MOSFET under the linear region is used to replace the passive resistor. The classical NMOS model equation under the linear region is

$$I_D = \mu_n C_{ox}(W/L)[(V_{GS} - V_{tn}) - aV_{DS}^2/2] \quad (1)$$

Where a is the process dependent parameter. The linear region is hold as the drain-source voltage is lower than the gate-source voltage. If the equation is exact, the perfect linear circuit can be obtained. However, this equation neglects higher order terms under the short channel process, and some of nonlinear terms would occur and then reduce the circuit performance. If a small drain-source voltage is used, we can simply neglect the second order terms in above equation. The drain current is linear with respect to the applied drain-source voltage. Thus we can obtain a small-signal resistance of $r_{DS}=1/\mu_n C_{ox}(W/L)(V_{GS} - V_{tn})$ (2). As the linear region resistor is introduced, the resistance would be proportional to the gate bias voltage and we add the **transconductance**

continuous tuning ability. If the drain-source voltage is kept constant, the drain current is linear with respect to the applied gate-source voltage. Fig2.3 shows the transconductor which uses a constant drain-source technology. By using regulated control loop, the drain voltage is set to the voltage Vtune through the feedback topology. Then,

$I_1 = \mu_n C_{ox}(W/L)\ [(V_i+ - V_{tn})\ V_{tune} - a\ V_{tune}^2/2]$ (3)

$I_2 = \mu_n C_{ox}(W/L)[(V_i-\ - V_{tn})\ V_{tune} - a\ V_{tune}^2/2]$ (4)

We can have,

$I_1 - I_2 = \mu_n C_{ox}\ (W/L)V_i+ - V_i-)\ V_{tune}$ (5)

$Gm = \mu_n C_{ox}\ (W/L)V_{tune}$ (6)

From the above equation, the transconductance and biasing current are proportional to the Vtune. In practice, the second order effect would limit the accuracy of the model.

Transconductor

A transconductor is nothing but but the **operational transconductance amplifier** (**OTA**). It is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control amplifier's transconductance.

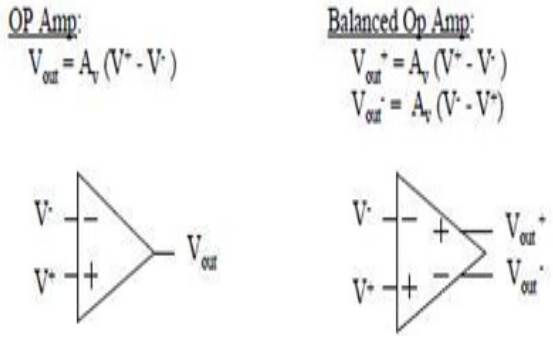

Figure2: A Basic Operational Amplifier

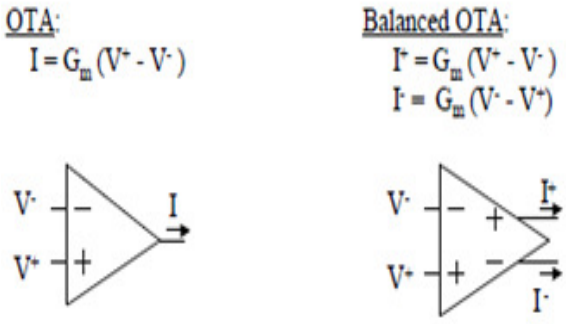

Figure 3: An Operational Transconductance Amplifier

The OTA mainly consists of ,

1) Basic transistor differential amplifer
2) Wide-output-range differential amplifier
3) Build with cascodes or folded cascode or differential approaches.

The OTA also called a Transconductor Cell Or Simply A Transconductor

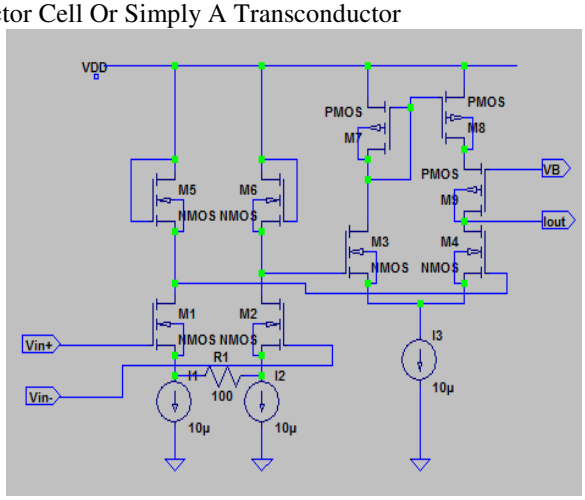

Figure1: The proposed transconductor cell

Gm-C filter

A Simplest Gm-C Filter is a first order Gm-C filter and it acts as an Integrator.

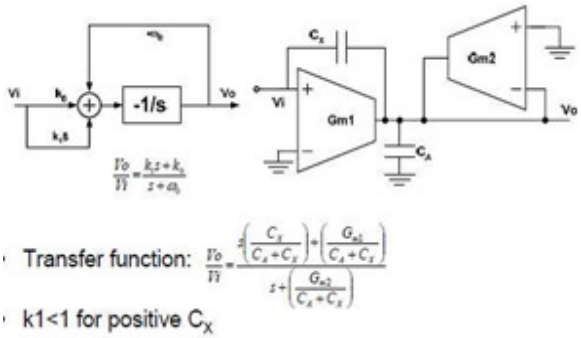

Figure4: A first Order Gm-C Integrator

We can set Gm and build C sufficiently big enough (slow down the amplifier), or set by C (smallest size to get enough SNR), and change Gm. The transconductance can be tuned by changing its bias current.

Continuous time filter

In the analog signal processing, the low-pass filter would be one of the most important circuits in the transceiver architecture. There are different ways to implement low-pass filters by CMOS technology at the circuit level. The switched-capacitor(SC) technique which uses switches, capacitors, and operational amplifiers exhibits good linearity. The active-RC technique which

uses operational amplifiers, resistors, and capacitors also exhibits high linearity. Another technique to realize continuous-time analog filters is to utilize transconductors and capacitors to implement integrators. The absence of the local feedback in the Gm-C analog filter technique performs good frequency responses of the signal transfer functions. Furthermore, Gm-C analog filters do not require extra processing steps, as compared with active- RC filters, and their frequency tuning is easily achieved using DC bias voltage or current. The performance of the transconductor will largely affect the Gm-C analog filters

IV. SIMULATION TOOLS

SPICE TOOL

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general- purpose, open source analog electronic circuit simulator. It is a powerful program that is used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit.

Introduction

Unlike board-level designs composed of discrete parts, it is not practical to breadboard integrated circuits before manufacture. Further, the high costs of photolithographic masks and other manufacturing prerequisites make it essential to design the circuit to be as close to perfect as possible before the integrated circuit is first built. Simulating the circuit with SPICE is the industry-standard way to verify circuit operation at the transistor level before committing to manufacturing an integrated circuit.

Board-level circuit designs can often be breadboarded for testing. Even with a breadboard, some circuit properties may not be accurate compared to the final printed wiring board, such as parasitic resistances and capacitances. These parasitic components can often be estimated more accurately using SPICE simulation.

Circuit Designing using Linear Time SPICE

Circuit Designing is done through selecting the appropriate component and giving proper connectivity. There are signal sources such as voltage, current, grounding the circuit. While run the circuit the displaying of the output is available through probing the circuit.

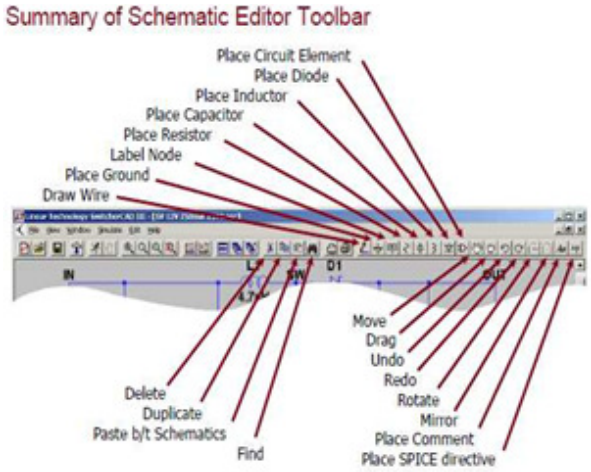

Figure5: Summary Schematic of SPICE Tool

Simulation Commands

To run a simulation, specify the type of analysis to be performed.

There are six different types of analyses:

1) Transient analysis
2) Small signal AC
3) DC sweep
4) Noise
5) DC transfer function
6) DC operating point

CMOS Analog Filter Design and Simulation

The design using double pseudo-differential pairs and the source degeneration structure under nano-scale CMOS technology, the nonlinearity caused by short channel effect from small feature size can be minimized. Then, another transconductor with pseudo-differential structures is proposed. The linearity is improved by mobility compensation techniques as the device size is scaled down to achieve high-speed operation. Short channel effects in the nano-scale technology are discussed and eliminated, and the results show superior performance even at high-speed operation. Finally, a transconductor with the specific target for ADSL2C application is discussed. A precise model is adopted to eliminate short channel effects and high linearity performance can thus be achieved.

The transconductor is one of the most important building blocks in analog and mix-mode circuits, including multipliers, continuous-time Gm-C filters, voltage controlled oscillators and continuous-time sigma-delta modulators. Its main idea is to convert the input voltage into the output current with a linear transformation factor. The active device is used for replacing passive devices owing to power and area consideration with the tradeoff the non-ideal performance. The main non-ideal characteristics of the transconductor are the limited linear input range, limited output impedance, finite signal-to-noise ratio, and finite bandwidth. The linear performance is the most important issue in the transconductor design. Moreover, as the feature size of CMOS technology scales down with supply voltage, the dynamic range, bandwidth, and power consumption will be limited under specific linearity.

This filter uses first, the fundamental of the integrator is discussed. Then, the methods of filter synthesis are introduced. The transconductors and capacitors are assumed ideal under filter synthesis. After discussing the synthesis methods, the non-idealities of the filter are presented. A second-order band-pass filter is used as an example to illustrate the effects of the transconductor non-idealities. It will show that transconductor properties determine the filter performance.

Integrator

To realize an integrator in Gm-C technology, a transconductor and a capacitor can be used as shown in the fig.3.1 We assume that the transconductor and the capacitor, CL, and the output voltage is given by

$$Vo=(Gm/SCL)Vi \qquad (7)$$

The ideal integrator has an infinite DC gain and a phase shift of -90 degree. We can model to have transfer function as $H(w)=(R(w)+jX(w))-1$ (8). The quality factor, which is defined as $Q(w)=X(w)/R(w)$ (9), indicates the integrator phase deviation from -90 degree. If the integrator is ideal, the quality factor would be infinite. In most of the integration circuits, it is required to keep the signals fully differential. The fully differential circuits show good noise and distortion properties as described in previous section. The fully differential integrator can be realized by two structures, as shown figure6.

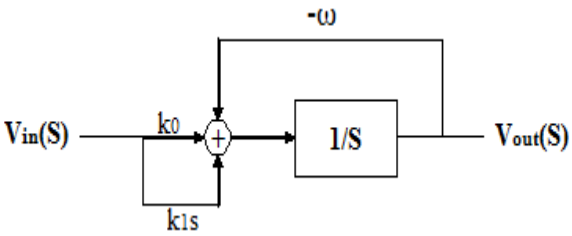

Figure6: first order integrator

Biquad Sections

The biquad synthesis is a method to realize the filter transfer function by cascading multiple first or second order sections. A biquad transfer function can be implemented by a two-integrator loop. The loop is composed by a lossy inverting integrator and a Non-inverting integrator. An integrator is lossy when we connect a resistor in parallel with The loading capacitor. The resistor is lossy when we connect a resistor in parallel with the Loading capacitor. The resistor can be implemented by a transistor within negative feedback. Fig.7 shows the realization of a lossy integrator. The transfer function is given by

$$\frac{Vo}{Vi} = -\frac{gm1}{sCL} + g \qquad (10)$$

A general biquad section has a second order function given by

$$\frac{Vo}{Vi} = K\frac{a\,o + a1s + a2s^2}{s2 + s\omega/Qp + \omega^2} \qquad (11)$$

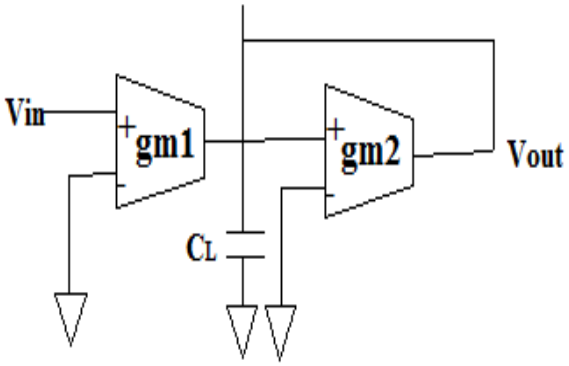

Figure7:integrator

The low-pass, high-pass, band-stop, band-pass, and all-pass functions are dependent on the constants a0, a1, a2. We should note that a0 is equal to ω^2 and thus K is the DC gain of the transfer function. The figure shows a Gm-C implementation of the biquad section.

Filter Archetecture

To demonstrate the basic building block in a system level, a fifth order Elliptic low-pass filter is implemented. The fifth- order Elliptic low-pass filter design starts from a standard fifth-order Elliptic low-pass LC-ladder prototype, as shown in Fig. -6dB DC gain can be easily obtained under very low frequency when resistor Rs equals to resistor R_L. From the RLC-ladder prototype, through the use of the signal-flow graph method, the fifth-order Elliptic low-pass Gm-C filter, which consists of seven identical transconductors and seven capacitors, including two floating capacitors, is obtained. The transconductance, which equals to the value of 1/Rs and 1/RL, is used for all transconductors. Q tuning circuits are not considered here with the intrinsic quality of the low Q structure. The final Gm-C Filter implementation is shown in fig. The transconductor introduced in the previous section is used here in the design of the fifth-order Elliptic low-pass Gm-C filter. In our circuit, when the transconductor works in the weak inversion region, a small value of capacitance will be enough to achieve the low cutoff frequency owing to the small transconductance in the nS order. On the other hand, the larger transconductance can also be obtained in the same filter architecture for higher cutoff frequency when the transconductor works in the saturation region.

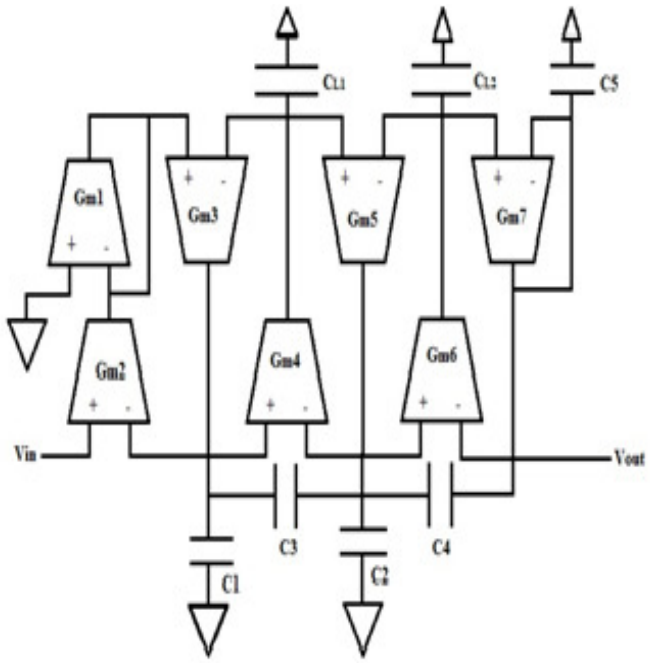

Figure8: Fifth Order LPF architecture

Transconductor Cell Design

The transconductor is designed with a differential input pair operating in the triode region. The drain current of a MOS transistor in the linear region can be expressed as:

$$I_D=K_{lin}[(V_{GS} - V_{th})V_{DS} - \tfrac{1}{2}V_{DS}^2] \qquad (12)$$

where K_{lin} is the device parameter, V_{GS} is the gate to source voltage of the MOS transistor, V_{DS} is the drain to source voltage of the MOS transistor, and V_{th} is the threshold voltage. Thus, the output current will have a linear relationship with the applied input gate-to-source voltage under a constant drain-to-source voltage. The transconductance, obtained from the derivative of the current-to-voltage characteristic, can be expressed as

$$G_m=\delta I_D / \delta V_{GS}= K_{lin}V_{DS} \qquad (13)$$

The above equation is obtained by assuming that the V_{DS} voltage doesn't change with the variation of V_{GS} voltage. However, efforts should be made to maintain the independence in realistic circuit implementation.

The transconductance is proportional to the V_{DS} voltage from above equation, so the transconductance tuning can be achieved. However, if a large tuning range is required, the MOS transistor operation will shift from the triode region to the saturation region owing to the increased V_{DS} voltage and thus degrading the linearity performance

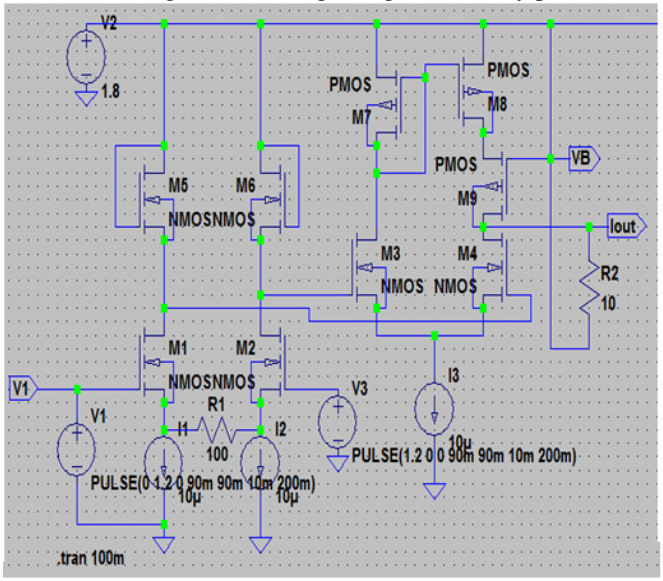

Figure9: The Design Archetecture of Transconductor Cell

A CMOS transconductor for multi-mode channel selection filter is presented. The transconductor includes a voltage-to-current converter multiplier. Voltage-to-current conversion employs linear region MOS transistors and the circuit features high linearity over a wide input swing range. The current multiplier, which operates in the weak inversion region, provides a wide transconductance tuning range without degrading the linearity. A third-order Butterworth low-pass filter implemented with the transconductors was designed by LT-SPICE 180nm CMOS process. The measurement results show that the filter can operate with the cutoff frequency of 135kHz to 2.2MHz. The tuning range and the linearity performance would be suitable for the wireless specifications of GSM, Bluetooth, cdma2000, and Wide-band CDMA. In the design, the maximum power consumption at the highest cutoff frequency is 2mW under a 1-V supply.

Experimental Results

The transconductor and the filter were fabricated in the 180 nm CMOS process. Body effects can be simply eliminated by connecting the source and the bulk terminals together in the process. The aspect ratio of 11.5um/2um is used for transistors M1 , M2 , M3, M4, M5, and M6, and 11.5um/0.2um is used for transistors M7, M8, and M9. The value of 8um/4um is used for MR5 and MR6, and Iref is equal to 20uA in the euivalent resistor circuit. 1um/1um is used for linear region MOS resistor MRS. Since the mismatches in transconductors and capacitors directly translate to the degradation of overall performance, such as nonlinear effects and errors of transformation, the filter has been laid out very carefully. Metal-insulator-Metal capacitors were used in the circuit and the unit of the capacitor array is 0.1pF. In this section, the experimental results are presented. All of the results were obtained with a single power supply voltage of 1.8-V.

The measurement results of the transconductor's transfer curves are shown in figure10, 11, 12 and 13. In figure10, the measurements of voltage to current transfer curves are obtained when both the input and output stages of the transconductor operate in the weak inversion region as Ic1 equals to 10nA and Ic2 changes from 10nA to 80nA. The saturated resistor circuit is selected here by setting Vmode to GND. The transfer curves in the weak inversion region follow the expected formula described previously. Also, the transconductance is changed from 2.5nS to 16nS, as shown in the figure9. In figure11, owing to the increment of Ic2, the output stage of the transconductor extends the operation from the weak inversion region to the strong inversion region while the input stage and the equivalent resistor remain in the same previous condition, and thus achieves to a much larger transconductance. The measured transconductance could be tuned form 3nS to 610nS by increasing Ic2 to the value of 10uA.

In figure12, the input and output stages of the transconductor both operate in the strong inversion region to achieve a large transconductance, as compared with the weak inversion region operation. The linear region MOS resistor circuit is selected here by setting Vmode to VDD. The transconductance from 11uS to 18uS is obtained while the current Ic1 equals to 1uA and Ic2 changes from 10uA to 40uA. We can find that the transconductance would be tuned proportional to the square root of Ic2 as described in the formula above. In figure13, the decreased Ic2 results that the output stage of the transconductor extends the operation from the equivalent resistor remain in the same condition, and thus achieves to a much smaller transconductance. As shown in the figure, the transconductance could be tuned from 20.2uS to 0.19uS by decreasing Ic2 to the value of 0.5uA.

From the measurement results of figure11 and 13, continuous tuning from weak inversion operation to strong inversion operation can be guaranteed and the transconductor can be tuned for a very wide range. However, the linearity of the transconductor should be maintained over the range because it will directly affect the linearity of the proposed Gm-C filter. For the linearity of this transconductor, when both the input and output stages of the transconductor operate in the weak inversion region, and THD is about -56dB with Ic1 = 10nA Ic2 = 10nA at 100Hz 300Vpp input signal. As Ic2 increases to 10uA, the output stage will operate in the strong inversion region while the input stage stays in the weak inversion region, and THD is measured to be -44dB. On the other hand, when the input and output stages of the transconductor operate in the strong inversion region, THD of -43dB is measured by giving Ic1 = 1uA and Ic2 = 40 uA with 10 KHz 300mVpp input signal.

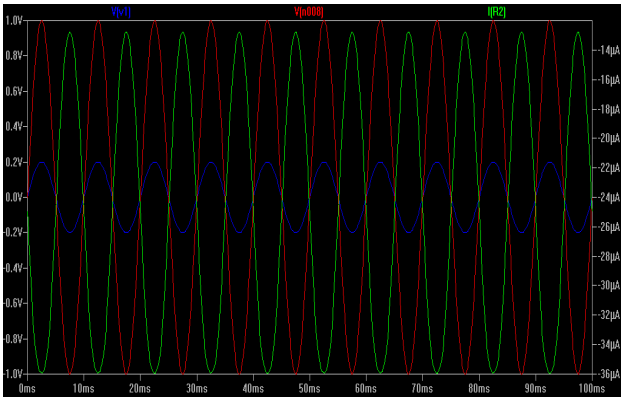

Figure10

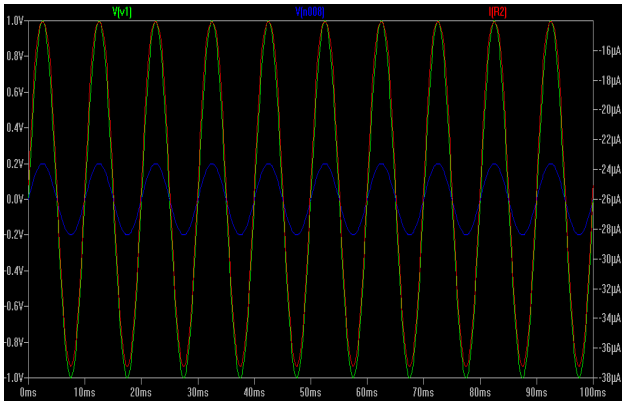

Figure11

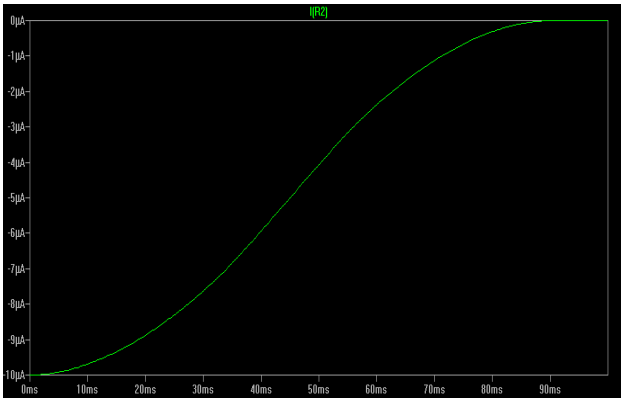

Figure12

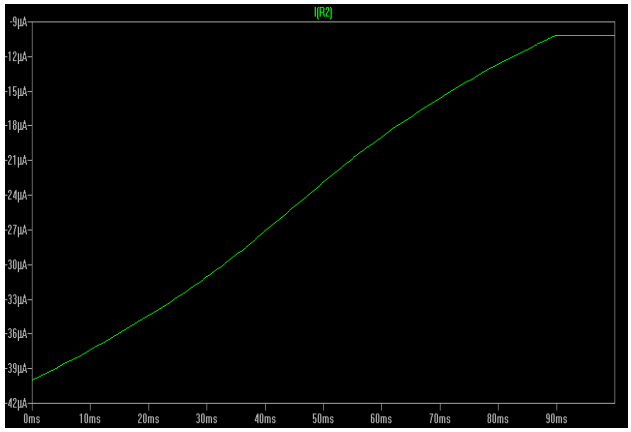

Figure13

Input signals with higher frequency are applied here owing to the fact that the large transconductance would be used for the filter with higher cutoff frequency. As Ic2 decreases to 0.5uA, the output stage of the transconductor operates in the weak inversion region while the input stage stays in the same region, and THD of -42 dB is measured.

Table 3 illustrates the filter measurement results over the tuning range for different bias currents Ic1 and Ic2. The cutoff frequecy can be tuned from 250Hz to 1 MHz, a tuning ratio of 4,000. The third-order inter-modulation distortion, which implies the linearity performance of the proposed filter, is measured at cutoff frequency. By using two sinusoidal tones with the amplitude of 300mVpp, -53dB is measured when the filter operates at low cutoff frequency of 250Hz. On the other hand, when the filter operates at low cutoff frequency of 250Hz. On the other hand, when the cutoff freuncy of the filter is tuned to 1 MHz, the IM3 versus cutoff frequency for the proposed wide tuning range filter. The worst case which happens in the middle band of the wide tuning range filter.

The worst case which happens in the middle band of the wide tunable filter is due to the multi-inversion operation.When the cutoff frequency of the filter is 250Hz, a dynamic range of 52 dB is measured with the 300mVpp input signal as Vmode is set to ground voltage. On the other hand, at the cutoff frequency of 1 MHz, a 48 dB dynamic range is measured as Vmode is set to VDD voltage. The measured PSRR at 100Hz is 36dB. The filter dissipates 0.2mW and 0.8mW for lowest and highest cutoff frequency setting, respectively, at 1.8-V supply

TABLE I. FILTER COMPONENT SIZES

Transistor Sizing	
DEV ICE	**W/L**
M1	11.5µm/2µm
M2	11.5µm/2µm
M3	11.5µm/2µm
M4	11.5µm/2µm
M5	11.5µm/2µm
M6	11.5µm/2µm
M7	11.5µm/0.2µm
M8	11.5µm/0.2µm
M9	11.5µm/0.2µm

Capacitor Values	
DEV ICE	**capacitance**
C1	0.1pF
C2	0.1pF
C3	0.1pF
C4	0.1pF
C5	0.1pF
CL1	0.1pF
CL2	0.1pF

TABLE II. FILTER OPERATING IN WEAK INVERSION REGION

Ic1 (Weak)	**Ic2 (Weak)**	**Gm**	**THD (Vin=0.3sin100 Hz)**	**IM3 (Vin=0.3sin250 Hz)**
10nA	10nA	2.5nS	-56dB	-53dB
10nA	20nA	4.8nS	-55dB	-53dB
10nA	30nA	8.0nS	-54dB	-52dB
10nA	40nA	10nS	-54dB	-52dB
10nA	50nA	13nS	-53dB	-51dB
10nA	60nA	14nS	-53dB	-51dB
10nA	70nA	15nS	-52dB	-50dB
10nA	80nA	16nS	-52dB	-50dB
10nA	10µA (strong)	610nS	-44dB	-48dB

TABLE III. FILTER OPERATING IN STRONG INVERSION REGION

Ic1 (Strong)	**Ic2 (Strong)**	**Gm**	**THD (Vin=0.3sin10K Hz)**	**IM3 (Vin=0.3sin1M Hz)**
1µA	10µA	11µS	-46dB	-48dB
1µA	20µA	14µS	-45dB	-47dB
1µA	30µA	16µS	-44dB	-46dB
1µA	40µA	18µS	-43dB	-45dB
1µA	0.5µA (weak)	0.2µS	-42dB	-41dB

TABLE IV. FILTER PERFORMANCE SUMMARY

Technology	LT SPICE Circuit Simulation
Supply Voltage	1.8 Volts
Filter Type	Fifth-order elliptic low-pass
Tuning Range	250Hz to 1MHz
Tuning Ratio	4000
IM3 (for Vin=0.3Vpp, f=250Hz-1MHz)	-40dB
Dynamic Range	48dB
Power consumption	0.8mW

V. CONCLUSION

There are so many simulation techniques to realize the analog devices. This is a wide variety application oriented simulation of filter design. There is a wide tuning range achieved.

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