# Impact of NBTI on SRAM Arrays for efficiency Improvement through Recovery Boosting

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**Abstract- Negative Bias Temperature Instability is an important lifetime reliability problem in microprocessors. SRAM based structures with in the processor are especially susceptible to NBTI since one of the pMOS devices in the cell always has an input of '0'. SRAM's are widely used in controller & Processor memories. It supports high speed implementation. The SRAM exhibit a major problem called negative bias temperature instability (NBTI) while storing the data '0' so large amount of energy is wasted here. In our paper we are going to remove this hazard and we are going to modify the SRAM circuit using Recovery Boosting. As well as we are designing 4-Bit SRAM Through Recovery Boosting for improving READ and WRITE ability of the SRAM circuit. By this we are improving the efficiency of the circuit by reduction in power consumption. In this paper design, simulation, layout design are done by using DSCH and MICROWIND tools.**

***Keywords*- : NBTI, SRAM, Recovery Boosting.**

## 1. INTRODUCTION

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for digital systems. The use of integrated circuits in high performance computing telecommunications and consumer electronics has been growing at a very fast pace. This trend is expected to continue, with very important implications for power-efficient VLSI system designs. Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important consideration as performance and area.

**R**eliability is one of the biggest challenges facing the microprocessor industry today. With continued technology scaling, processors are becoming increasingly susceptible to hard errors. Hard errors are permanent faults that occur due to the wearing out of hardware structures over time. These failures occur partly due to design-time factors such as process parameters and wafer packaging, as well as runtime factors such as the utilization of the hardware resources and the operating temperature. It is important to ensure that the reliability of the micro architectural structures in the processor is maximized so that one can make use all the available hardware resources effectively over the entire service life of the chip.

One important hard error phenomenon is negative bias temperature instability (NBTI), which affects the lifetime of pMOS transistors. NBTI occurs when a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor. The negative bias can lead to the generation of interface traps at the Si/SiO2.

## 2. OVERVIEW OF NBTI

### A. ISSUES IN NBTI:

**Negative bias temperature instability** (NBTI) is a key reliability issue in MOSFETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also nMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance. The degradation exhibits logarithmic dependence on time.[8] It is commonly accepted that two kinds of trap contribute to NBTI:

- First, interface traps are generated. Those traps cannot be recovered over a reasonable time of operation. Some authors refer to them as permanent traps. Those traps are the same as the one created by Channel Hot Carrier. In the case of NBTI, it is believed that the electric field is able to break Si-H bonds located at the Silicon-oxide interface. H is released in the substrate where it migrates. The remaining dangling bond Si- (Pb center) contributes to the threshold voltage degradation [7].
- On top of the interface states generation some pre-existing traps located in the bulk of the dielectric (and supposedly nitrogen related), are filled with holes coming from the channel of pMOS. Those traps can be emptied when the stress voltage is removed. This Vth degradation can be recovered over time [7].

The existence of two coexisting mechanisms created a large controversy, with the main controversial point being about the recoverable aspect of interface traps. The situation is clearer but not completely solved. A tight coupling between two mechanisms may exist but nothing is demonstrated clearly.

## 3. SRAM

**Static random-access memory** (SRAM) is a type of semiconductor memory where the word static indicates that, unlike dynamic RAM (DRAM), it does not need to be periodically refreshed,as SRAM uses bistable latching circuitry to store each bit. SRAM exhibits data remanence [10], but is still volatile in the conventional sense that data is eventually lost when the memory is

not powered. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote **0** and **1**. Two additional access transistors serve to control the access to a storage cell during read and write operations. A typical SRAM uses six MOSFETs to store each memory bit. In addition to such 6T SRAM, other kinds of SRAM chips use 8T, 10T, or more transistors per bit [1]. This is sometimes used to implement more than one (read and/or write) port, which may be useful in certain types of video memory and register files implemented with multi-ported SRAM circuitry. Generally, the fewer transistors needed per cell, the smaller each cell can be. Since the cost of processing silicon wafer is relatively fixed, using smaller cells and so packing more bits on one wafer reduces the cost per bit of memory. Memory cells that use fewer than 6 transistors are possible - but such 3T or 1T cells are DRAM, not SRAM. Access to the cell is enabled by the word line (WL in Fig.1) which controls the two access transistors M5 and M6 which, in turn, control whether the cell should be connected to the bit lines: BLB and BL. They are used to transfer data for both read and write operations. Although it is not strictly necessary to have two bit lines, both the signal and its inverse are typically provided in order to improve noise margins.

During read accesses, the bit lines are actively driven high and low by the inverters in the SRAM cell. This improves SRAM bandwidth compared to DRAMs - in a DRAM, the bit line is connected to storage capacitors and charge sharing causes the bitline to swing upwards or allows for differential signaling, which makes small voltage swings more easily detectable. Another difference with DRAM that contributes to making SRAM faster is that commercial chips accept all address bits at a time.

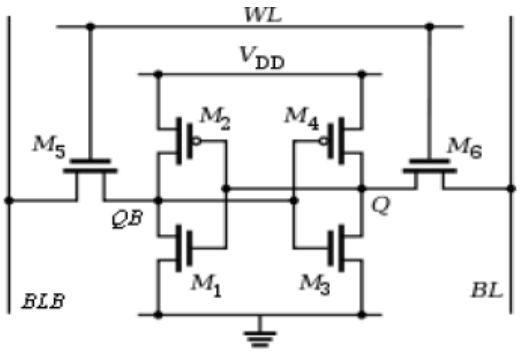


Fig1: Basic SRAM cell

**4. SRAM OPERATION**

An SRAM cell has three different states it can be in: standby (the circuit is idle), reading (the data has been requested) and writing (updating the contents). The SRAM to operate in read mode and write mode should have "readability" and "write stability" respectively. The three different states work as follows:

**a) STANDBY:** If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

**b) READING:** Assume that the content of the memory is a 1, stored at Q. The read cycle is started by pre-charging both the bit lines to a logical 1, then asserting the WL, enabling both the access transistors. The second step occurs when the values stored in Q and QB are transferred to the bit lines by leaving BL at its pre-charged value and discharging BLB through M1 and M5 to a logic 0 (i.e. eventually discharging through the transistor M1 as it is turned on because the Q is logically set to 1). On the BL side, the transistors M4 and M6 pull the bit line toward VDD, logic 1 (i.e. eventually being charged by the transistor M4 as it is turned on because QB is logically set to 0). If the content of the memory was 0, the opposite would happen and BLB would be pulled toward 1 and BL toward 0. Then these BL and BLB will have a small difference of delta between them and then these lines reach a sense amplifier, which will sense which line has higher voltage and thus will tell whether there was 1 stored or 0. The higher the sensitivity of sense amplifier, the faster the speed of read operation [9].

**c) WRITING:** The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write 0, we would apply 0 to the bit lines, i.e. setting BLB to 1 and BL to 0. This is similar to applying a reset pulse to an SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation [9].

**5. EFFECT OF NBTI IN SRAMS**

NBTI occurs when a negative bias (i.e., a logic input of “0”) is applied at the gate of a pMOS transistor. The negative bias can lead to the generation of interface traps at the Si/SiO2 interface, which cause an increase in the Vth of the device. This increase in the Vth degrades the speed of the device and reduces the noise margin of the circuit, eventually causing the circuit to fail [2], [3]. One interesting aspect of NBTI is that some of the interface traps can be eliminated by applying a logic input of “1” at the gate of the pMOS device.

This puts the device into what is known as the recovery mode which has a “self-healing” effect on the device [4]. Memory arrays that use static random access memory (SRAM) cells are especially susceptible to NBTI. SRAM cells consist of cross-coupled inverters that contain pMOS devices. Since each memory cell stores either a “0” or a “1” at all times, one of the pMOS devices in each cell always has a logic input of “0.” Since modern processor cores are composed of several critical SRAM-based structures, such as the register file and the issue queue, it is important to mitigate the impact of NBTI on these structures to

maximize their lifetimes. Previous work on applying recovery techniques to SRAM structures aim to balance the degradation of the two pMOS devices in a memory cell by attempting to keep the inputs to each device at a logic input of "0" exactly 50% of the time [4], [2], [6] . However, one of the devices is always in the negative bias condition at any given time. In this paper, we propose a novel technique called Recovery Boosting that allows both pMOS devices in the memory cell to be put into the recovery mode. The basic idea is to raise the ground voltage and the bit lines to Vdd when the cell does not contain valid data [5].

**6. Recovery Boosting**

By adding this control line the pMOS device in the logic'1' stage can be changed from negative bias to the forward bias mode. Thus the NBTI can be removed & the transistor in the 1 stage can be made off. So we can reduce the power consumption in that pMOS device. In the memory cell design given in Fig. 2, the CR signal serves the same purpose as before. When a value of "0" is input to the CR line to transition the cell into the recovery boost mode, in addition to raising the ground voltage, the two extra pMOS devices connected to the Vdd rail are also turned on.

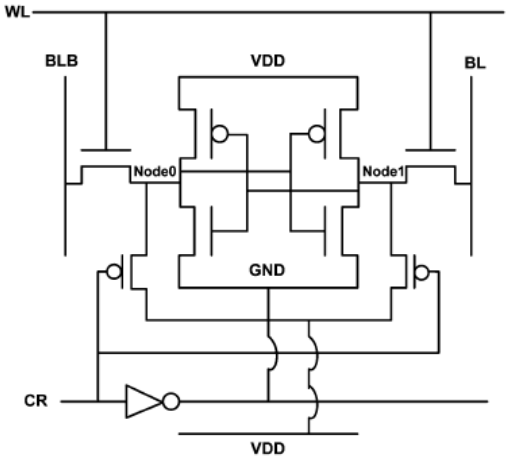


Fig2:Recovery Boosting

| CR | WL | BL | BLB | Node0 | Node1 | Operation |
|---|---|---|---|---|---|---|
| 1 | 0 | X | X | 0/1 | 1/0 | Hold |
| 1 | 1 | 1 | 1 | 0/1 | 1/0 | Read |
| 1 | 1 | 1 | 0 | 0 | 1 | Write '1' |
| 1 | 1 | 0 | 1 | 1 | 0 | Write '0' |
| 0 | X | X | X | 1 | 1 | Recovery Boost |

Table1:modified SRAM Cell Operation

Therefore, by raising the ground and connecting the bitcell to Vdd, the cell can be transitioned into the recovery boost mode without affecting cells in other rows of the array. We make the extra pMOS devices resilient against NBTI by using high- Vt transistors. Although high- Vt devices are slower, these devices are used only when transitioning the cell into the recovery boost mode and not when transitioning to the normal operating mode. Therefore, these devices do not impact performance but may delay the transition into the recovery boost mode. Moreover, since these devices do not lie on the performance critical path, they are sized so as to minimize the overall area. However, the pMOS devices do consume leakage power [5].

**7. 4-Bit SRAM Array**

An SRAM array that uses this cell for controlling individual entries to operate either in normal or recovery boost mode is shown in Fig.3.

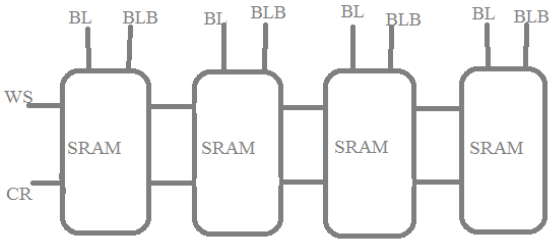


Fig3: 4-Bit SRAM cell

**8. RESULT ANALYSIS**

The existing SRAM cell will leads to power dissipation by applying a negative bias (i.e., a logic input of "0") at the gate of a pMOS transistor. This causes negative bias temperature instability. The proposed SRAM cell will reduce power dissipation by providing a control line. The proposed system enhances efficiency by error free transmission. SRAM array consumes less power than basic SRAM cell. The simulation result shown in Fig. 4(a),4(b) and Fig.4(c) are power calculated for conventional SRAM

and SRAM with control line. The Table shows that SRAM with control line power will be less when compared with conventional SRAM circuit. The power analysis is performed using Microwind tool.

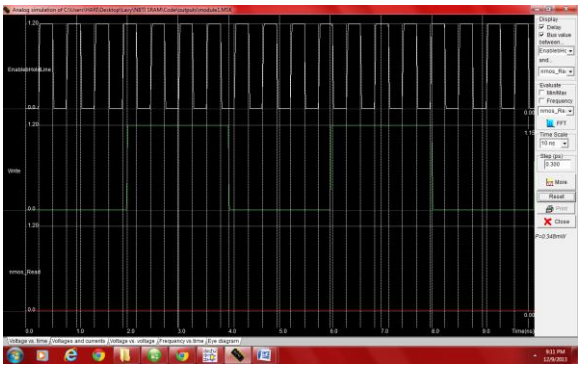

Fig 4(a): basic SRAM cell

Fig4(b): SRAM through recovery boosting

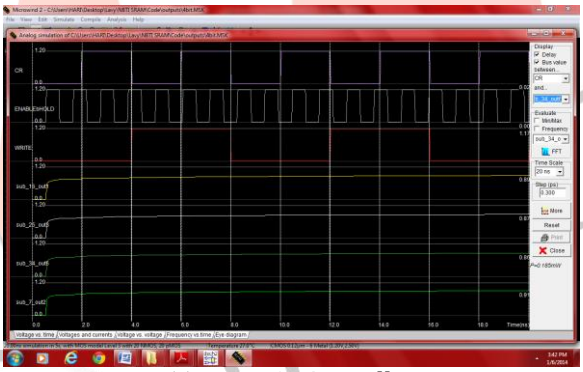

Fig4(c): 4-Bit SRAM cell output

**9. Comparison Table**

| Circuit | Power | Area |
|---|---|---|
| SRAM cell | 0.348 mw | 87.7 µm2 |
| SRAM with CR | 77.84 µw | 107.4 µm2 |
| Recovery Boosting | 0.186 mw | 153.0 µm2 |
| 4-Bit SRAM | 0.185 mw | 501.8 µm2 |

Table 2

**10. CONCLUSION**

In this paper, we propose recovery boosting, a technique that allows both pMOS devices in the cell to be put into the recovery mode by raising the ground voltage and the bit line to Vdd. So that NBTI problem is reduced. We show how fine-grained recovery boosting can be used to design the array of SRAM's and evaluate their designs via Microwind level simulations. By this we are also reduced power dissipation of the circuit. And also we designed 4bit SRAM array to improve the read and write ability of the circuit.

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