Design and Implementation of High Gain, High Bandwidth CMOS Folded cascode Operational Transconductance Amplifier

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***Abstract*— This paper deals with design and analysis of CMOS folded-cascode operational transconductance amplifier. Operational transconductance Amplifier (OTA) is a fundamental building block of analog circuits and systems which were previously implemented by using OPAMP. First description of optimum OTA architecture is given to optimize transistor sizing. Second, a design of folded cascode OTA, which is useful in high frequency applications like RF application. In order to implement higher frequency application, we need OTAs which have both high (DC) gain and a high bandwidth. The designed folded-cascode OTA are implemented in 0.13µm CMOS process with BSIM3V3 level 49 MOSFET model and simulation results are performed using SPICE software. From it is found that designed folded cascode OTA has a 53.99dB DC gain, around 351 MHz unity gain bandwidth and 53° phase margin.**

Index Term- Folded-cascode OTA, Unity gain bandwidth, Op-amp,

I. INTRODUCTION

The design automation of analog integrated circuits is a demanding task in microelectronics industry due to the crescent necessity for low power design and time to market. The objective of analog circuit design is to map signal conditioning constrains into electronic circuit blocks that meet those specifications. This task is a challenging activity because the analog design procedure targets complex design specifications like dynamic range, noise, offset voltages, gain, etc. These parameters are closely related to transistor sizing, device technology dependent. So design process imposes to designers to make some choices based on their experience to achieve successful design.

Today operational amplifiers (OPAMPs) are used to implement variety of analog applications such as amplifiers, summers, integrators, differentiators, filters and oscillators. OPAMPs work well for low-frequency applications, such as audio and video systems but for higher frequencies, OPAMP designs become difficult due to their frequency limit [6].At those high frequencies, operational transconductance amplifiers (OTAs) are deemed to be promising to replace OPAMPS as the building blocks.

This paper is organized as follows. An Optimum Architecture of OTA was introduced in section II. Section III describes design of this OTA, Section IV present simulation results, section V shows comparative analysis with previous work while section VI provides concluding remarks.

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II. OPTIMUM OTA ARCHITECTURE

Several issues exist for selecting optimum architecture. Choice aimed both at large gain and large bandwidth. In order to achieve high gain, the differential telescopic topologies can be used. The telescopic architecture has low power consumption and it is a low noise OTA but Limited output swing and difficulty in shorting the input and output are two main drawback of this architecture [15].

In order to overcome some of the drawbacks of telescopic OTA, a folded cascode OTA based on cascode current mirror can be used. This OTA has good power supply rejection ratio (PSRR) compared to two stage OTA since the OTA is compensated with load capacitance.

A. Folded cascode OTA

The Operational Transconductance amplifiers (OTA's) are important building blocks for various analog circuits and systems which were previously implemented by using OPAMP. OTA is an amplifier whose differential input voltage produces an output current and hence it is a voltage controlled current source.OTA is an OP-amp without an output buffer and can drive capacitive loads.

An OTA is amplifier whose all nodes are at low impedance except input and output nodes. Transconductance of OTA can be adjusted by bias current. The performance of OTA is limited by its input and output swing. To overcome these limits of simple OTA, folded cascode OTA is used.

Folded cascode OTA is shown in Fig 1. The name "folded cascode" comes from folding down n-channel cascode active loads of a diff-pair and changing the MOSFETs to p-channels.

The input stage provides the gain of the operational amplifier. First, one has to know why NMOS transistor had been chosen. For a comparable device dimensions and bias currents, the PMOS input differential pair exhibits a lower transconductance than a

NMOS pair does. This is due to the greater mobility of NMOS device [5]. The first stage should provide the largest gain, so NMOS transistor has been chosen.

B. Circuit Analysis

The Folded cascode OTA has a differential stage consisting of NMOS transistors M_1 and M_2. MOSFETS M_3 and M_4 Provide the DC bias voltages to M_5-M_6-M_7-M_8 transistors.

Apply AC input Voltage between V+ and V-, cause the diff-amplifier drain current to become gmVin. This AC differential drain current is mirrored in the cascaded MOSFETs M9 to M12.

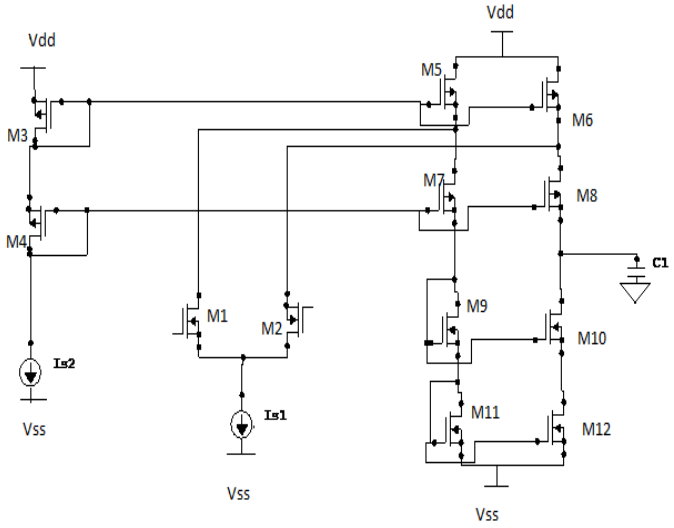

Figure1. Folded cascode OTA [14]

The output Voltage of the OTA is given by:

$$\mathbf{Vout = g_m V_{in} Ro} \quad \textbf{(1)}$$

The "Unity gain frequency" of the OTA is:

$$\mathbf{Fu = g_{m1}/2\pi C_L} \quad \textbf{(2)}$$

Transconductance of OTA is computed as

$$\mathbf{g_m = 2\pi GBWC_L} \quad \textbf{(3)}$$

The open-loop voltage gain is given by:

$$\mathbf{A_v = \{g_{m1}\, g_{m8}\, gm_{10}\}/\, I_D^{\,2}(g_{m8}\lambda_P^{\,2} + g_{m10}\lambda_N^{\,2})} \quad \textbf{(4)}$$

Where, g_{m1}, g_{m8} and g_{m10} are respectively the transconductances of transistors M1, M8 and M10. I_D is the bias current flowing in MOSFETs M1, M8, and M10. Like, C_L is the capacitance at the output node. λ_N and λ_P are the parameters related to channel length modulation respectively for NMOS and PMOS devices. Taking the complementarities between the Transistors M4 and M6 into account: $g_{m8} = g_{m10}$.

The dominant pole of OTA is located at $1/2\prod R_oC_L$. Parasitic poles exist at the sources of M7/M8 and M9/M10.These parasitic pole should be larger than the unity gain frequency of OTA.

III. DESIGN OF FOLDED CASCODE OTA

Based on design steps, following dimensions are found.

Table 1:- Device dimensions

M9, M10, M11, M12	2.52µm

Table 2:-Specifications

Gain	60dB
Unity gain bandwidth	300MHz
Phase margin	55°
Load capacitance(C_L)	0.1pF
Technology	0.13µm

THE DESIGNED FOLDED CASCODE OTA WAS BIASED AT 1.2V POWER SUPPLY VOLTAGE USING CMOS TECHNOLOGY OF 0.13MM WITH THE BSIM3V3 LEVEL 49 MOSFET MODEL

IV. SIMULATION RESULT

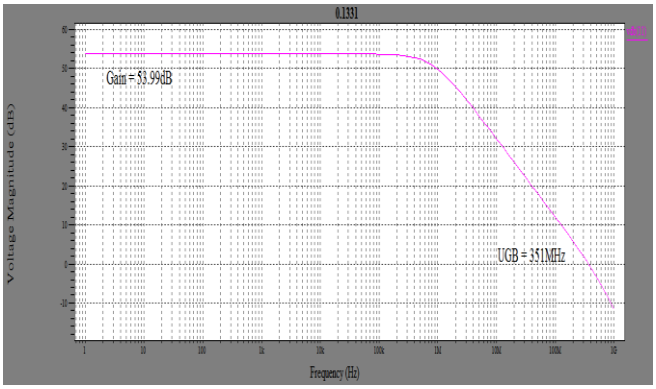

Figure 2:- gain, unity gain bandwidth

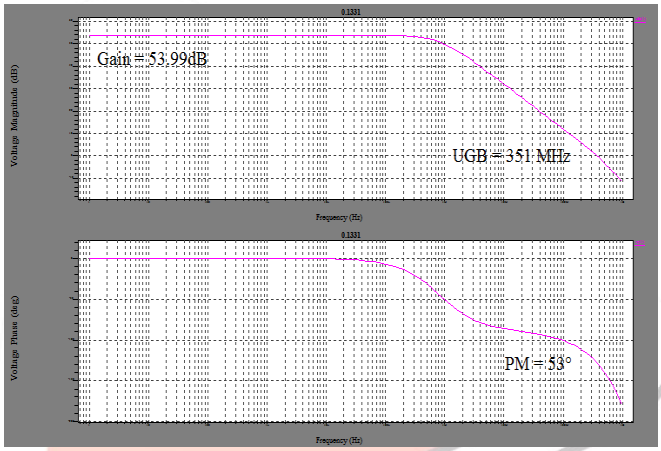

Figure 3. Phase Margin

Simulation result of Common Mode gain is shown in figure 4. From this we can get CMRR is 127.71dB

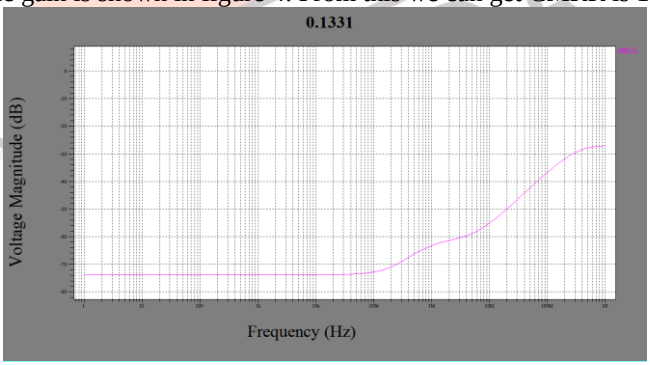

Figure 4. Common mode gain

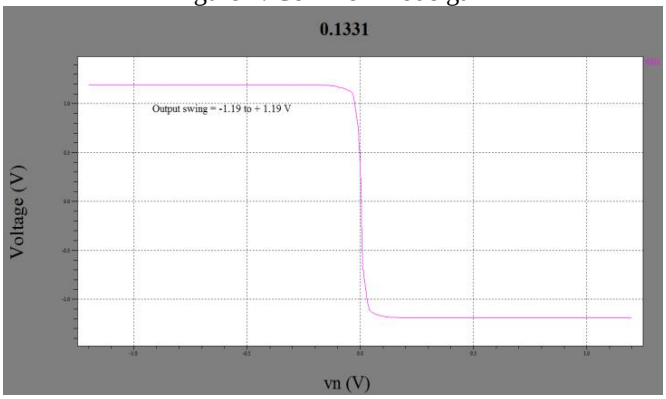

Figure 5. Output swing

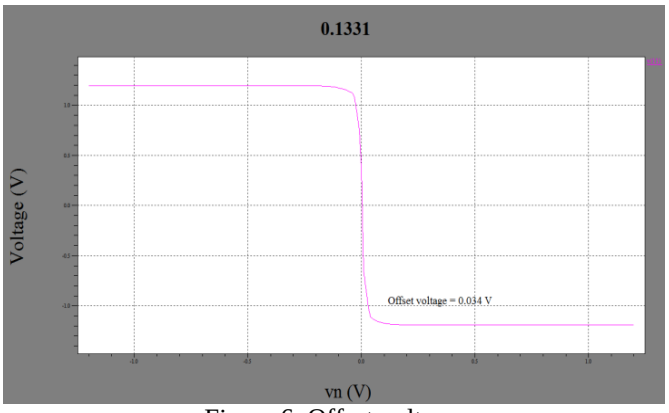

Figure 6. Offset voltage

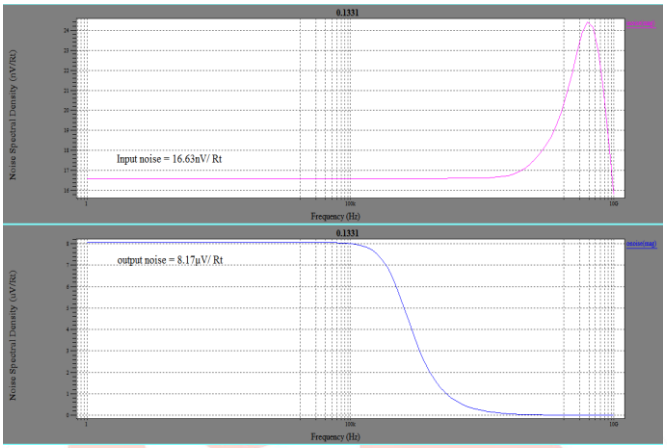

Figure 7. Input and output noise

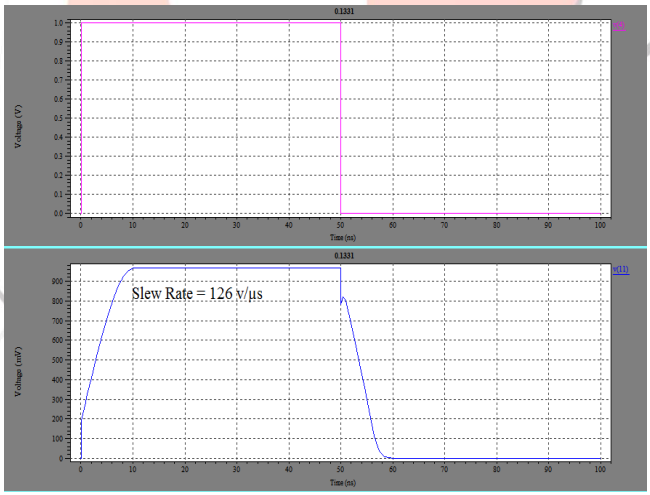

Figure 8. Slew rate

V. COMPARATIVE ANALYSIS

Parameter	[1]	[2]	[3]	[4]	[7]	[8]	[9]	[10]	[11]	[12]	Proposed work
Technology(μm)	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.18	0.13
Dc gain(dB)	68	80	95	71.7	46	80	-	76.26	62	70.02	53.99
UGB(MHz)	93.3	50	312	159	70.7	200	10	291	218.3	14.98	351
Phase margin(Degree)	80	58	56	70.3	83.6	89	-	79.88	79.3	78.76	53
Slew Rate (v/μs)	-	-	-	99	42.1	-	-	-	-	11.37	126

C_L(pF)	-	0.18	2	2.2	5.6	1	-	0.1	1	3	0.1
Supply voltage(v)	0.8	1	1.8	1	1.8	1.8	2.7	2	1.8	1.8	1.2
CMRR(dB)	-	-	70	-	-	-	-	-	-	-	127.71
Output swing	-	-	-	0.9	-	-	-	-	-	-	-1.19 V to 1.19 V
Offset voltage(V)	-	-	-		0.079	-	-	-	-	-	0.034
Input noise spectral density	-	-	-	-	-	-	-	-	-	-	16.63nV/ Rt
Output noise spectral density		-	-	-	-	-	-	-	-	-	8.17µV/ Rt

VI. CONCLUSION AND FUTURE SCOPE

This work presents a design method of CMOS Folded- cascode OTA in BSIM3V3 0.13µm technology. Behavioral simulation show that designed OTA achieves High gain and High unity gain bandwidth for ±1.2V power supply. This high bandwidth Folded-cascode OTA is very useful in the high bandwidth applications like RF application.

Future work would involve measurement of parameters using PMOS and PMOS‖NMOS differential pair in place of NMOS differential pair, layout, implementation of same design using gm/I_D methodology and to find percentage of variation in W/L and parameters with same specification..

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