Design of Low Power Gating Technique in NAND Type CAM Cell Architecture

(Low Power CAM)

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***Abstract*— Content addressable memory (CAM) is special type of flash memory is used to attain a high speed search function in a single clock cycle throughput making them faster than other hardware- and software-based search system .Binary CAM has a parallel active circuitry which consumes more power to its operation without scarifying its speed and memory .This paper deals with a parity based CAM operation to increase the performance in comparison part of the traditional CAM and NOR type cell is used in CAM architecture The proposed work includes the implementation of NAND/XNOR type CAM cell instead of its NOR type CAM cell which overcomes the limitation of the previously used type cell and obtain the less silicon area by minimizing the number of transistor in each cell. The power gated technique is used in these type of cell to optimize the power in comparison part by automatically turn off the power supply when the respected block is not in enable.**

***Index Terms*— Gated power, CMOS, content addressable memory (CAM), NAND-type CAM, searchline**

I. INTRODUCTION

A content addressable memory is an SRAM based memory which data are accessed by their content instead of its physical location. It is special kind of memory which have reverse operation of the traditional memory .CAM supplies data and get back the address in parallel search design so it is power hungry .Basically, CAM is categories into two:Binary CAM have logic 0 and logic 1 and ternary CAM have one extra digit is namely logic0, logic 1 and don't care X. The operation of CAM are read, store, compare and write mainly fastest compare operation is especially used in supporting CAM to attain the high speed search function in real time application.

This fast data search operation is indicating the match. However, query data is given in search data register and compare this data with memory bank if any match is found output is indicate a match. CAM is mainly used in high speed operation for low voltage and low power system performance. Nowadays, The widespread application of CAM such as Network routers, data compressors, packet forwarding, translation look-aside, artificial intelligence and image processing buffers for virtual memory systems, tag directories in fully associative cache organizations, logic inference, pattern matching. The Components of CAM are search data register, memory bank, searchline, matchline, sense amplifier and encoder. Low power can be obtain in CAM by consuming power in match line and search line operation. Replica technique for word line and search control in [2], Pipelined and hierarchical method is designed to matchline and searchline scheme[4]low power cam with segmented matchline is described in [7]. A high speed low power single ended sense amplifier can sense even a small change ML. in each row sense is required in form of MLSA. It is to sense the voltage change on ML and amplifies it. An encoder is used in the system where only a single match is expected.

In this paper, parity bit based CAM operation is to boost the search speed function. We propose a NAND type CAM cell architecture is designed using gated power technique which is compared with NOR type CAM cell. The rest of the paper is organized as follows- sections II describe the parity bit based CAM design. In section III NOR and NAND type CAM cell is designed using gated power technique. Section IV explains results discussion and performance comparison.

II. EXISTING METHODOLOGY

Parallel operation of CAM is obviously reduced the search time and also simultaneously increases power consumption. In previous work concentrate on the search operation such as pre-computation on one's count parameter extractor and block XOR approach to improve the efficiency of the power than pre-computation (PB-CAM).The PB-CAM comparison operation has two parts, first part is parameter extractor is to filter the unwanted match and second part is to compare the data.

This requires minimizing the comparison operation. The blocked XOR approach is based on eliminating Gaussian distribution and improves efficiency in comparison operation. The input data bit is divided into blocks.XOR logic operation is used in each block and valid bit is chosen and et into next step. A multiplexer is to select the correct parameter which is to optimize the power consumption than one's count pre-computation CAM.

III. PARITY BIT BASED CAM

The Parity bit computation is advanced technique of pre computation CAM .Basically pre-computation is the filtering process to eliminate mismatched data before it go to original comparison process .since pre-computation is calculated by one's complement method so it prevent from the unwanted matches in the comparison stage. Mismatch data bits can neglect in the starting stage of the comparison so it leads to speed up process shown in fig.1 Shows the parity bit computation where seven bit data be taken for computation here data bits are already stored in the memory bank if match occurs between search data and data bits match line will be enable.

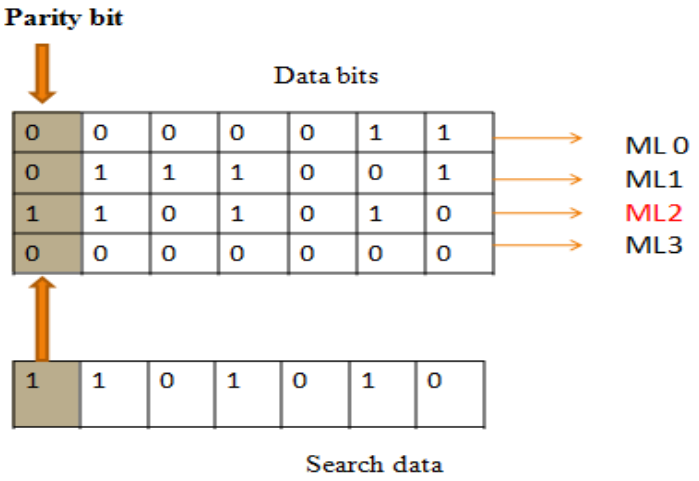

Fig.1 Parity Bit

Now consider a search data where seventh bit represents parity bit of the data if the given data seventh bit be computed as parity bit of the data if the given data contains odd number of one's it denoted in the seventh bit be '0' else '1' i.e., search data contain even number of one's. In previous method counting bits is stored in separate column where in presented method parity bit is stored with in memory cell column so it reduce area, delay and boost up the driving strength of mismatch by half. In the matched in the data segment (eg.,ML2),the parity bit of search data and stored bit is the same ,thus ML indicate a match .this match is indicate by activating ML line and it sense the voltage and produce output through priority encoder. other data be not checked because parity bit itself not matched and also 3-mismatch occurs in remaining data bits(eg.,ML0.ML1,ML3).finally ML2 matches all data as search data contain so ML2 be activated. In CAM architecture one extra area is concerned for parity bit so negligible area overhead with boost the compare operation obtain high speed.

IV. NOR/NAND CAM CELL IS DESIGNED USING GATED POWER TECHNIQUE

Basically CAM is designed in both NOR type and NAND type CAM cell.NOR type CAM is high performance in search function but disadvantages in low power .In contrast NAND (XNOR) type CAM is best in low power feature. Power gating technique is shown in Fig.2 used to reduced the power dissipation by shutting off the current to specific blocks of the circuit currently which are not in enable condition. This technique is used in both NOR/NAND type Cam cell architecture and its comparison

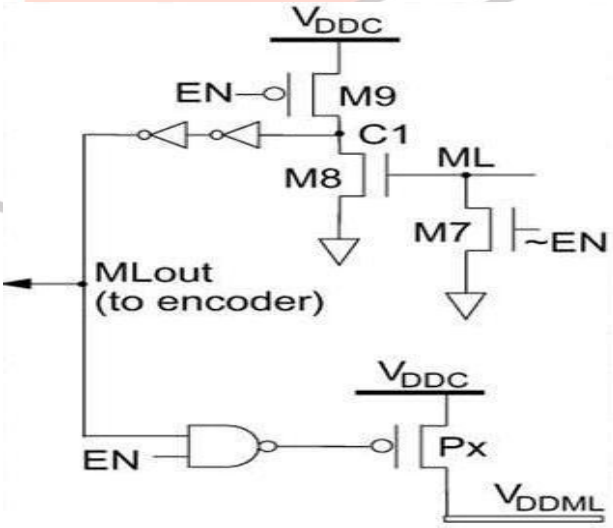

Fig.2 Power Controller Circuit

A. NOR/XOR type CAM cell architecture

This XOR type CAM cell is designed using power gating method. In CAM architecture each cell has a number of transistor .here conventional NOR type CAM is used in this block which contains 10 T transistor in each block. Traditional CAM block has mainly two parts namely store unit and compare unit is used to store the data and comparing data respectively. Naturally CAM is based on SRAM structure. here cross coupled inverter is used to store the data in floating fashion as like as SRAM structure and transistor M1to M4 is used in comparison part of the block. V_{DDML} and V_{DD} are two separate power supply where V_{DDML} is power supply for match line and V_{DD} is to isolate the comparison unit from the storing unit. It is to save the power consumed by the

disabled circuit. $_{PX}$ is power control where ML reaches certain threshold voltage it is automatically turn off the circuit .initially enable is zero i.e.,

precharge phase transistor is on condition then power controller is turned off .when input is given enable is one i.e., Evaluation phase where P_X will conduct.

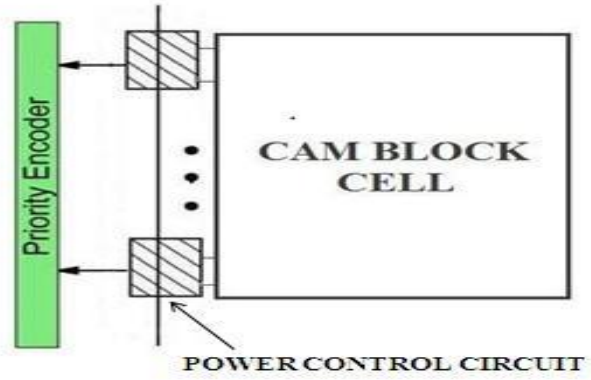

Fig. 3 Conventional CAM block is design using power controller circuit

NOR type cell has 10T inverters as shown in fig 4 its operation is based on power controller circuit. Consider a 4x4 matrix CAM cell is designed using schematic editor and performance can be analyzed through microwind/tanner tool.

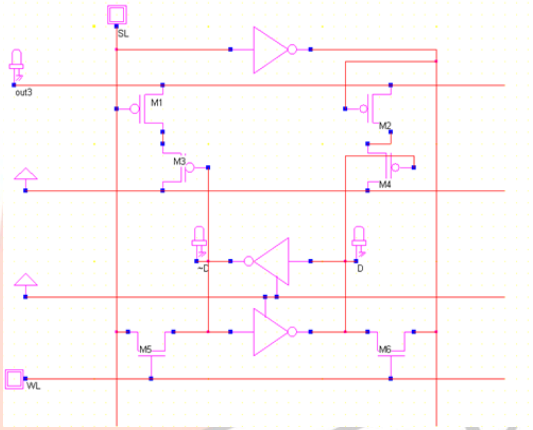

Fig.4 CAM cell is powered by two metal rails (XOR/NOR type)

B. NAND/XNOR Type CAM Cell Architecture

The NAND type cell is contrast to NOR type cell which is designed to reduce the power dissipation in search operation is shown in fig 5 .Pull down transistor is arranged in series fashion to consume more power than NOR. Now power gating is applied in NAND cell and it further improve the performance of low power. It contain 9T inverter as one inverter less as NOR in each block of cell consequently number of transistor is reduced than NOR. It also minimizes the area of the CAM. Specifically these cell is designed for 4x4 matrix and analyzed by microwind/tanner tool.

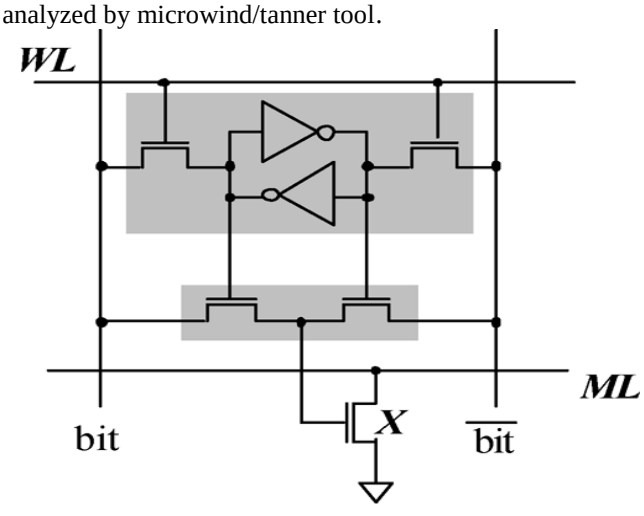

Fig.5 NAND/XNOR type CAM cell

V. SIMULATION RESULT AND DISCUSSION

The accurate method of both power reduction and search optimized design are performed. Simulation results to be verified.

A. Design Optimized For Search Speed

In this paper, we use 65-nm technology to implement the proposed parity based CAM. The design is simulated for seven input bit data and matching process is done according to even and odd parity and output is verified and shown in Fig6.This parity based CAM is simulated using modelsim/Xilinx .here, we verified the output using xilinx by using 65-nm technology .match line will be enable to indicate a output. comparison between pre-computation CAM and parity bit based CAM where pre-computation power dissipation be 107mW and parity bit based CAM power dissipation be 76mW similarly current consumed in pre-computation is 59mA and parity bit based CAM consumed 42mA.obvisouly total power is reduced in the parity bit based CAM. Therefore, total power consume in pre-computation will be 113 and parity will be 83

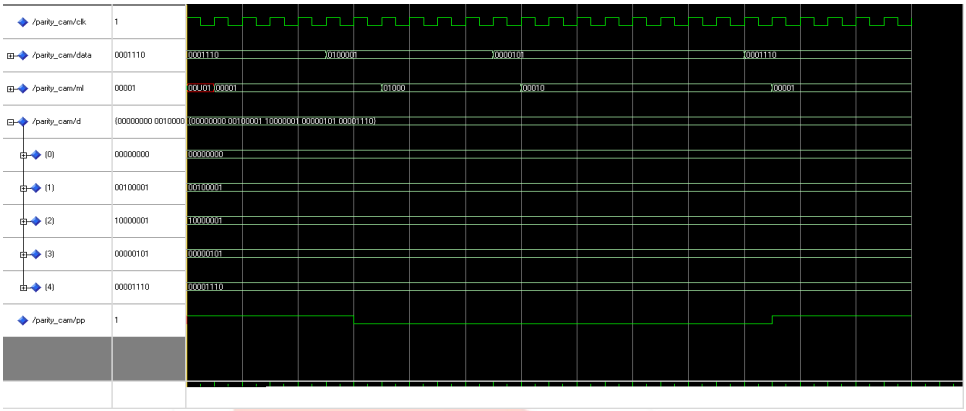

Fig. 6 Simulation Result Of Parity Bit

B. Design Optimized For Cell Architecture

Another way to optimize the power in CAM is cell architecture. To implement a NAND type CAM cell instead of NOR type CAM cell. Layout is simulated for NAND type cell architecture and voltage current waveform is obtained. NAND cell is to save power where this is designed to each row of circuit. Similarly power gating also low power. The layout is generated for both type of CAM cell design in architecture .A 4x4 matrix cell is designed using NOR type where parity bit based search operation is verified using Xilinx tool.

C. Peak Power Consumption

Peak power consumption is the maximum power consumption of the circuit when it execution the design. It also place a vital role in optimizing the power. Gated power technique is designed to reduce the peak power. It is estimated from worst case data pattern. The only difference between peak power consumption and power consumption is power dissipated in the one match line when it is switched .In NOR type CAM mismatched CAM data are consider to be a worst case pattern.

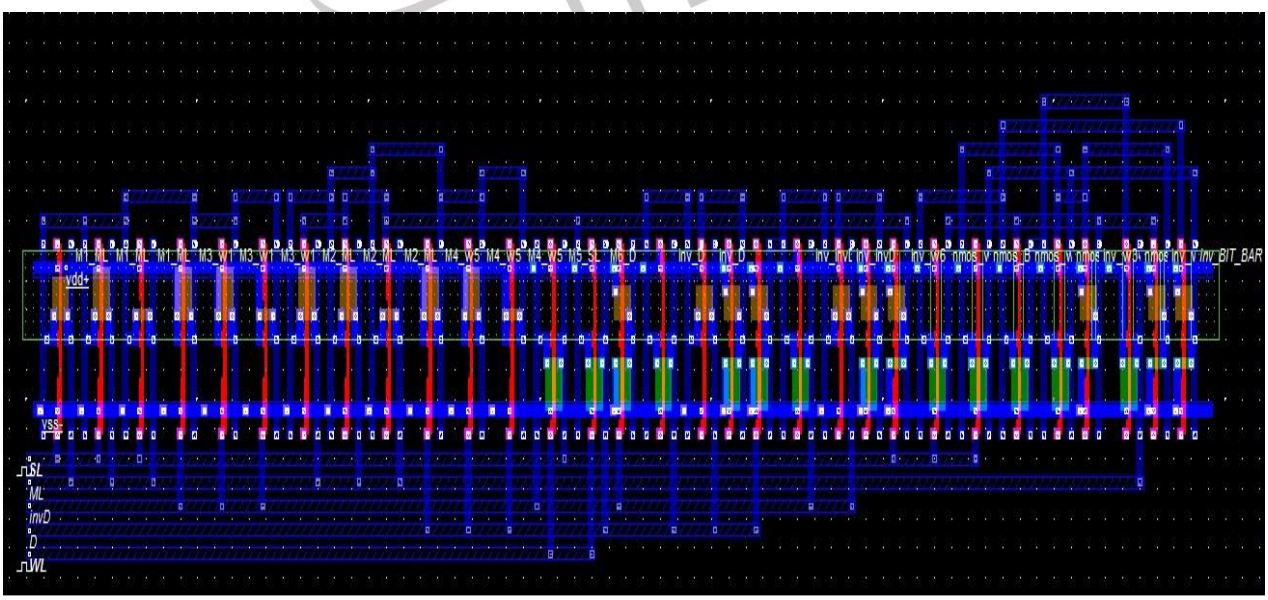

Fig. 7 Layout of NOR type CAM Cell using power gated technique

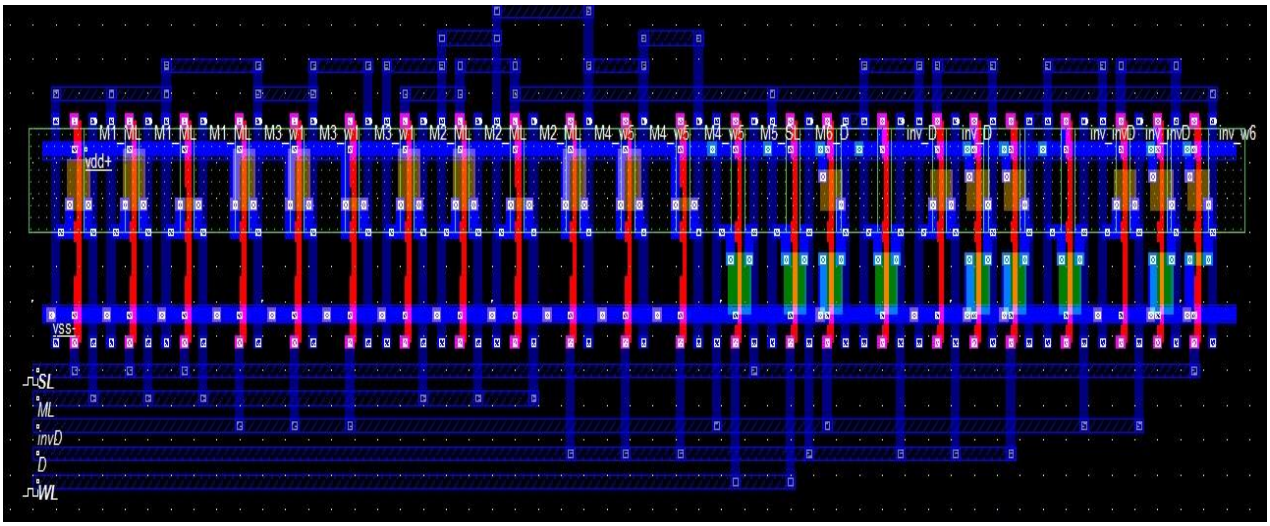

Fig 8 Layout of NAND type CAM Cell using power gated technique

Table I

Power Comparison Between NOR Type CAM Cell and NAND Type CAM Cell

NOR Type CAM Cell	NAND Type CAM Cell
Power Consumption= 61.926µW	Power Consumption =22.416µW

D .Dynamic power consumption

The power gated transistor reduces voltage swing on ML and automatically turned off feedback loop after the output is obtained in sense amplifier. so average power consumption is reduced. Tabulation I shows power comparison between NOR and NAND type CAM cell.

E. Process variation analysis

Process variation analysis is main issue in nano scale CMOS technology. The proposed design has smaller pull-down current due to gated power transistor P_X .Feedback loop is turned off automatically and it is insensitive.

VI.CONCLUSION

Content addressable memory is naturally a power hungry, its challenge to design of low power CAM. Mostly power dissipation is due to search line, and matchline part of CAM block. Parity bit based computation CAM is to boost the search operation of the CAM. Total power consumption in parity is 45% less than that of pre-computation CAM. Cell architecture is designed by NAND type cell rather NOR type cell using power gating technique in each block. Moreover, this is implement to whole CAM block to further optimize power.here,4x4 matrix cell is designed using NAND type cell and power consumption 35% is achieved.

ACKNOWLEDGMENT

The authors would thank Dr. P.N Neelekantan, Professor of Electronics and Communication Engineering, Dean of Electrical Science, Akshaya College of engineering and technology for his valuable suggestions and contributions. They would also like to thank the anonymous reviewers of IJEDR.

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