Analysis and Design of High Speed Low Power Comparator in ADC

[1]Abhishek Rai, [2]B Ananda Venkatesan

[1]M.Tech Scholar, [2]Assistant professor
Dept. of ECE, SRM University, Chennai
[1]Abhishekfan1791@gmail.com, [2]anandavenkatesan@gmail.com

***Abstract* — the fast growing electronics industry is pushing towards high speed low power analog to digital converters. Comparator is electronic devices which are mainly used in Analog to Digital converter (ADC). In ADC they are used for quantization process, and are mainly responsible for the delay produced and power consumed by an ADC. A high speed low power comparator is required to satisfy the future demands. The circuits presented in this paper are designed using 0.18µm CMOS technology with 1.8v bias voltage and 1-2µA bias current. This paper also discusses the advantage of using programmable hysteresis to the comparators. Tanner EDA environment is used for the design and simulation for the comparator circuits. Comparison of the proposed comparator with existing double tail comparator is performed and the result is discussed in detail.**

***Index Terms*— Double Tail Comparator, high speed Analog to digital converter (ADC), hysteresis, Two stage CMOS amplifier, tanner EDA.**

I. INTRODUCTION

The Comparators are used in analog-to-digital converters (ADCs), data transmission applications, switching power regulators and many other applications. The voltages that appear at the inputs are compared by the comparator that produces a binary output which represents a difference between them. They are critical components in analog-to-digital converters. Designing high-speed comparators becomes more challenging when working with smaller supply voltages. In other words, for a given technology, to attain high speed, transistors with increased width and length values are required to compensate for the reduction of supply voltage, which also means increased chip area and power [1]. So, Transistor width and length are adjusted accordingly for minimum power consumption and maximum operating speed.

Hysteresis in the comparator circuit is applied by feeding back a small portion of the output voltage to the positive input [2]. This feedback voltage adds a polarity-sensitive offset to the input, which results in increased threshold range. A small amount of hysteresis applied to the comparator circuit can prove to be very useful as it reduces the circuit's sensitivity to noise, and also helps reduce multiple transitions occurring at the output if the input is slowly changing its state.

A model for the comparator is developed and discussed, and its functionality is verified by showing a comparison of result obtained for the proposed model and the existing model. The platform used to develop and analyze the existing model is tanner eda tool.

The research paper is organized as follows: an introduction to CMOS comparator is given, followed by detailed analysis of high speed comparator architecture with properties for each structure will be discussed. Finally, simulation result for all the architecture will be shown and discussed.

II. CIRCUIT DESIGN AND ANALYSIS

The first comparator circuit is the two-stage CMOS amplifier with an output inverter which has a total of three stages. The first stage is a differential amplifier, the second is a common-source amplifier, and the third is an inverting buffer. In this circuit, the input bias current is designed for 1µA. This current is mirrored to the first two gain stages, so the total amount of bias current is 3µA. The two analog input voltages, are attached to the differential pair. 'Vim' is set as the reference voltage in this circuit. Since speed is more important than gain in this circuit design, the length of the transistors was chosen to be 0.18µm. An NMOS differential pair is used because NMOS transistors have higher mobility than PMOS transistors.

In order to improve the gain of the first stage and get better matching, that is, lower the input offset voltage, the widths of the input differential pair, NMOS1-NMOS2, were increased. A common source amplifier is used to contribute for the overall gain of the amplifier. With the goal of reducing the high parasitic capacitance of transistor PMOS2 which causes delay in the first input stage the area of common source transistor PMOS2 is increased [4]. The result was decrease in the propagation delay of the circuit. The third stage is the inverter buffer stage which adds modest gain and increases slew rate of the circuit. The circuit designed is shown in Fig.1 with length, width and multiplier values for each transistor.

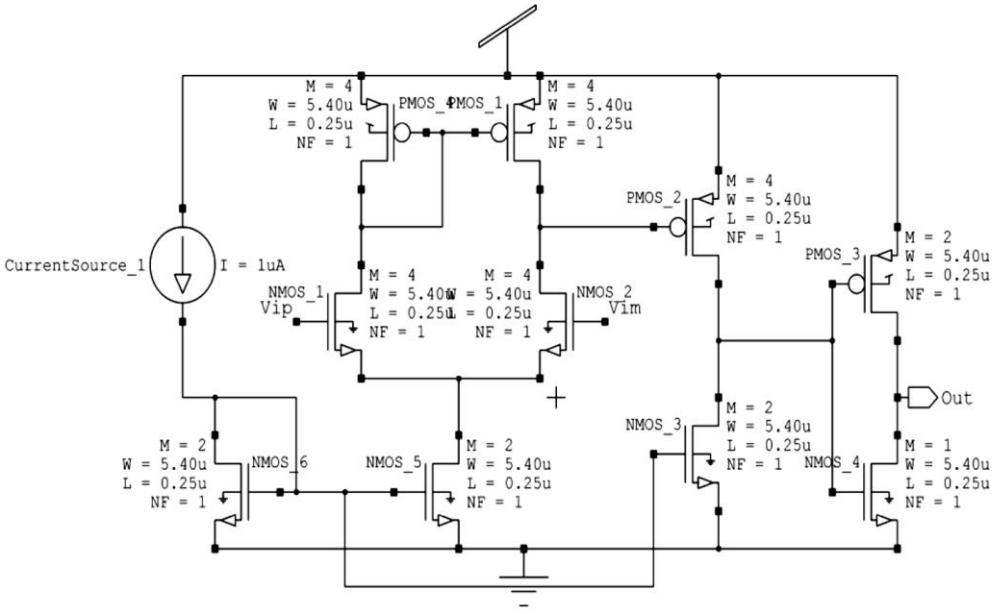

Fig. 1.First comparator: Two stage CMOS amplifier with output inverter

The problem in the design of first comparator circuit shown in Fig.1 is when the differencce between the two analog input reaches zero. Even a small amount of noise can cause spurious fluctuation in the comparator output. These fluctuations causes unnecessary power consumption in comparator circuit and also false result are produced. In practical applicatons noise can effect the output of the comparator. In fig.2 we can see how the output get affected with noisy input signal.

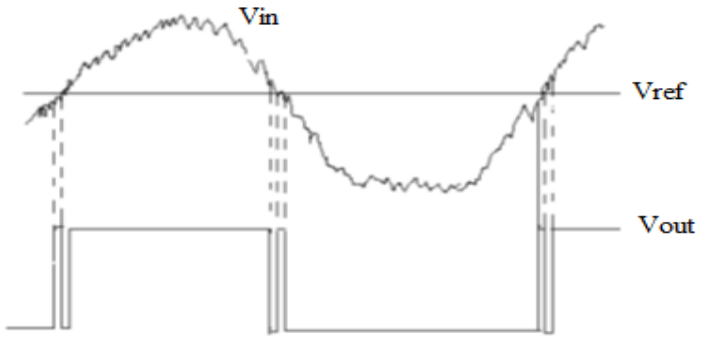

Fig. 2. Comparator response to noisy signal without hysteresis

To reduce the effect of noise in the first comparator circuit we use the concept of Hysteresis. Hysteresis is defined as the difference between the upper threshold voltage (V_{TH}) and Lower threshold voltage (V_{TL}) for which the output switches to higher value and to lower value respectively [3]. Hysteresis helps to reduce circuit sensitivity towards noise, and helps reduce multiple transition at the output. The response of comparator using hysteresis is shown in fig.3

V_{TH} = Upper threshold voltage

V_{TL} = lower threshold voltage

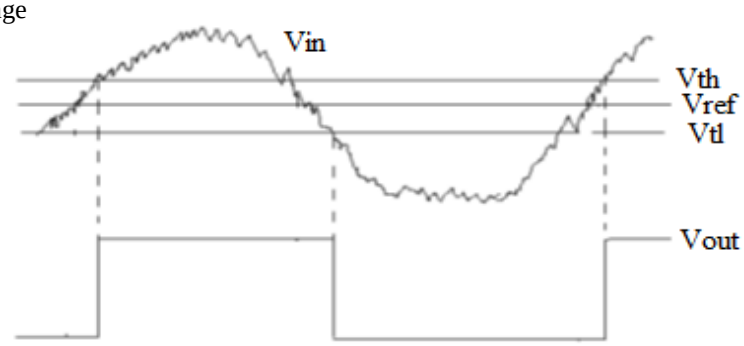

Fig. 3. Comparator response to noisy signal after adding hysteresis

A small amount of hysteresis is then used in the First comparator circuit to reduce the effect of noise in the circuit. A programmable hysteresis using an unbalanced differential pair is added in the first comparator circuit. The modified comparator circuit is shown in fig. 4.

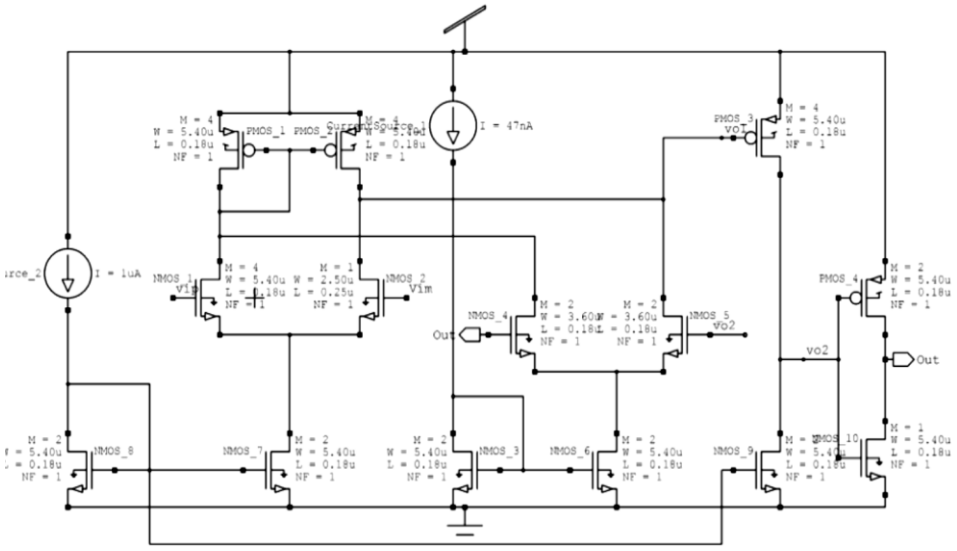

Fig. 4. Second comparator: Two-Stage Amplifiers with an Unbalanced Differential Pair

The second comparator circuit is a two stage CMOS amplifier with unbalanced differential pair plus output inverter. An explanation of the working of the circuit is as follows. A second differential pair, NMOS4-NMOS5, unbalances the input differential pair. The gates of the second differential pair are tied to the output signals which establish positive feedback, or hysteresis. Transistors NMOS3-NMOS6 form a current mirror that provides a hysteresis bias current for the second differential pair. Note that device sizes of the second differential pair are kept small, so as to introduce only a little parasitic capacitance to the input differential amplifier. The amount of hysteresis can be programmed by varying this hysteresis current.

The propagation delay in the first and second comparator circuit is calculated as [3]

$$T_{PD} = \frac{T_{PHL}+T_{PLH}}{2} \quad (1)$$

Where T_{PHL} and T_{PLH} are the time difference between 50% of the output and 50% of the input.

In the double tail comparator circuit the propagation delay is calculated as [1]

$$T_{PD} = T_0 + T_{LATCH} \quad (2)$$

The power consumption for all circuits are generated during simulation.

III. SIMULATION RESULT

In order to compare the modified comparator with the existing Double tail comparator all circuits have been simulated in a 0.18 µm CMOS technology with V_{DD} = 1.8v. All simulation are performed using Tanner EDA tool. On the basis of the simulation results a table has been prepared showing all the result inferred from the graphs.

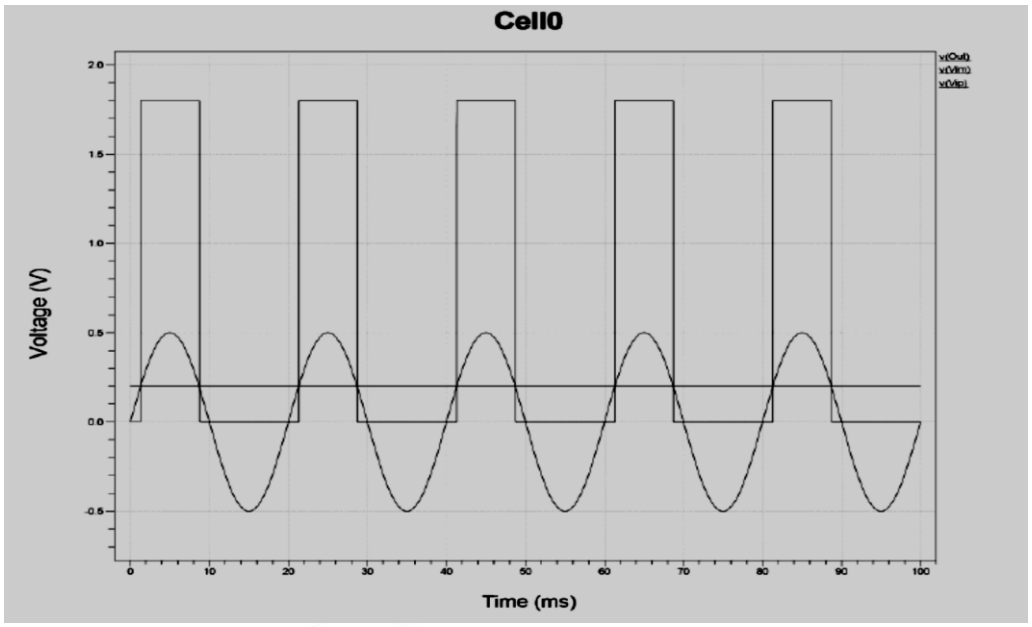

Fig. 5. First comparatort circuit output for sine wave input

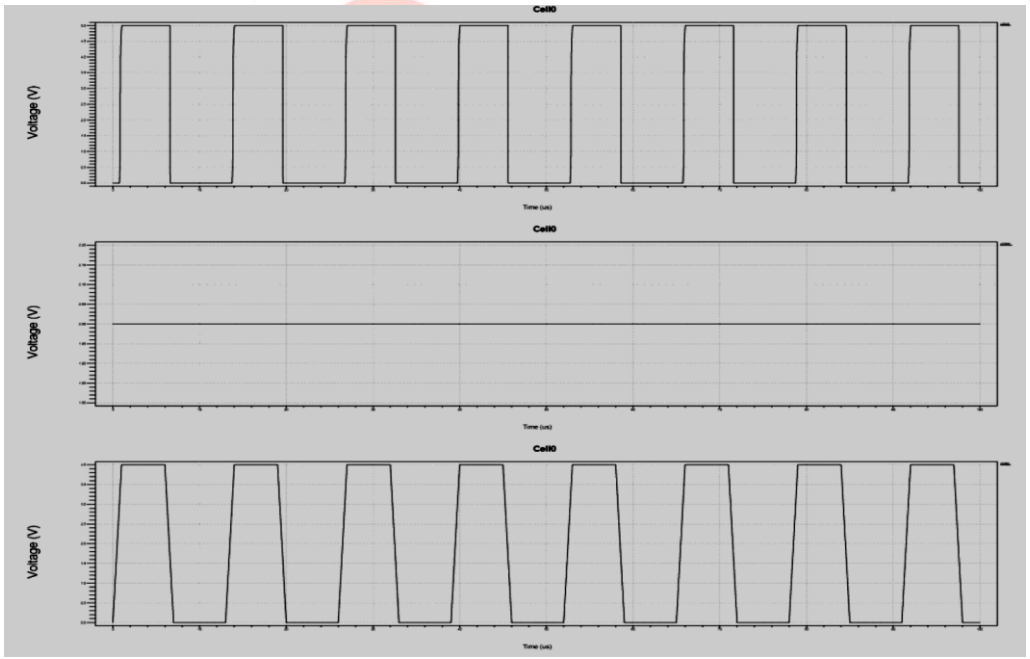

Fig. 6. First comparatort circuit output for pulse wave input

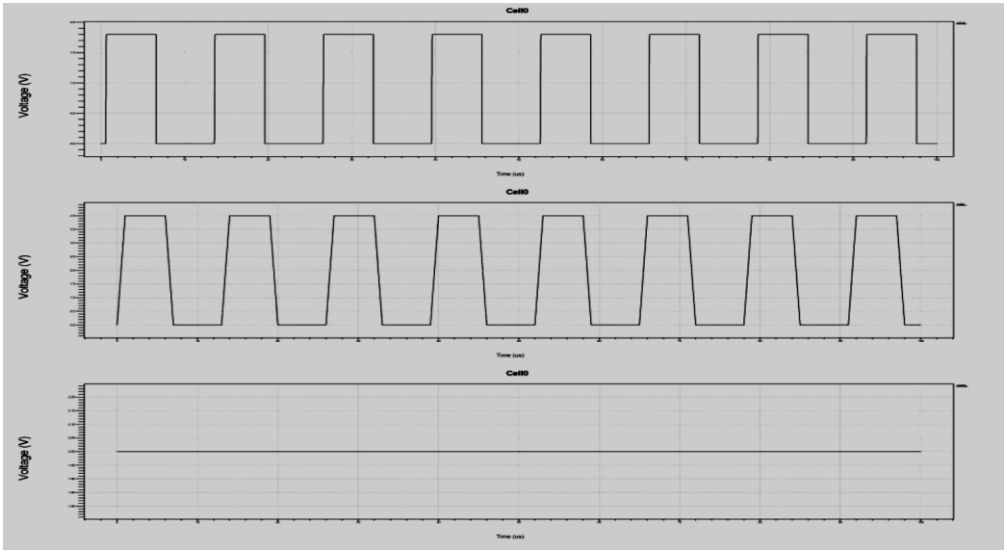

Fig. 7. Second comparator circuit output for pulse wave input.

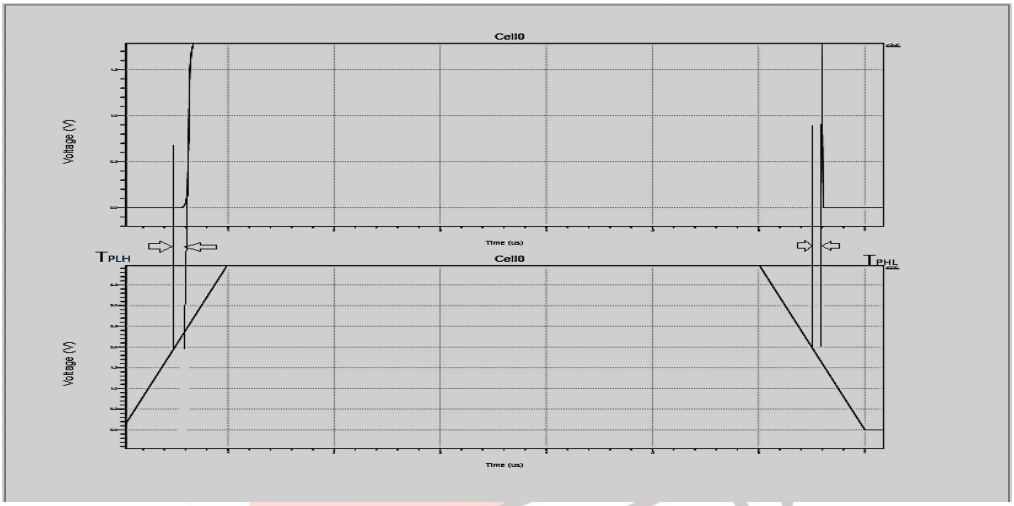

Fig. 8. Calculation of propagation delay for first and second comparator circuit.

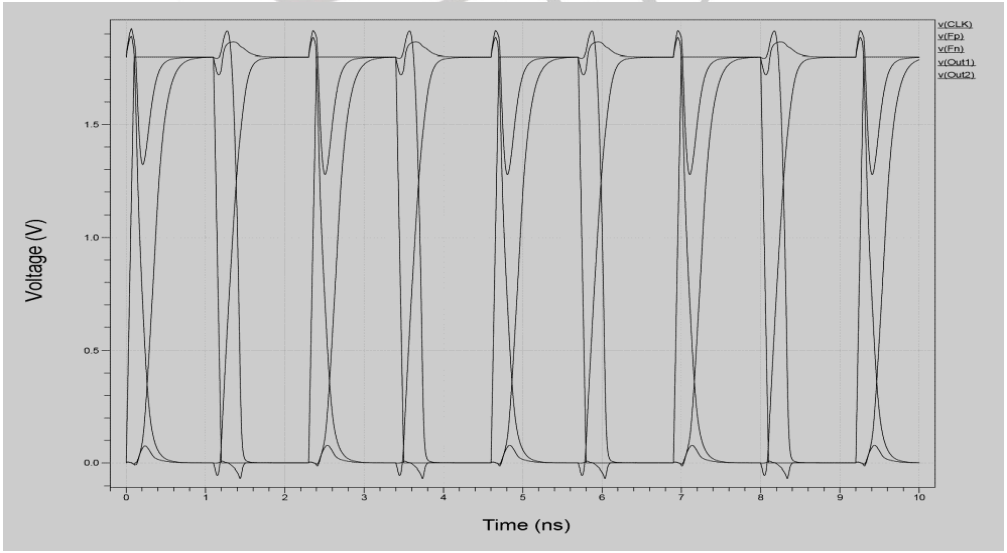

Fig. 9.Transient simulation of Double tail comparator circuit.

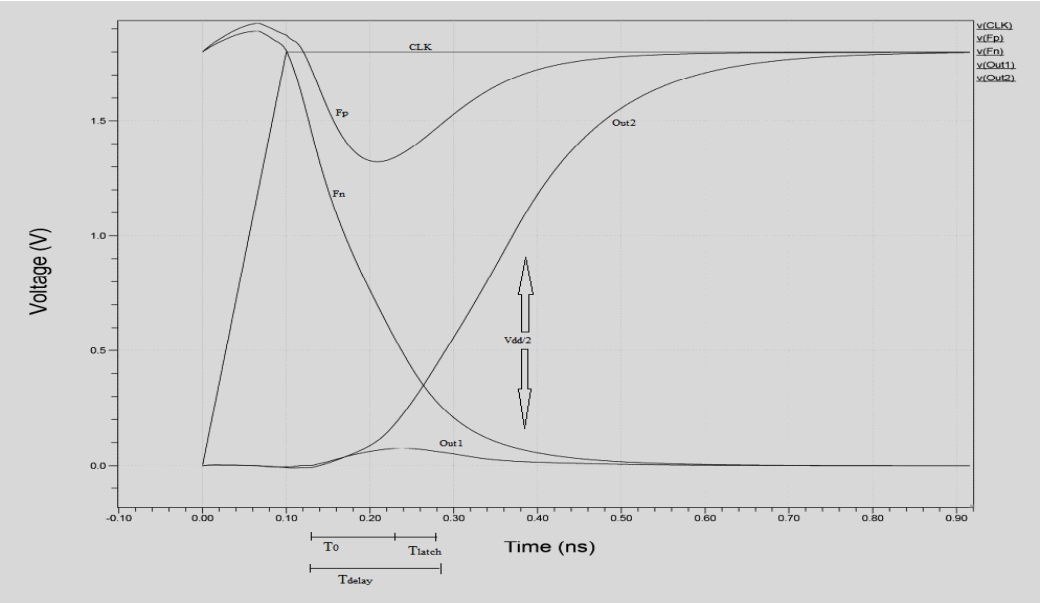

Fig. 10. Calculation of total delay in double tail comparator circuit.

TABLE I Summary of Comparators Performance

	CMOS Comparator without Hysteresis	**CMOS Comparator with Hysteresis**	**Double Tail Comparator**
Technology	180nm	180nm	180nm
Voltage Supply	1.8v	1.8v	1.8v
Propagation Delay(T_{PD})	141ns	190ns	50ns
Average Power Consumption	4.591µw	6.46µw	21.37µw

IV. CONCLUSION

In this paper, we presented two different comparator circuits with their working and simulation result. A table is presented to show values of different parameter obtained during the simulation. Based on theoretical analysis, we designed second comparator circuit in which we successfully reduced the effect of noise in the comparator output. The simulation result obtained shows that comparator circuit with hysteresis consumed one third of the total power consumed by double tail comparator circuit. The Propagation delay result obtained shows double tail comparator faster than comparator circuit with hysteresis. Further research can be done on decreasing the delay for the comparator circuit with hysteresis.

V. REFERENCES

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