L-Band Power Amplifier Design for WCDMA Applications

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Abstract - Mobile communication is one of the important areas and it is developing extremely fast in present times. Nowadays the use of 3G mobile communication systems seem to be the standard, while 4G stands for the next generation of wireless and mobile communications. This paper presents the design and simulation of Power Amplifier (PA) at 1.8 GHz. This PA is designed for WCDMA (Wideband Code Division Multiple Access) applications. This amplifier uses RFMD's FPD3000SOT89EDS which is a high-linearity packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). The key points are analysis device's stability with Stability factor and the input and output impedance matching with Smith Chart and Tuning. Finally, the performance parameters of PA were obtained with the simulation of S parameters. The simulation has been performed using Advanced Design System (ADS) 2011.10 simulation tools.

Keywords - Power Amplifier (PA); ADS tools; PAE; WCDMA; pHEMT

I. INTRODUCTION

Power amplifiers are used in many different applications including the majority of wireless and radio communications equipment, wireless and cable TV broadcast systems, cable and other wired transmission systems, optical driver amplifiers, audio systems and Radars. Depending on the application, frequencies range from audio frequencies to millimeter wave frequencies. Amplifier power ranges from a few milli watts to several mega watts are used for different applications.

In this paper our main focus is on applications for cellular phone handsets and portable wireless devices, with an emphasis on linear power amplification. CDMA, TDMA and OFDM based handsets (or other portable systems) are among these related applications. The carrier frequencies in these applications range from several hundred megahertz to a few gigahertz, while peak powers of 100 milli watts to a few watts are most common. The most well known common objectives in amplifier designs for these applications are: cost and size reduction; efficiency and talk time improvement; and meeting linearity, gain, stability, robustness, reliability and other related requirements. Therefore, while our main focus is linear amplifiers, we briefly stretch further into some nonlinear applications such as GSM handsets to highlight the more general applicability of the techniques.

II. PARAMETER OF POWER AMPLIFIER (PA)

Gain:

The gain of an amplifier is defined as the ratio of its output to input power

$$G = 10log_{10}(\frac{P_{out}}{P_{in}})$$

Where G is the gain of the amplifier in dB, Pout and Pin are output and input powers in W respectively. When a relative small input power is injected into a PA, the gain of the amplifier is independent of the input signal level. On the contrary, the gain of an amplifier drops when a relative large input power is injected because of nonlinearities in the amplifier.

Transducer Power Gain: It is the ratio of the power delivered to the load to the power available from the source. This depends on both ZS and ZL.

$$G_t = \frac{1 - |\Gamma_s|^2}{|1 - s_{11}\Gamma|^2} |s_{21}|^2 * \frac{1 - |\Gamma_L|^2}{|1 - s_{22}\Gamma|^2}$$

1 dB compression point: At low-level input signals, an amplifier has a constant gain and linear behavior. However, as the input levels increases, amplifier gets saturated and the output signal will no longer increase proportionally with the input signal. The input power level where the amplifier has a 1 dB less linear gain due to saturation is defined as 1 dB compression point and it is considered as an important parameter for the linearity of a PA.

Efficiency: Another important factor in a power amplifier is the efficiency. Drain efficiency is defined as the ratio between output power and the injected DC power

$$\eta = \frac{P_{out}}{P_{dc}},$$

Where Pout is the output power of the amplifier and Pdc is the DC power consumption of the amplifier. The other definition to characterize the power conversion efficiency is Power Added Efficiency (PAE). It is the ratio of difference between output and input power to the DC power consumption

$$\label{eq:pae} \text{PAE} = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out}}{P_{dc}} (1 - \frac{1}{G}),$$

Where Pout is the output power, Pin is the input power, Pdc is the DC power consumption and G is the gain of the amplifier.

POWER AMPLIFIER DESIGN STEPS

1. Selection of Transistor

III.

FPD3000SOT89EDS	
Output Power (P1dB)	30dBm
Small-Signal Gain	13dB
OIP3	43dB
Noise Figure	0.9
Power-Added efficiency	45%
$ m V_{DS}$	5v
$\mathbf{I_{DS}}$	150mA

2. Stability analysis

Amplifier is not reliable when it is instable condition. The stability of a circuit is characterized by stern stability factor. The circuit is stable only when K>1 and $\Delta<1$. When the input and output reflection coefficients are less than one then we determined the absolute stability factor:

When K<1, then Smith chart is stable but when the K<0, then the Smith chart is unstable.

$$K = \frac{1 + \Delta^2 - S_{11}^2 - S_{22}^2}{2S_{11}S_{22}}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

S_{22}	0.595∠161.9
S ₁₁	0.823∠167.8
S_{12}	0 .054∠34.5
S_{21}	3.808∠62.6

Table: 01

After calculation find $\Delta = 0.6359$ and k=0.9069.

So, transistor is unstable. To stabilize the transistor use the smith chart matching circuit. For this matching plot a load and source circle in smith chart. Radius and Center of circle is find by equations,

For Load,

$$C_L = \frac{(S_{22} - \Delta S_{11^*})^*}{|S_{22}|^2 - |\Delta|^2} \quad r_L = \frac{|S_{12}S_{21}|}{|S_{22}|^2 - |\Delta|^2}$$

For Source,

$$C_S = \frac{(S_{11} - \Delta S_{22^*})^*}{|S_{11}|^2 - |\Delta|^2} \quad r_S = \frac{|S_{12}S_{21}|}{|S_{11}|^2 - |\Delta|^2}$$

Transistor is unconditionally stable when this circle is completely outside the smith chart.

3. Input and Output matching

The input matching network is used to make the input return loss (S11) minimized without introducing additional noise. The input matching circuit that terminates the transistor to gamma optimum (Γ out) which represents the input impedance of the transistor for the best noise matches. Attenuation is lowest at 77 Ω and power handling capability is highest at 30 Ω . So, the compromise between these two parameters gives the 50 Ω resistive input impedance to design PA. The next step in PA design

involves output matching. The input and output impedance matching is required to maximize the power transfer and minimize the reflections. Smith chart is used for impedance matching. According to maximum power transfer theorem, maximum power delivered to the load when the impedance of load is equal to the complex conjugate of the impedance of source $(ZS = ZL^*)$.

4. Simulation Circuit & Results

By using advance design system (ADS) software design a power amplifier circuit. The Semitic diagram is show in figure. Simulation results of PA are shown in Figure. The designed power amplifier offers forward gain $(S_{21}) = 14.25$ dB at 1.8 GHz and Input return loss $(S_{11}) = -27.073$ dB and Output return loss $(S_{22}) = -26.378$ dB at 1.8 GHz which are shown in Fig. The Stability Factor K is greater than 1 for 1 GHz to 2 GHz which indicates that PA is unconditionally stable in this frequency range.

Parameters	Frequency(1.8 GHz)
S_{21}	14.25 dB
S ₁₁	-27.073 dB
S_{22}	-26.378 dB
Stability Factor K	1.510
VSWR	1.093

Table: 02

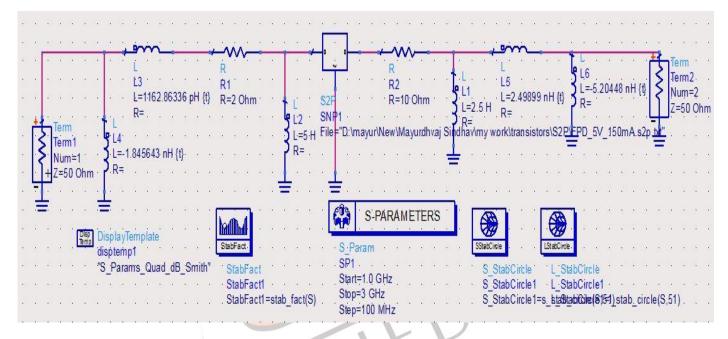


Figure 1: Power Amplifier Circuit

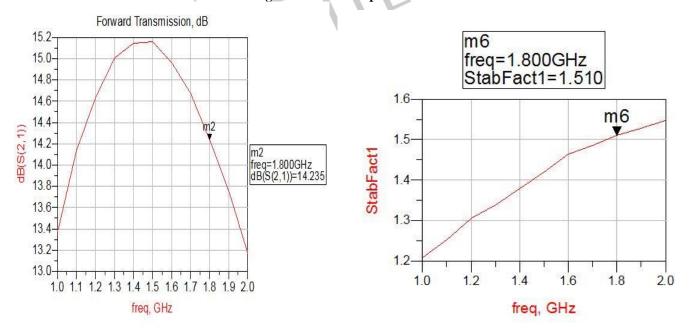
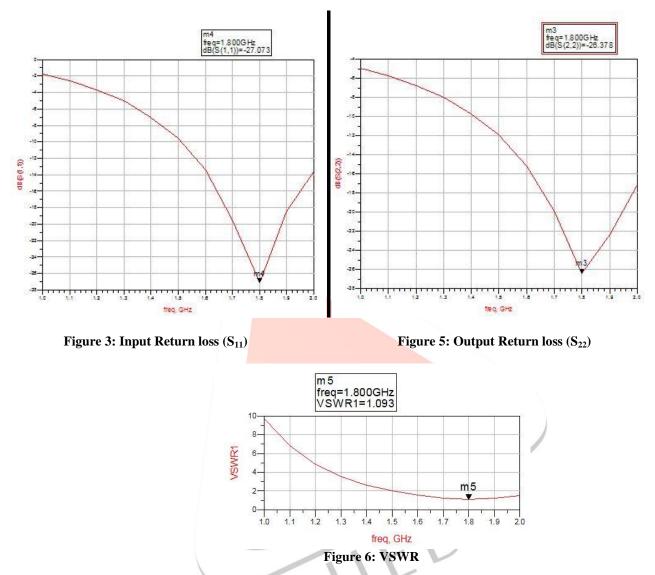


Figure 2: Forward Gain (S₂₁)

Figure 4: Stability Factor K



IV. CONCLUSION

In this paper Power amplifier circuit has been designed and simulated for 1.8 GHz. Simulation results are obtained using Advanced Design system (ADS) Software. The parameters like forward gain (S21), return loss, stability factor has been optimized. Improvements to the power amplifier performance are being addressed. To further improve the efficiency of the amplifier, harmonic traps will be added at the output to reduce the harmonics of the fundamental frequency and to prevent the undesired harmonics from delivering to the load.

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