Physical Design and Simulation of an n stage Ring Oscillator using, 300 nm Technology

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***Abstract*— Voltage controlled Oscillators or Ring Oscillators are crucial components in any timing and memory circuits. The goal of this paper is to do physical design for a high speed, low power consumption multistage high performance ring oscillator circuit based on 300 nm CMOS technology which provides frequency of high order (KHz). This oscillator is used for high speed wireless communication applications and in control circuitries of numerous analog and digital integrated circuits. This ring oscillator is designed to be controlled in a oscillation frequency by a voltage input. The physical design will include C5 process, simultaneously various design rule check and network consistency checks were performed to improve performance characteristics of the oscillator. The Complementary-Metal-Oxide-Semiconductor (CMOS) is the most popular technology for the modern integrated circuit design and fabrication. Based on this technology, a VCO can be implemented by the LC resonant or Ring structure. In this paper a ring based VCO is design which has small chip area, low power consumption which is suitable for wide tuning band VCO of namely 11 stages, 21 stages and 51 stages. The paper will also focus on various design considerations namely basic cell design, bias circuitry and design implementation and testing of the same.**

***Index Terms*— Voltage controlled Oscillators, Inverter, CMOS Technology, Physical Design, Spice, DRC, LVS**

I INTRODUCTION

Electrical oscillators are used in all kinds of electronic systems. Oscillators that will be discussed in this paper will find its application in synchronization of control logic with various analog and digital integrated circuits. Oscillatory behavior is ubiquitous in all physical systems specially in memory and mixed signal integrated circuits, in frequency and communication systems. Oscillators are the prime requirements of circuits needing time references and also to synchronize operations. An ideal oscillator would provide perfect time reference i.e. a perfect periodic signal [1], but oscillators are corrupted by undesired noise.
A variety of Oscillators are available but the principle of operation, the frequency of oscillation, their fabrication with respect to different CMOS logics relative, process technologies and their performance in noisy environment is different from one class of oscillators to other.

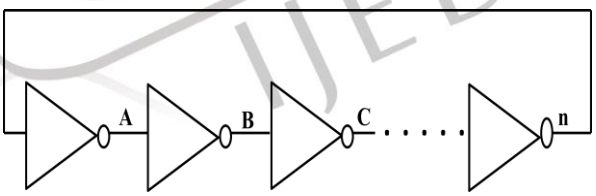

Fig.1 Ring Oscillator realization with n digital inverters

This ring oscillator is designed to be controlled in a oscillation frequency by a voltage input. The physical design of the very same will include C5 process, 300 nm process technology simultaneously various design rule checks and network consistency checks were performed. CMOS inverter ring oscillators offer numerous advantages like tuning ranges, signal swing and a small chip area.

II BARKHAUSEN CRITERIA

The Barkhausen criterion is used to determine the oscillation startup condition. The Barkhausen stability criterion is necessary but not sufficient for oscillation[4].

$$|H(j\omega)| \geq 1 \qquad \text{(i)}$$

$$\angle |H(j\omega)| = \pi \qquad \text{(ii)}$$

The criteria for oscillation is not well understood, there is no known sufficient criteria for oscillation. If considering the unity gain negative feedback which is as shown below, where

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)} \qquad \text{(iii)}$$

Them the circuit may oscillate at ω if the conditions (i) and (ii) are met called the Barkhausen criterion.

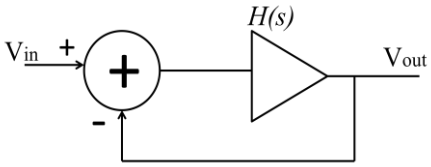

Fig. 2 Generalized Feedback System[6]

III PHYSICAL DESIGN OF INTEGRATED CIRCUITS

The process of creating an accurate physical representation of an engineering drawing (netlist) that conforms to constraints imposed by the manufacturing process, the design flow, and the performance requirements shown to be feasible by simulation. Today, layout design is carried out in an environment that is ever changing with corresponding processing technology. The software tools and methodologies, computing platforms, the EDA companies providing these tools, the applications that are being implemented, and the market pressures IC are all changing year by year. These changes make this industry an interesting one in which to be involved. However, the fundamental concepts behind producing quality layout are based on physical and electrical properties that never change [7].

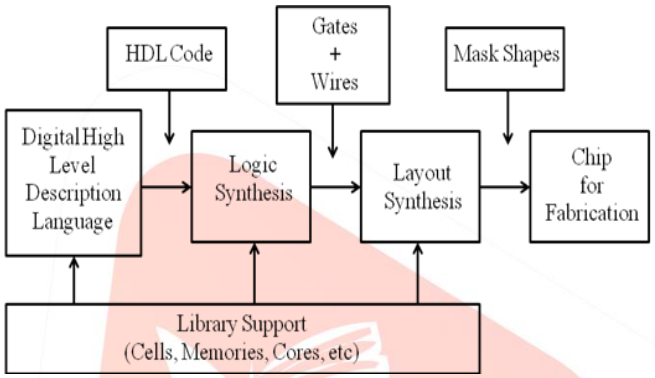

Fig. 3 Co evolution of EDA tools and Methodology [26]

Limitations and Challenges to be overcome[11]

In this section, various established and emerging design quality metrics and the main challenges of CAD tools to effectively predict, analyze their interactions, and optimize them in the CMOS technology were discussed. In the last few years, the research developers have witnessed increasing levels of interactions between physical, logical, and functional realms in the synthesis of VLSI circuit and systems. Various approaches with varying levels of interactions between the synthesis and layout phases have been proposed. These techniques are classified into several classes:

A. Gain-Based Synthesis: It is based on logical effort theory, which performs the gate sizing based on logical effort, electrical effort and timing constraints. The succeeding layout phase, is then performed with additional timing and capacitance constraints to meet the initial gate sizing decision. Appropriate circuit libraries are must.

B. Layout-Friendly Synthesis: Here, Synthesis of layout implications is given more importance. The wire planning is a best example for this type of synthesis. The research developers use the placement of I/O pins to achieve a layout-friendly logic factorization.

C. Layout-Driven Synthesis: In this synthesis depends on companion, layout/placement of various parts of the logic. After synthesis nodes may get created or deleted, and the companion layout may need to be updated to reflect these changes. The benefit of having a companion layout view is access to a more realistic estimates about the interconnect parasitics. This would allow the synthesis phase to make better decisions, while optimizing the logic.

D. Integrated Synthesis and Layout: **T**he ultimate integration of the synthesis and layout phases were carried out by this class.

E. Synthesis-Driven Layout: This category consists of those techniques which perform layout optimization moves either within the synthesis phase or in a post-layout phase where synthesis and layout optimizations are applied to improve the design or meet the performance constraints.

F. Synthesis-Friendly Layout: This type of synthesis consists of layout synthesis algorithms and environments which is capable of withstanding functional and logic changes, with minimal disruption to the layout.

IVRING OSCILLATOR

Ring Oscillator is a cascaded combination of odd number of inverters arranged serially, also connected in a closed loop negative feedback configuration. It is realized by connecting an odd number of open loop inverting amplifiers in a feedback loop[1]. Here simple CMOS inverter is used as an amplifier. A logic change will gradually appear after every stage and henceforth the signal will propagate around the loop with an inversion. The change will propagate through all the stages (in this paper preferably 11,21 and 51 stages). Assuming each Inverter has a delay of τ seconds and there are N inverters , the frequency of oscillation can be calculated by

$$\frac{T}{2} = n\tau \qquad \text{(iv)}$$

$$f_{oscillation} = \frac{1}{2\,n\,\tau} \qquad \text{(v)}$$

Generally the performance of ring oscillators is better than other oscillators although not as good as that of the sinusoidal oscillators. But the continuous up gradation of processing technology has yielded in improving the performance of ring oscillator so as to attain a good level of satisfaction which can now be used successfully in clocking and synchronization of mixed signal integrated circuits. The level of optimization has been achieved in both cases: speed of operation and noise performance.

V CMOS INVERTER

CMOS Inverter is a basic building block for any digital and analog integrated circuit design. This is the simplest logic gate which implements the logic operation of negation. A CMOS inverter is a circuit which is built from a pair of nMOS and pMOS transistors operating as complementary switches as shown

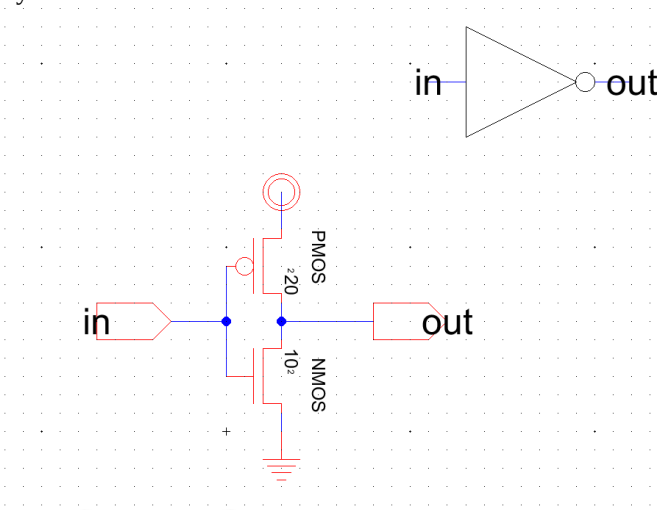

Fig.4 Schematic and Icon view for CMOS Inverter

The main advantage of a CMOS inverter over many other solutions is that it is built exclusively out of transistors operating as switches without any other passive elements like resistors and capacitors.

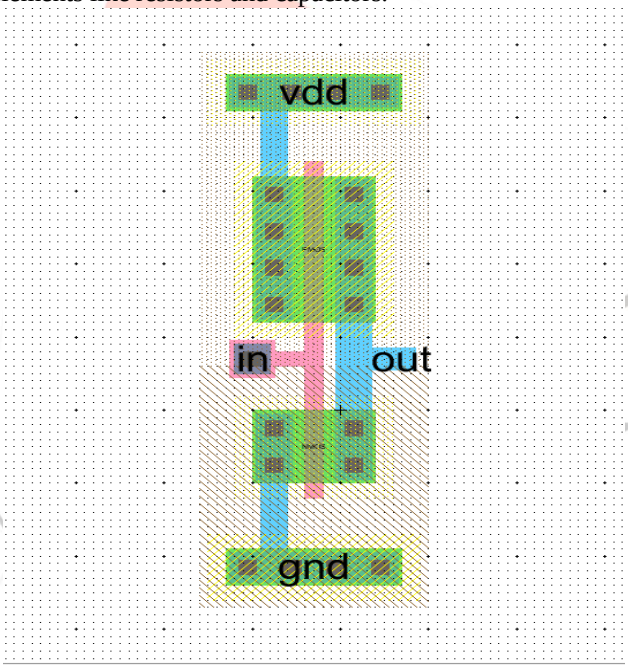

Fig.5 view for CMOS Inverter

The principle of operation is as follows:[6]

1) For small values of the input voltage, VIN, the nMOS transistor is switched off, whereas the pull-up pMOS transistor is switched on and connects the output mode to VDD

2) For large values of the input voltage, VIN, the pMOS transistor is switched off, whereas the pull-down nMOS transistor is switched on and connects the output mode to GND = 0V.

DC characteristics are as plotted

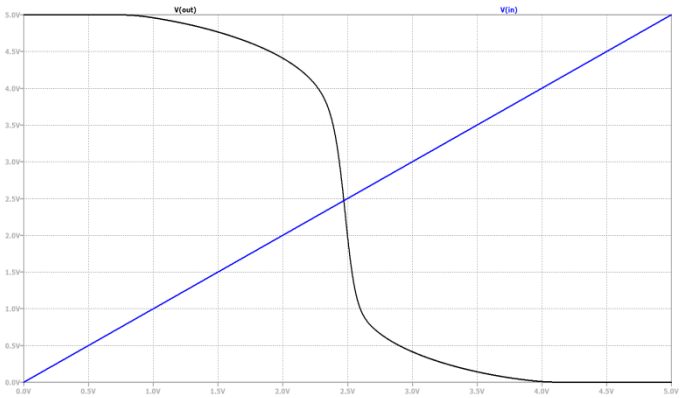

Fig.6 DC Characteristics of CMOS Inverter

VIDESIGN OF SCHEMATIC AND LAYOUT OF OSCILLATOR

In this paper we represent a ring oscillator with 11 stages, 21 stages and 51 stages with CMOS inverters in 300nm C5 process technology. The Schematic includes PMOS transistors of width = 20 units and length 10 units. For the layout we chose these transistors with respect to schematic. For connections we use Metal 1, Metal 2 and Metal 3 different ways.
The individual CMOS inverters are cascaded serially maintaining all DRCs.

VIIESTIMATION OF OSCILLATION FREQUENCY

A perfect oscillator would have localized tones at discrete frequencies i.e. harmonics. The approach for calculating oscillation frequency is very conventional but effective. The total time period or time difference of oscillation is calculated from simulation graphs. By taking the inverse of it, the oscillation frequency can be easily estimated.

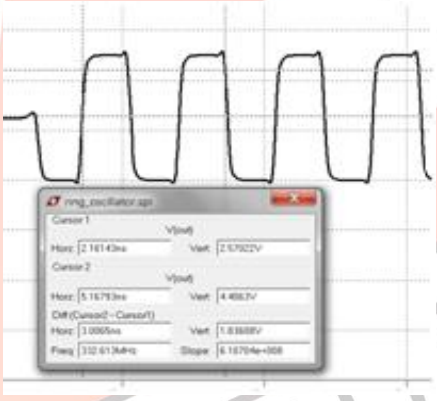

Fig.7 Frequency estimation using difference method

VII. Design and Simulation Results

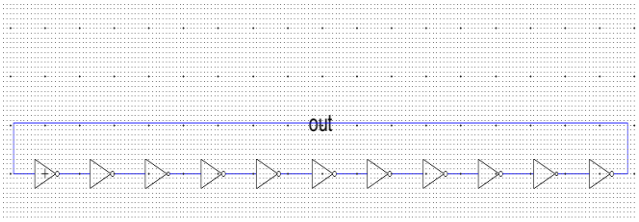

Fig.8 Schematic of 11 stage Ring Oscillator

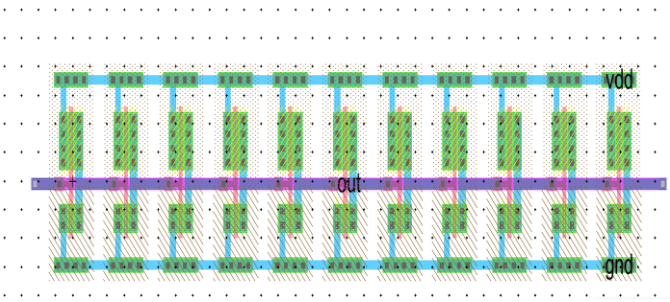

Fig.9 Layout of 11 stage Ring Oscillator

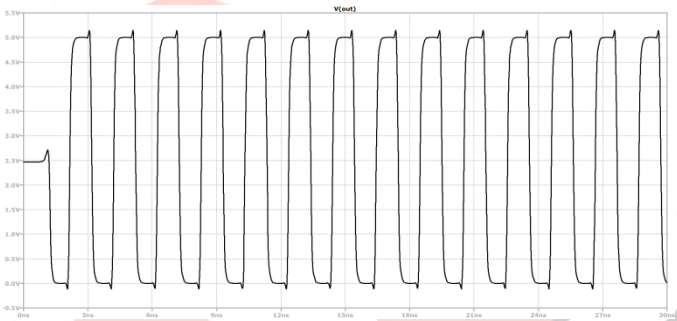

Fig.10 Transient plot for 11 stage Ring Oscillator

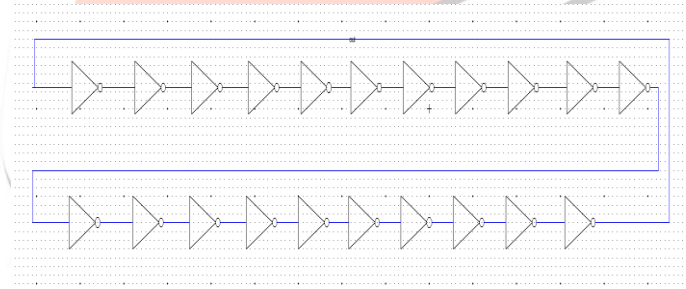

Fig.11 Schematic of 21 stage Ring Oscillator

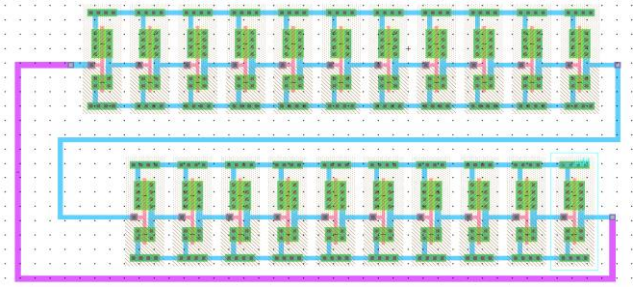

Fig.12 Layout of 21 stage Ring Oscillator

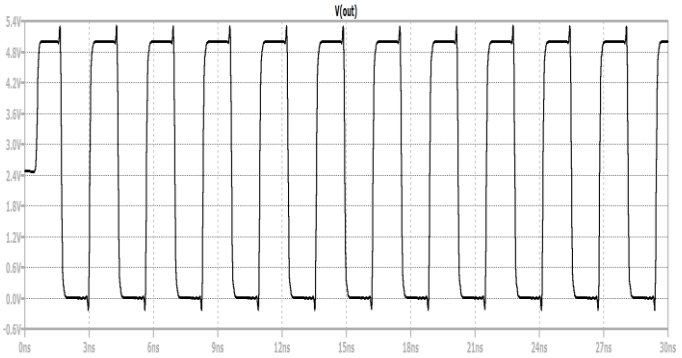

Fig.13 Simulation plot for 21 stage Ring Oscillator

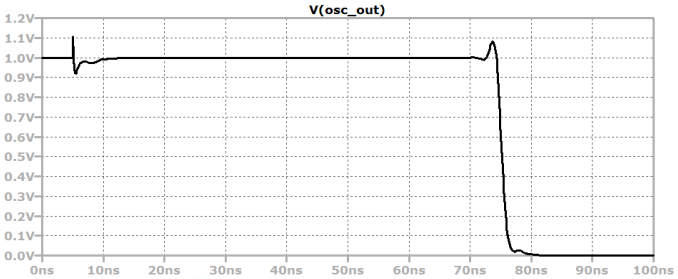

Fig.14 Simulation plot for 51 stage Ring Oscillator (Transient 30 n)

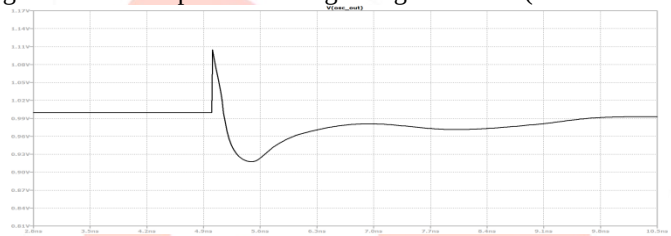

Fig.15 Simulation plot for 51 stage Ring Oscillator (Transient 100n)

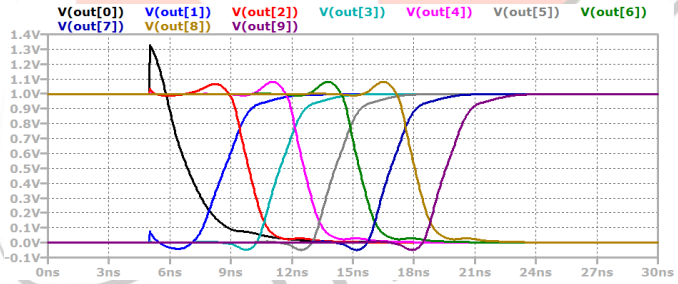

Fig.16 Simulation plot for 51 stage Ring Oscillator
(Output of first 10 stages)

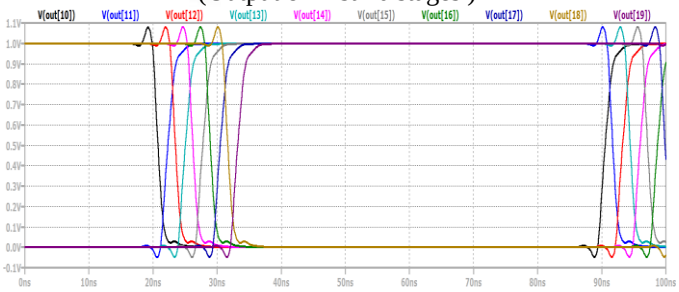

Fig.17 Simulation plot for 51 stage Ring Oscillator
(Output of 10-20th stages)

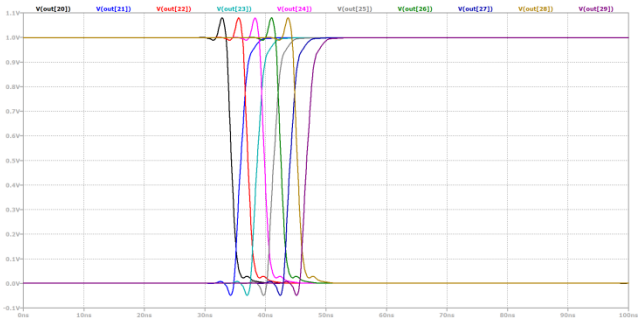

Fig.18 Simulation plot for 51 stage Ring Oscillator
(Output of 20-30th stages)

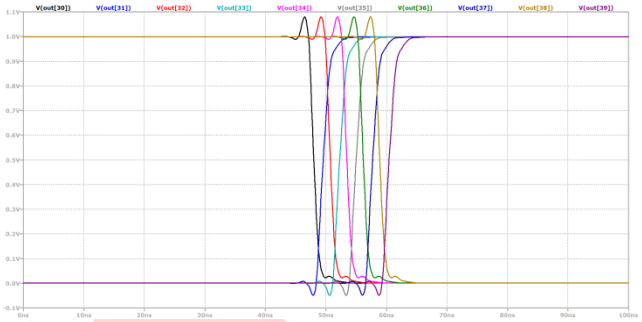

Fig.19 Simulation plot for 51 stage Ring Oscillator
(Output of 30-40th stages)

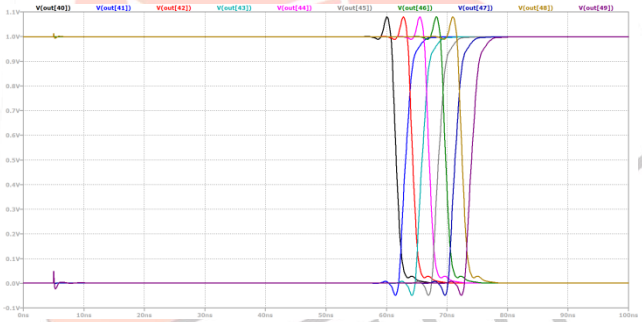

Fig.20 Simulation plot for 51 stage Ring Oscillator
(Output of 40-50th stages)

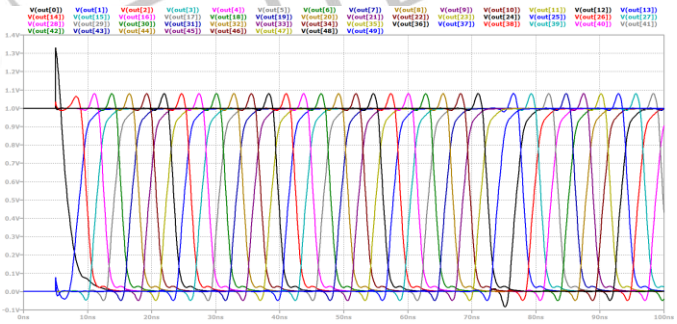

Fig.21 Simulation plot for 51 stage Ring Oscillator
(Output of individual 51 stages)

VIII VLSI CAD TOOLS VS METHODOLOGIES

As we make progress in design technology, there is a ongoing debate within the design technology community about the importance of new algorithms and tools or new methodologies and associated tool flows.

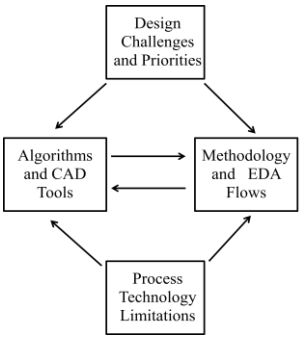

Fig.22 VLSI CAD/EDA vs CMOS Design Methodologies [1]

The simple fact is that history of design for microelectronic systems includes the going of both of them hand in hand to get the maximum benefit and in act these two aspects of the design technology are tightly coupled and correlated in terms of their impact. VLSI Design incorporates both the design methodologies and associated CAD tools because both forms the integral parts and should go hand in hand as they evolve based on the designer's needs.

IX Conclusion

This paper presents design aspects for layout and simulation of a ring oscillator with CMOS inverters. The schematic and layouts are designed for the ring oscillator with 11,21 and 51 inverter stages in 300 nm , C5 process technology. The corresponding frequency of oscillation can also be estimated from simulations. Design rule check and network consistency check is also satisfied for individual oscillators.

Acknowledgements

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