CMOS Full Adder for Energy Efficient Arithmetic Applications

[1] Mr. Kiran R. Barapatre, [2] Mr.Mayur B. Petkar, [3] Ms.Asmita R. Padole
Lecturer
Electronics Engineering, DBACER, Nagpur, India
[1]barapatre.kiran@gmail.com, [2] mayur_petkar@yahoo.com , 3vaidehidhopte@gmail.com

***Abstract*—In this paper, we present Energy efficient CMOS full adder, which is one of the basic building blocks of a modern electronic systems design. Energy-Efficiency is one of the most required features in digital electronic systems for high-performance and/or portable applications which signify PDP, it measures the energy consumed per switching event. This paper shows that complementary CMOS is the logic style of choice for the implementation of combinational circuits, if low voltage, low power, and small power-delay products are of concern with relatively low area.**

***Keywords*- Adders, CMOS Full Adder, Low power, VLSI, High-Speed, Low-area.**

I. INTRODUCTION

In the today's world of VLSI system such as application specific DSP architectures, microprocessors, FIR filter and systolic array design there is requirement of fundamental operations such as addition. Thus Full adders are the core of many arithmetic operations such as addition, subtraction, multiplication, division and address generation. In the majority of systems, the adder is part of the critical path that determines the overall performance of the system. As stated, the system's overall performance would affected by PDP exhibited by the full-adder [1]. Hence enhancing the performance of the full adder cell results of great interest [1].By considering this facts the design of a full-adder having low-power consumption and low propagation delay results of great interest for the implementation of modern digital systems.

In advancement of mobile product, which worked with a high throughput capability makes the design of low-power adder module another significant goal to be achieved. Power dissipation can be cause by three major components in complementary metal oxide semiconductor (CMOS) circuits [2] namely switching power, short circuit power and static power. Reducing any of these components will accounts for lower power consumption for the whole system design.

II. PREVIOUS WORK

Various papers have been published related to the design of low power full adders. They were trying on both, the logic style and the logic structure used to build the adder. Since the standard CMOS realization [3], various full adders were built upon different static logic styles. They have been presented, namely: Differential Cascade Voltage Switch (DCVS) [4], Complementary Pass-Transistor Logic (CPL) [5], Double Pass-Transistor Logic (DPL) [6], and Swing Restored CPL (SR-CPL) [7]. Depending On these logic styles, few tasks have been done to build advance full adders by changing the internal logic structure of the adder module. In recent work [8], a full adder is designed by using transmission function theory. It is formed by three main logic blocks namely XOR-XNOR gate to obtain A XOR B and A XNOR B signals (Block 1), and a multiplexers to obtain the SUM (So) and CARRY (Co) outputs (Blocks 2 and 3) respectively , as shown in Figure 1.

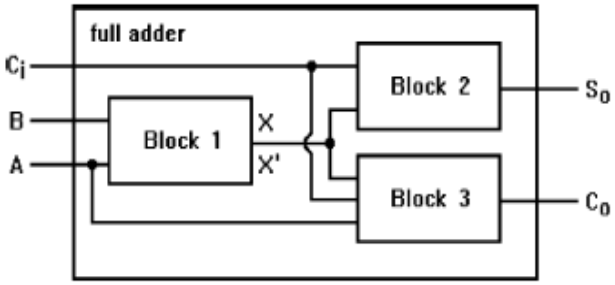


Fig 1: Full-adder cell using three main logical blocks.

The specified logic structure is based on the full adder's truth-table shown in Table 1, and it has been accepted as the standard internal structure in the most of the field area developed for the single bit full adder cell.

TABLE 1- TRUE-TABLE FOR A 1-BIT FULL ADDER WITH A, B AND C AS AN INPUTS, AND SO AND CO ARE OUTPUTS.

C	B	A	So	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

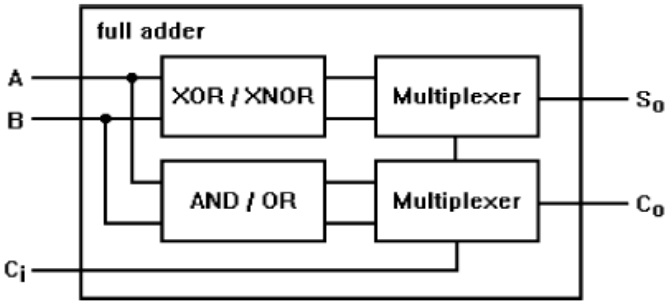
In paper [9], detail study is done on one bit cmos full adder, the efficient realization for block 1 in fig 1 was implemented with SR-CPL logic style. But there is an important conclusion was pointed out regards of propagation delay. For a full adder built upon the logic structure shown in Figure 1. It is essential to obtain A XOR B and A XNOR B internal signals, which are then feed to drive other blocks which are block1 and block 2 in order to generate the final outputs. Thus the overall power consumption, depend on the delay and voltage swing of the (A XOR B) and (A XNOR B) signals, generated within the module.

Thus, to increase the operational speed of the full adder, it is essential to research for a advance logic structure that avoids the generation of internal signals used to control the selection or transmission of other signals located on the critical path.

III. ENERGY EFFICIENT FULL ADDER

After studying the truth table of full adder in Table 1, it can be observed that the So output is equal to the (A XOR B) value when C=0, and equal to (A XNOR B) when C=1. From this observation we conclude that a multiplexer will be used to obtain the respective value based upon the Carry input, as stated earlier. Using the same scenario, the Co output is equal to the (A AND B) value when C=0, and (A OR B) value when C=1. In the similar way, carry will be used to drive a multiplexer. Hence, an energy efficient logic scheme to design a full adder cell can be formed by a logic block to get the (AXOR B) and (AXOR B) signals, other block to obtain (A AND B) and (A OR B) signals, and two multiplexers being driven by the Carry input to generate the So and Co outputs, as shown in Figure 2.

Fig 2: Alternative logic scheme for Energy Efficient Full Adder



The features and advantages that can be expected for this energy efficient logic structure are given below [10],

1. There is no requirement of internal signal for controlling the select line of multiplexers. Instead, the Carry input signal, which has full voltage swing and without delay, is used to drive the select line of multiplexers, which reduces the overall propagation delay of full adder.
2. It reduces the capacitive load for the carry input, because it is connected only to some transistor gates and not to some drain or source terminals, where the diffusion capacitance is becoming very large. Hence, the overall delay for larger modules where the carry signal falls on the critical path can be reduced.
3. The propagation delay can be tuned up individually by adjusting the XOR/XNOR and the AND/OR gates for the So and Co outputs; this criteria is advantageous for applications where the skew between arriving signals is critical for a proper operation (e.g., wave pipelining).
4. By interchanging the XOR/XNOR signals, and the AND/OR gates to NAND/NOR gates at the input of the multiplexers, the placement of buffers at the full-adder outputs can be implemented which can improve the performance for load-sensitive applications.

Depending on the results obtained in [11], two new full-adders will be been designed using the logic styles DPL and SR-CPL. Fig. 3 presents a full-adder designed using a DPL logic style to build the XOR/XNOR gates, and a pass-transistor based multiplexer to obtain the So output.

In Fig. 4 presents the SR-CPL logic Style which will be used to build XOR/XNOR gates. AND/OR gates have been built using a powerless and groundless pass-transistor configuration, respectively in both cases and a pass-transistor based multiplexer to get the Co output.

Fig 3: Full-adder designed with the Energy Efficient structure using a DPL logic style

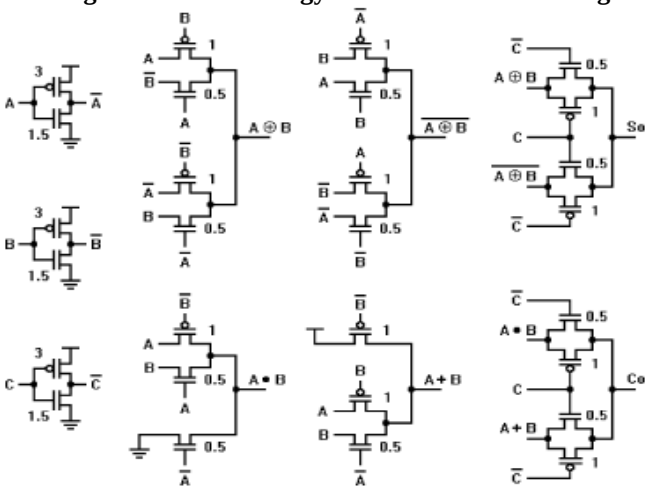
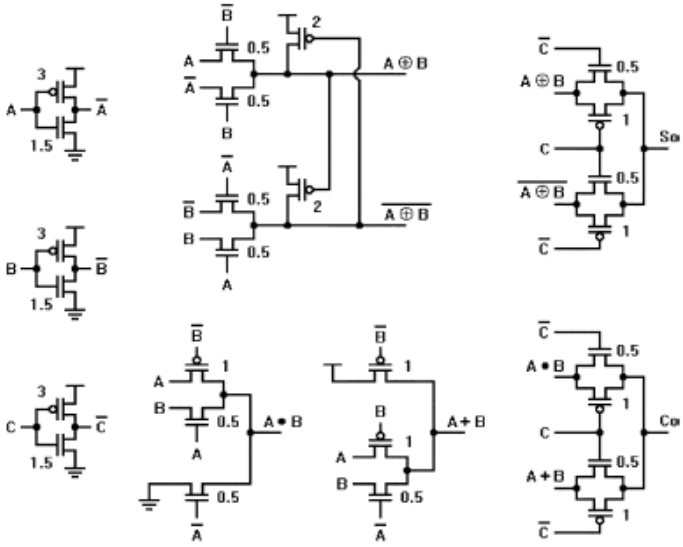


Fig 4: Full-adder designed with the Energy Efficient structure using a SR-CPL logic style



IV. COMPARISON OF DIFFERENT LOGIC STYLE

The logic style used in logic gates basically depends on the speed, size, power dissipation, and the wiring complexity of a circuit. Depending on these criteria comparison of different logic style is listed below [12]

Table 2- Qualitative Logic Style Comparisons

Table 1: Gate comparisons.

cell type	logic style	delay (ns)	power (μW)	PT (norm.)	# trans.	cell type	logic style	delay (ns)	power (μW)	PT (norm.)	# trans.
FA	CMOS	1.94	65	1.00	28	AOI/OAI	CMOS	1.17	41	1.00	6
	CMOS [1]	1.96	78	1.20	40		CPL	1.12	80	1.89	14
	TGATE [2]	1.85	82	1.20	24		SRPL	4.48	108	10.21	12
	CPL	1.17	97	0.90	32	MUX2	CMOS	0.93	46	1.00	8
	DPL	2.03	119	1.91	48		CPL	1.24	57	1.66	10
	WANG [3]	1.68	81	1.08	25	MUX4	CMOS	1.39	62	1.00	18
NAND2	CMOS	0.67	37	1.00	4		CPL	1.55	66	1.19	18
	CPL	1.17	65	3.09	10	XOR2	CMOS	1.27	38	1.00	8
AND4	CMOS	1.09	44	1.00	12		CPL	1.29	59	1.58	10
	CPL	1.48	98	3.02	18		WANG [3]	1.27	51	1.33	6

V. CONCLUSION

The design of high-speed low-power full adder cells based upon an alternative logic approach has been presented. Which results in a great improvement on regards of power-delay metric for the proposed adders, when compared with several previously published realizations.

The full adders designed using improved logic structure and DPL and SR-CPL logic styles, less delay of around 720ps and less power consumption of around 840 µW, for an overall reduction of 30% respect to the best featured one of the other adders been compared, but in general about 50% respect to the other ones.

In the future some work can be done for the designing of high-speed low-power full adders, considering alternative logic structure and trying on new realizations for the constituent logic blocks (XOR/XNOR, AND, OR and MUX cells).

REFERENCES

[1] A. M. Shams and M. Bayoumi, "Performance evaluation of 1-bit CMOS adder cells ", IEEE ISCAS, Orlando, Florida, May 1999, pp. I27 -130.

[2] A.P.Chandrakasan, S.Sheng and R.W.Brodersen, "Lowpower CMOS digital design ", IEEE JSSC, Vol. 27, April 1992, pp. 473-483.

[3] N. Weste and K. Eshraghian, Principles of CMOS design, A system perspective, Addison-Wesley, 1988.

[4] K. M. Chu and D. Pulfrey, "A comparison of CMOS circuit techniques: Differential cascode voltage switch logic versus conventional logic, "*IEEE J. Solid-State Circuits*, vol. SC-22, no. 4, pp.528–532, Aug.1987.

[5] K. Yano, K. Yano, T. Yamanaka, T. Nishida, M. Saito, K. Shimohigashi, and A. Shimizu, "A 3.8 ns CMOS 16□16-b multiplier using complementary pass-transistor logic," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 388–395, Apr. 1990.

[6] M. Suzuki, M. Suzuki, N. Ohkubo, T. Shinbo, T. Yamanaka, A. Shimizu, K. Sasaki, and Y. Nakagome, "A 1.5 ns 32-b CMOS ALU in double pass-transistor logic," IEEE J. Solid-State Circuits, vol. 28, no. 11, pp. 1145–1150, Nov. 1993.

[7] R. Zimmerman and W. Fichtner, "Low-power logic styles: CMOS Versus pass-transistor logic," IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[8] N. Zhuang and H. Wu, "A new design ofthe CMOSfull adder", IEEE JSSC, Vol. 27, No. 5, May 1992, pp. 840-844

[9] A. M. Shams and M. Bayoumi, "A new cellfor low power adders ", Proceedings of the International MWSCAS, 1995.

[10] C. Chang, J. Gu, and M. Zhang, "A reviewof 0.18-□mfull adder performances for tree structured arithmetic circuits," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13, no. 6, pp. 686–695, Jun. 2005.

[11] M. Aguirre and M. Linares, "An alternative logic approach to implement high-speed low-power full adder cells," in Proc. SBCCI, Florianopolis, Brazil, Sep. 2005, pp. 166–171.

[12] Reto Zimmermann and Wolfgang Fichtner, Fellow, IEEE" Low-Power Logic Styles: CMOS Versus Pass-Transistor Logic" in IEEE Journal Of Solid-State Circuits, Vol. 32, No. 7, July 1997.