# Design and Simulation of Quaternary Logic Gates

Dhara Anil Pandya

PG Student Electronics and Communication Engineering Department L. J. Institute of Engineering, Gujarat Technological University, Ahmedabad, Gujarat dpandya9488@gmail.com

*Abstract*—Multiple-valued logic circuits have received an increased attention in recent years, due to possibility of reduction in number of interconnections and the potential for increased information content per unit chip area. With an increasing density of the chips, the number of inter chip connections is greatly increased as more and more functions are put on the same chip. The quaternary logic cells design of inverter, NAND and NOR with quaternary inputs and quaternary outputs are represented in this paper. Physical design of the logic circuits is simulated and correctness of the results is verified with TANNER tool at 250nm CMOS technology.

Index Terms-MVL, CMOS, NMIN, NMAX, VLSI, quaternary, SPICE.

#### I. INTRODUCTION

In a typical binary VLSI circuit, interconnect accounts for 70% of the chip's area while the processing transistors occupy only 10% of the chip<sup>[3]</sup>. The remaining 20% is devoted to insulation. Thus the design of the binary logic circuits is limited by the requirement of the interconnections. A more cost effective way of providing interconnections could thus be of great benefit. One of the most promising approaches to solve these interconnection problems is the use of multi-valued logic (MVL) inside the VLSI chip<sup>[4]</sup>. Multiple-Valued Logic system is one of the most promising approaches to realize future beyond-binary electronics and systems.

One possible solution can be achieved by using a larger set of signals over a similar chip area, such as multiple-valued logic (MVL) devices <sup>[1]</sup>. Multiple-valued logic can provide improved circuit interconnections, reduced chip area and increased bus efficiency, since more logic levels are used per line as compared to conventional binary logic.

### **II.** FUNCTIONAL DESCRIPTION

Out of two possible views on multiple-valued systems, first one i.e. systems with multiple inputs and multiple outputs is being selected for logic cells design and implementation. The focus will be on implementation of multiple-valued processing circuit. i.e. the circuit with multiple-valued inputs and multiple-valued output is to be designed and implemented.

Quaternary logic cells that are being designed and implemented with CMOS technology are:

- ~ Complement: Analogous to binary INVERTER
- ~NMIN: Analogous to binary NAND
- ~ NMAX: Analogous to binary NOR

The quaternary logic is used as a MVL function to design the logic gates in this paper. The logic level "0", logic level "1", logic level "2" and logic level "3" are represented by voltages 0V, 1V, 2V and 3V respectively in 250nm CMOS technology.

# III. QUATERNARY INVERTER

The Quaternary inverter circuit is an elementary form of various logic circuits. Function of inverter is to just complement the input signal.



Fig. 1 Quaternary Inverter

Table 1 Truth Table for Quaternary Inverter

Xi(i/p)	Xo(o/p)	
0	3	
1	2	
2	1	
3	0	

The output signal expression or the complement function is calculated as: Xo = r - 1 - Xi

Here, r = radix of the system, Xo = output Xi = input The schematic of inverter in gate level representation is shown in Figure 2. The quaternary logic inverter requires 5 NMOS and 5 PMOS. The schematic is designed in TANNER EDA tool for 250nm technology.



Fig. 2 Schematic of Quaternary Inverter



Fig. 3 Simulation result of Quaternary Inverter

# IV. QUATERNARY NAND GATE

Quaternary NAND gate is also an elementary form of various logic circuits. Like inverter and NOR, it can be used to realize the memory circuits.

Output expression of quaternary NAND gate is:

OUT = (In1 . In2)' Here, In1 = Input 1, In2 = Input 2



Table 2 Truth Table for Quaternary NAND Gate

The principle of operation of quaternary NAND gate is based on the standard INVERTER. Three mor transistors are added in parallel. Table 2 represents the truth table for quaternary NAND gate.



Fig. 5 Simulation results of Quaternary NAND

# V. QUATERNARY NOR GATE

Quaternary NOR can be used to realize the memory circuits such s flip-flops. By using flip-flops shift registers and counters can be designed.



Fig. 6 Quaternary NOR Gate

In1 In2	0	1	2	3
0	3	2	1	0
1	2	2	1	0
2	1	1	1	0
3	0	0	0	0

Table 3 Truth Table for Quaternary NOR Gate

Output expression of NOR gate is: OUT = (In1+In2)' Here, In1 = Input 1, In2 = Input 2

The Table 3 represents the truth table for quaternary NOR gate. The schematic and simulation results of the quaternary NOR gate is shown in the Figure 7 and Figure 8 respectively.



Fig. 7 Schematic of Quaternary NOR



Fig. 8 Simulation results of Quaternary NOR

# **VI.** CONCLUSION

This paper present implementation of quaternary basic logic cells such as inverter, NAND and NOR. CMOS technology is used to design the logic cells. The circuits are simulated using TANNER SPICE.

Circuit complexity has been reduced by using three values of enhancement mode threshold voltage and by utilizing a priority rule in establishing the output voltage i.e. the priority is given to low level at all times when several transistors are in the ON state. This principle of operation leads to the marked decrease in the in the transistor number and exact transient response.

## VII. FUTURE WORK

Quaternary logic cells are designed using SPICE low-level model parameters. In future, the work could be extended to higher level model parameters. This work can further be extended by layout extraction from SPICE code of the logic cells. The layout can further be optimized to get results nearer to ideal conditions.

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