CNT FETs the Next Generation of FETs

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Abstract - In this paper I have tried to show the various types of CNTFETs yet being manufactured their process of manufacturing and also various applications with their performance yet as various logic gates.

Keywords - CNTFET,SBFET

I. INTRODUCTION

By the year 1991 the discovery of CNT by ijima. CNTs have attracted most of the nanocircuits designers with there unique electrical and mechanical properties. Ever since the 0.35m node, the gate length of MOSFET has entered the deep-submicron region. 65 nm technology becomes the mainstream since 2006, and 45nm technology has been announced in 2007. As CMOS continues to scale deeper into the nano scale, various device non-idealities cause the I-V characteristics to be substantially diff erent from well-tempered MOSFETs. It becomes more difficult to further improve device/circuit performance by reducing the physical gate length. The discrepancy between the fabricated physical gate length and the ITRS projected gate length becomes larger as the technology advances. On the other hand, as the major driving force for the semiconductor industry, the device contacted gate pitch (Lpitch) is scaled down by a factor of 0.7 every technology node.

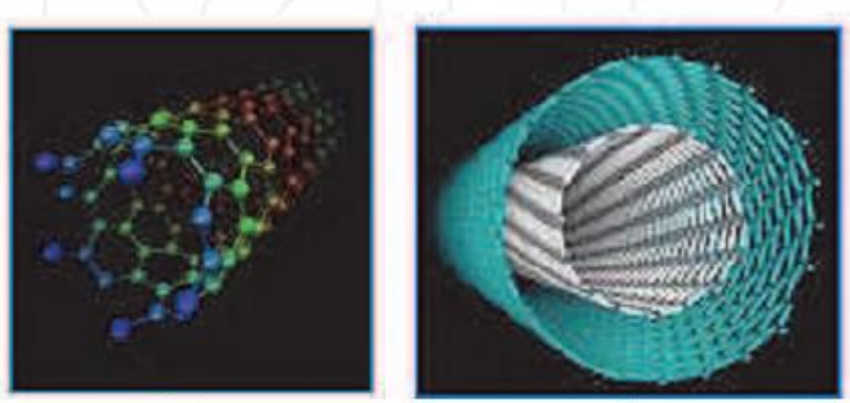
Last few years have seen an extensive increase in research regarfing new materials to replace the existing CMOS so to fit into the present needs of scaling.CNTFETs appear to be the most promising technology to take the place of CMOS in coming days of nano technology.they are most preferred over the other complement traditional silicon technology due to three reasons: First, the opera- tion principle and the device structure are similar to CMOS devices; we can reuse the established CMOS design infrastructure. Second, we can reuse CMOS fabrication process. And the most important reason is that CNFET has the best experimentally demonstrated device current carrying ability to date.

Carbon Nanotube Field-Effect Transistors

As one of the promising new devices, CNFET avoid most of the fundamental limitations for traditional silicon devices. All the carbon atoms in CNT are bonded to each other with sp2 hybridization and there is no dangling bond which enables the integration with high-k dielectric materials. In the next section, we introduce the basic properties of CNFET.

II. CNT

CNTs have been a leading candidate in continued improvement of the performance, speed and density of integrated circuits. CNT can be viewed conceptually as graphene (a single atomic layer of graphite) sheets rolled up into concentric cylinders. The number of sheets is the number of walls and thus CNTs fall into two categories: single-wall CNTs (Figure 1a) and multi-wall CNTs (Figure 1b). There are currently three methods to synthesize CNTs: arc discharge, laser ablation and chemical vapor deposition (CVD).



(a) (b)

CNTs metals or semiconductors?

The atomic structure of a single-walled CNT is conveniently explained in terms of two vectors Ch and T. T is called translational vector, it defines the direction of CNT axis. Ch is called chiral vector, representing the circumference of a CNT. Two carbon atoms crystallographically equivalent to each other were placed together according to: Ch = n. a1 + m. a2, where a1 and a2 are the unit vectors of 2D graphene sheet (Figure below). (n, m) indices determine the diameter and chirality of CNTs.

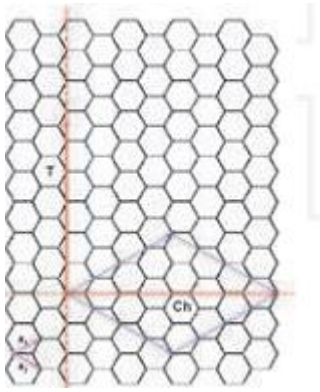


figure 1C

eoretical studies have shown that a single-walled CNT can be either metallic or semiconducting depending on its chirality and diameter. (n, m) nanotubes with n = m (arm-chair) are metallic; for n – m * 3 * integer, the nanotubes are semiconducting with band gap proportional to 1/d. For n – m = 3 * integer, the nanotubes would be quasi-semiconducting with a small band gap proportional to 1/d2. The sensitivity of electrical properties on structural parameters in unique for CNTs, which opens up numerous opportunities in nanotube systems.

Another figure below is given to strengthen the abovce argumet how chairality causes a CNT to be m etallic or semiconducting

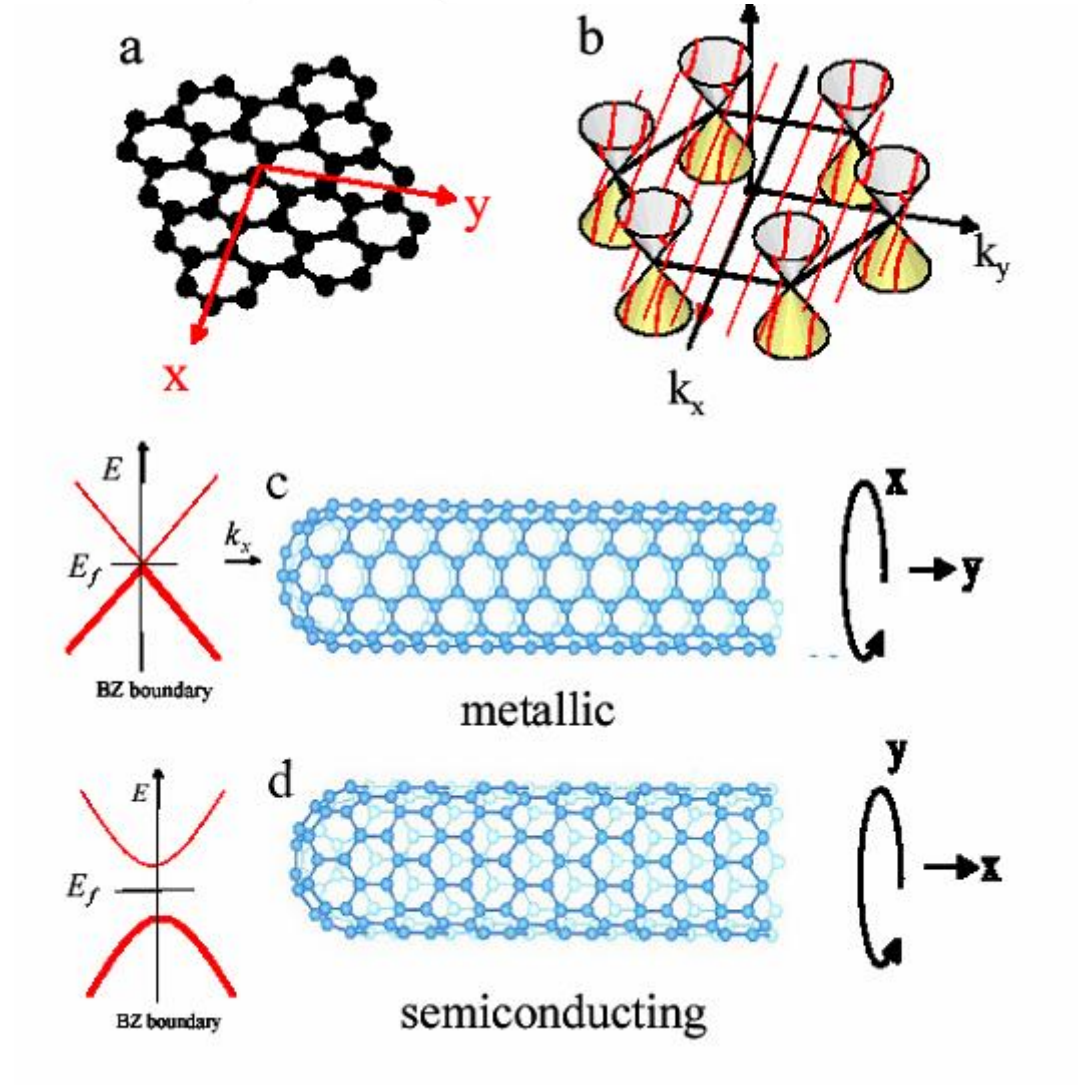


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figure 1d

In the above figure metallic one is the nornal arm-chair rolled graphene CNT whereas in case of the semiconducting rolling-up of graphene sheet is done at a particular angle.

Types of CNTFETs

There are basically two types of CNTFETs on basis of device operation mechanism.

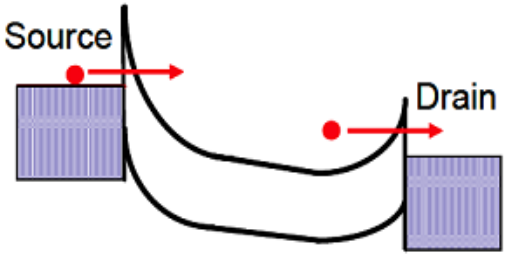
1. SBFET(schottky barrier FET)

2. MOS type FET.

Operation of CNTFETs

1-SBFET

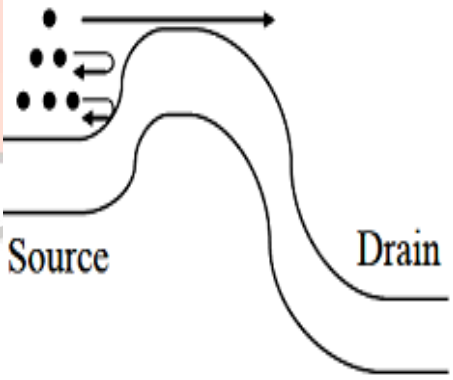
The operation principle of carbon nanotube field-eff ect transistor (CNFET) similar to that of traditional silicon devices. This three (or four) terminal device consists of a semiconduting nanotube, acting as conducting channel, bridging the source and drain contacts. The device is turned on or off electrostatically via the gate. The quasi-1D device structure provides better gate electrostatic control over the channel region than 3D device (e.g. bulk CMOS) and 2D device (fully depleted SOI) structures . The conductivity of SB-CNFET governed by the majority carriers tunneling through the SBs at the end contact .The on-current and thereby device performance of SB-CNFET is determined by the contact resistance due to the presence of tunneling barriers at both or one of the source and drain contacts, instead of the channel conductance, as shown by Fig (a). The SBs at source/drain contacts are due to the Fermi-level alignment at the metal-semiconductor interface. Both the height and the width of the SBs, and therefore the conductivity, are modulated by the gate electrostatically. SB-CNFET shows ambipolar transport behavior . The work function induced barriers at the end contacts can be made to enhance either electron or hole transport. Thus both the device polarity (n-type FET or p-type FET) and the device bias point can be adjusted by choosing the appropriate work function of source/drain contacts.

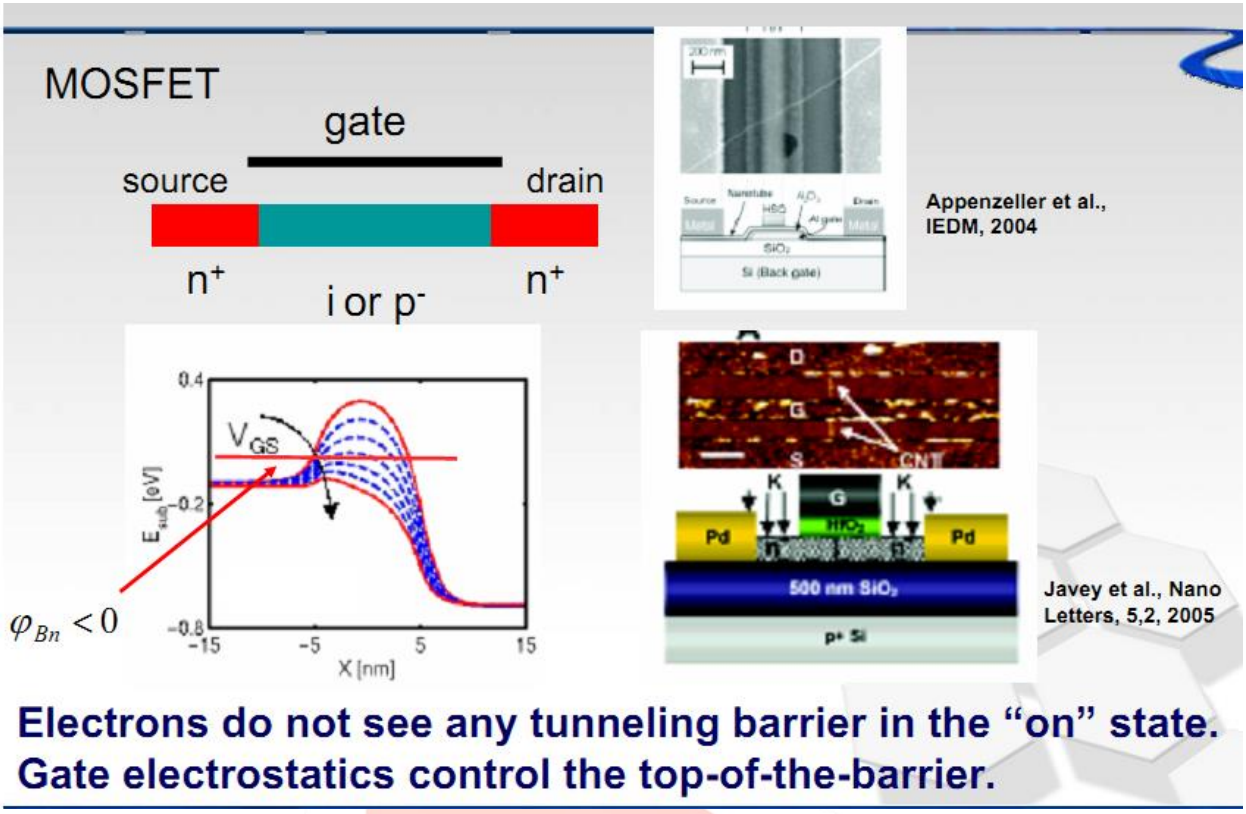


(a) SB-CNFET

2-MOS type FET

In case of mos type CNTFETs the source and drain are basically semiconductors p-type or n-type which are heavilly doped. . The non-tunneling potential barrier in the channel region, and thereby the conductivity, is modulated by the gate-source bias voltage same as the silicon enhancement type MOSFET.the mos type CNTFETs generally show a unipolar behaviour.





In the above figure it is shown that a barrier is created whose height can only be controlled using the gate voltage.as the height decreases more electrons can crossover and more will be the current but still we need some threshold voltage at gate after which this transport can only start.so we can conclusively say about the mos type CNTFETs that they exhibit characteristics of simple si type MOSFETs.

Fabrication of CNTFETs

There are two methods basically to fabricate CNTFETs pre grown and situ.

pregrown

There are various ways of synthesizing CNTs eg- by either arc discharge, laser ablation or CVD technique, and are dispersed in the aqueous surfactant solution. This solution is used to deposit CNTs on the oxidized substrate by drop casting or spin coating method.All the three types of gate structure can be made, namely global back gate , local back gate , and top gate . The major drawback of global back gate structure is that the individual transistor on the substrate cannot be controlled. However, using the local back gate or top gate structure, it is possible to control transistors individually. The subthreshold slope, a measure how fast the device switches, is more for local back gate and top gate CNTFET compared to global back gate CNTFETgate or triple gate CNTFET.

Situational

If during fabrication we grow CNTs it adds few advantages to fabrication and in situational CNT growth we grow the CNTs during the fabrication of CNTFETs. We have to use CVD technique for fabricating CNTs. The CNTs are synthesized on the substrate by depositing thin film of catalysts followed by CVD process. The CNTs can be either grown from the patterned catalytic island or non-patterned catalyst. After the growth of nanotubes, patterned source and drain contacts are deposited. The advantage of this process is that the origin of the CNTs can be known and most importantly, by changing the catalytic island dimensions, it is possible to have the required density of CNTs in the transistor. AFM method is also used to make the electrical contacts for the CNTs. The metal/CNT contact resistance will be less as the metal is deposited over CNT. Both top gate and back gate CNFETs can be fabricated using these CNTs. In both the above methods two types of FETs are fabricated back gated and top gated. Lets only see the backgated and top gated FETs fabrication for situational fabrication technique.

III. BACKGATE CNTFET

The fabrication of back gate CNTFET is carried out on low resistivity Si p-type substrate wafer. The fabrication process uses four level photo lithographic steps to realize the transistor. Si wafer is RCA cleaned and SiO2 of 50 nm thickness is deposited by thermal oxidation process and the resulting oxidized wafer is as shown in Figure 4(a). LOR and photo-resist-coated wafer is exposed to UV light through mask 1 for catalytic islands as shown in Figure 4(b). The mask 1 contains patterns in square shapes. The cross-sectional view after the development of both LOR and photo-resist is shown in Figure 4(c). Figure 4(d) shows the cross-sectional view after deposition of Pd thin film. SWCNTs shown in Figure 4(e) are grown by CVD technique at a suitable temperature in the presence of carbon source. Top view of the SWCNTs grown by CVD process is shown in Figure 5(a). Source

and drain contacts for CNTFET are obtained by patterning the photo-resist using the second-level mask as shown in Figure 4(f). Pd material of 5 nm thickness is deposited followed by lift-off process and resulting structure is as shown in Figure 4(g). Top view of the same is shown in Figure 5(b) for clarity. Using mask 3, the photo-resist is patterned to define larger area source and drain contacts as shown in Figure 4(h). A 50 nm thick Au is deposited over the Pd and is followed by lift-off, which results in a structure as shown in Figure 4(i). Unused SWCNTs outside the channel region are etched away in O2 plasma after protecting the CNTs over the channel using mask 4 shown in Figure 4(j). The cross-sectional view of the resulting structure is shown in Figure 4(k). The global back gate electrode of CNTFET is fabricated on back side of the wafer as shown in Figure 4(l) by depositing 50 nm thick Au using RF sputtering technique. Compared to the pre-grown back-gated CNTFET, this process requires an extra lithography, a metal deposition, and a CVD process.

Figure 4a: Si/SiO_2 thermally grown oxide.

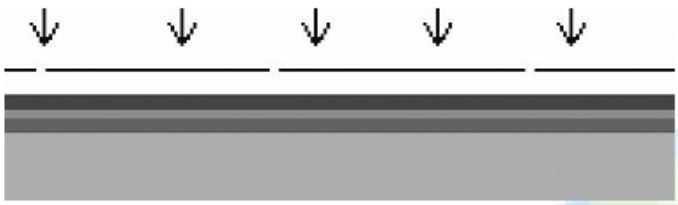


Figure 4b: Photolithography using mask 1 to define catalytic island regions.

Figure 4c: Developed LOR and photo-resist layers.

Figure 4d: Deposition of Pd for SWCNT growth.

Figure 4e: SWCNTs grown by CVD technique.

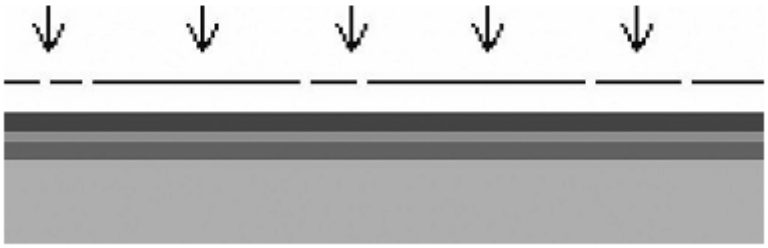


Figure 4f: Photolithography using mask 2 to define source and drain contacts.

Figure 4g: Thin layer of Pd deposited as source and drain contact.

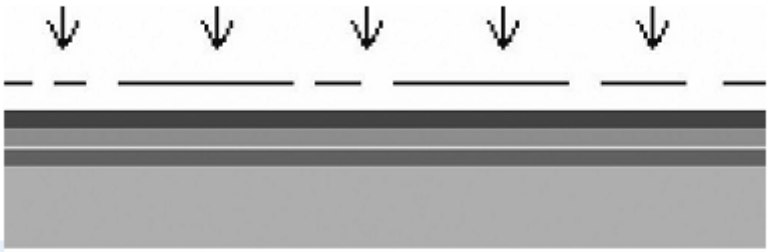


Figure 4h: Photolithography using mask 3 to define larger area source and drain contacts.

Figure 4i: Au deposited on source and drain contacts for probing purpose.

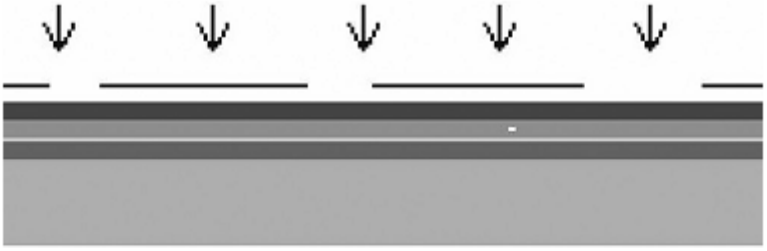


Figure 4j: Photolithography using mask 4 to protect CNTs in channel region.

Figure 4k: Unwanted SWCNTs etched by O_2 plasma.

Figure 4l: Au deposition as gate contact at back side of the substrate.

Figure 5a: SWCNTs grown by CVD technique.

Figure 5b: Pd deposited for source and drain contact.

Figure 5c: Unwanted SWCNTs etched by O_2 plasma.

IV. TOP GATED CNTFET

Initially the steps for the fabrication of top-gated CNFET using in situ CNTs are similar to back gate counterparts till the deposition of palladium for source and drain contacts. Third-level mask is used as shown in the Figure 6(a) to define the region of gate oxide. Deposition of thin layer of gate dielectric material is followed by the lift-off process and will result in a cross-sectional view as shown in Figure 6(b). Subsequent lithography process using mask 4 is carried out to define gate contact region as shown in Figure 6(c). Deposition of Pd followed by lift-off will provide the gate contact for CNTFET as shown in Figure 6(d). Using mask 5, in the last lithography process as shown in Figure 6(e), larger area contact regions are defined. Subsequent 50 nm thick Au deposition followed by lift-off process will result in a cross-sectional view as shown in Figure 6(f). Unused SWCNTs outside the channel region are etched by exposing the wafer to O2 plasma. CNTs in the channel region are protected by the gate oxide layer. The top view of the top-gated CNTFETs is shown in the Figure 6(g). In summary, this process consists of five lithography process, four metal, and one dielectric deposition process.[10].

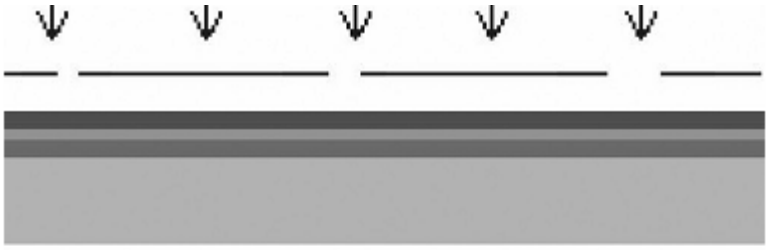


Figure 6a: Photolithography using mask 3 to define gate oxide region.

Figure 6b: Deposition of high k gate dielectric material.

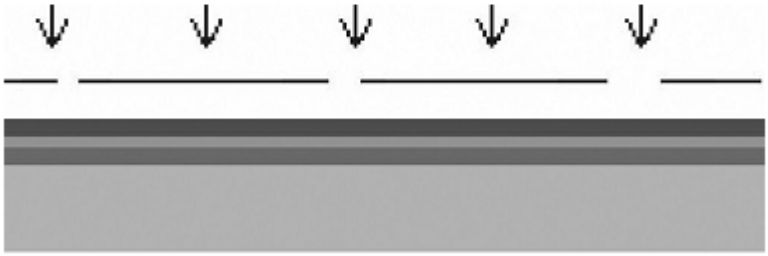


Figure 6c: Photolithography using mask 4 to define gate contact.

Figure 6d: Pd deposited for gate contact.

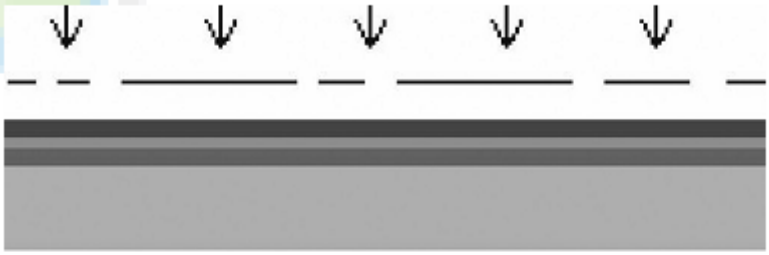


Figure 6e: Photolithography using mask 5 to define larger area source and drain contacts.

Figure 6f: Au deposited for probing purpose.

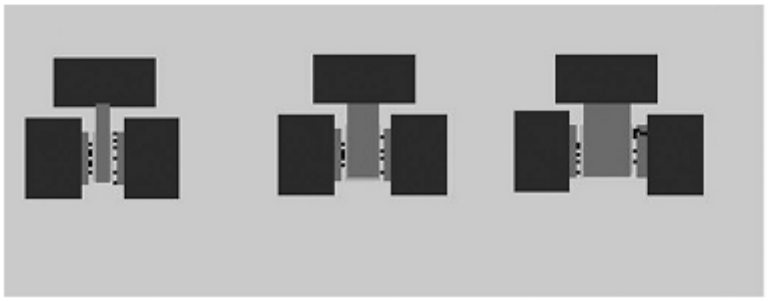


Figure 6g: Unwanted SWCNTs etched by O_2 plasma.

V. CHARACTERISTICS OF CNTFETS

The IV characteristics of CNTFETs can be said to be same as that of normal silicon MOSFETs The current voltage curve can be divided into two regions: linear and saturation.

$$I_d = \frac{W}{L}\mu C_{ox}[(V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}]$$

$$I_d = K_n\left[2\left(V_{gs} - V_T\right)V_{ds} - V_{ds}^2\right]$$

where K_n is conductance of CNTFET, W is the width of CNTFET, L is the length of CNTFET, μ is mobility of carriers, C_{ox} is oxide gate capacitance.

We can also obtain saturation current of CNTFET by replacing $V_{ds(sat)} = V_{gs} - V_T$. Then the expression of saturation current of CNTFET can be written:

$$I_{d(sat)} = K_n \left(V_{gs} - V_T \right)^2$$

The simulation for the IVcharacteristics can be shown as-

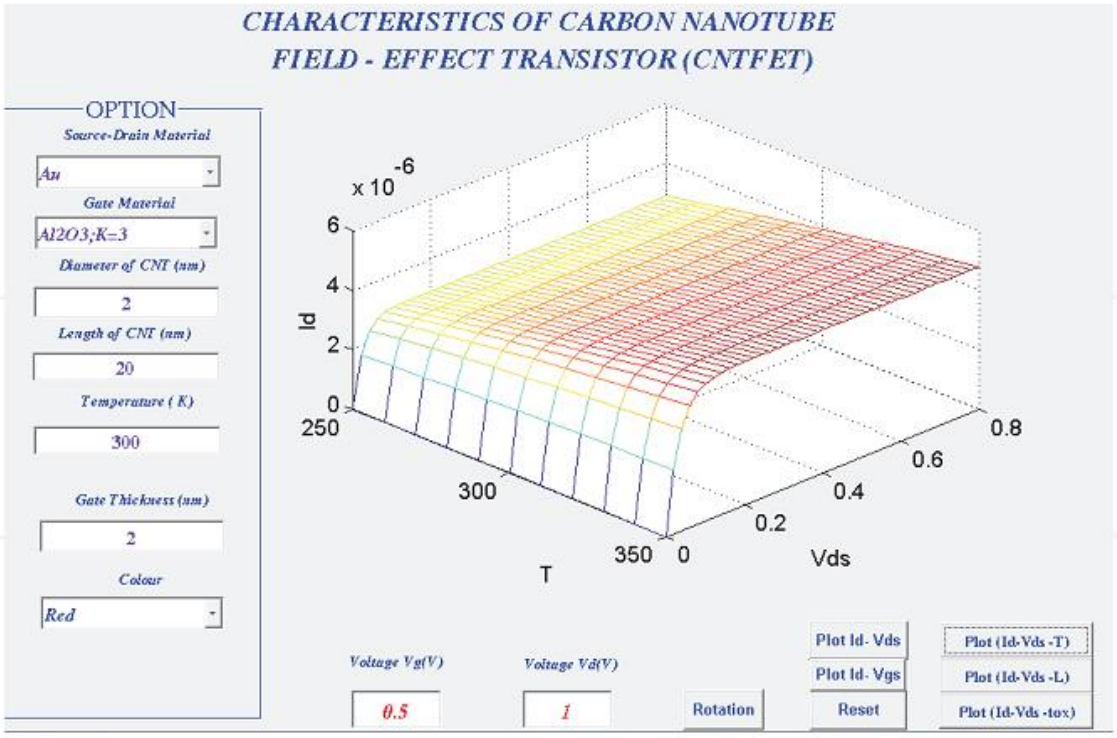
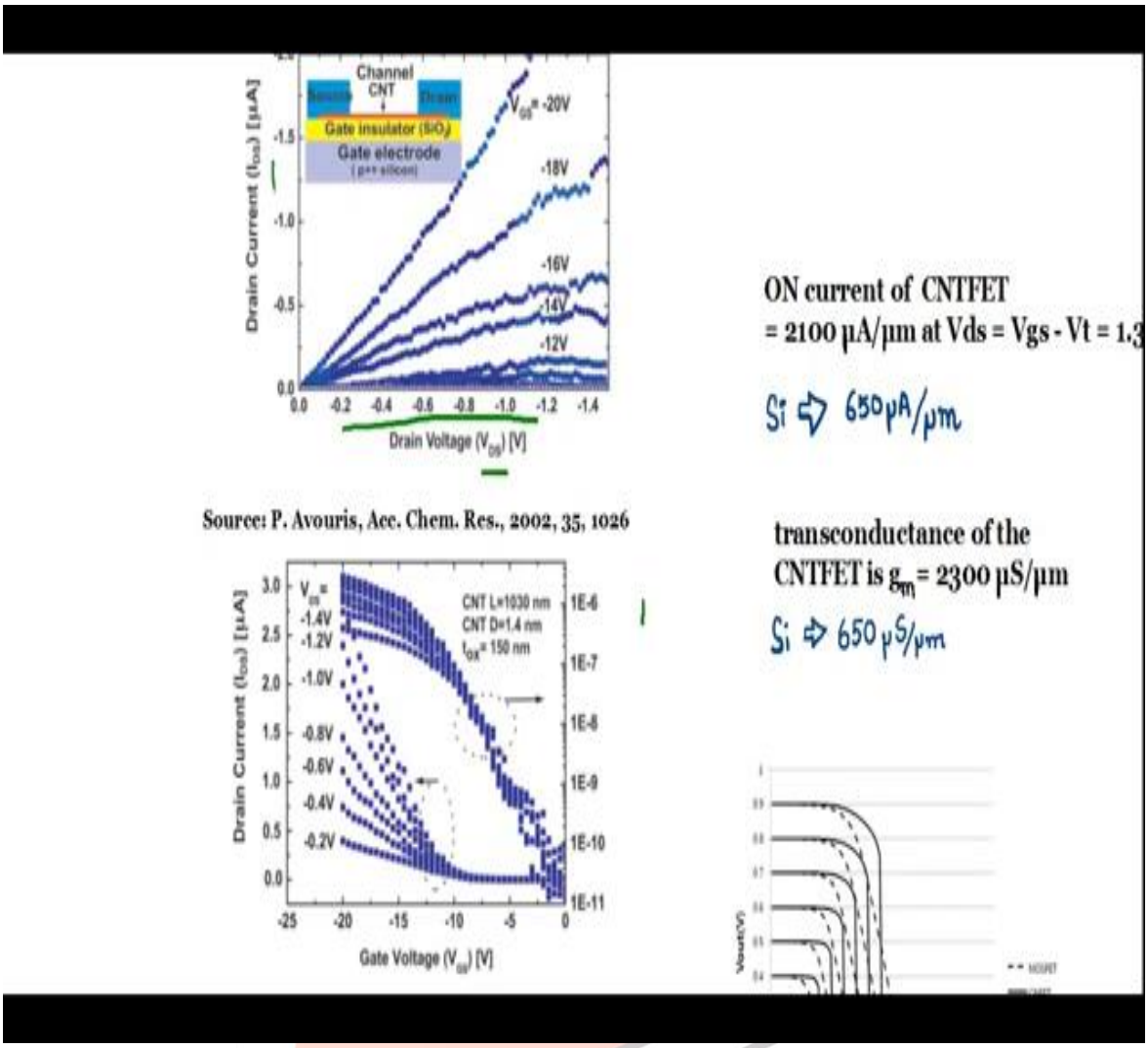


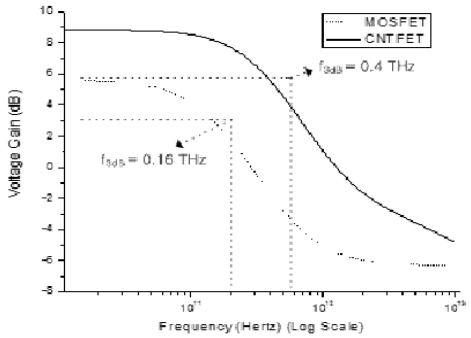
Fig. 9. Drain current-voltage characteristics in 3D. When CNTFET is cooled, its saturation drain currents are lightly decreased.

The plot of the IV characteristics can be shown as



Frequency response

The frequency response, AC simulation has been performed for both the MOSFET and CNTFET inverters. The results are given in (Fig), the CNTFET inverter shows nearly 3dB more voltage gain and 3 times higher 3dB frequency (f3dB) than the MOSFET inverter, thus confirming its superiority in terms of this metric.



VI. COMPARISON BETWEEN MOS LOGIC GATES AND CNTFET LOGIC GATES

In this section different metrics are utilized to compared CNFET and CMOS logic gates at 32nm features size.

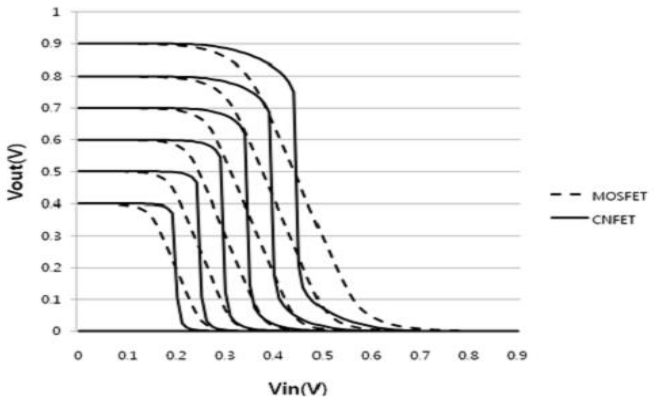
Power Delay Product (PDP)

Due to the increased demand for high-speed, high-throughput computation, and complex functionality in mobile environments, reduction of delay and power consumption is very challenging. MOSFET and CNFET can be compared using the Power Delay Product (PDP) as metric. Table 2.1 shows the delay, power ,and Power Delay Product (PDP) of logic gates in 32nm MOSFET and 32nmCNFET technologies; the PDP of the 32nm MOSFET is about 100 times higher than that of the 32nm CNFET.

LEAKAGE

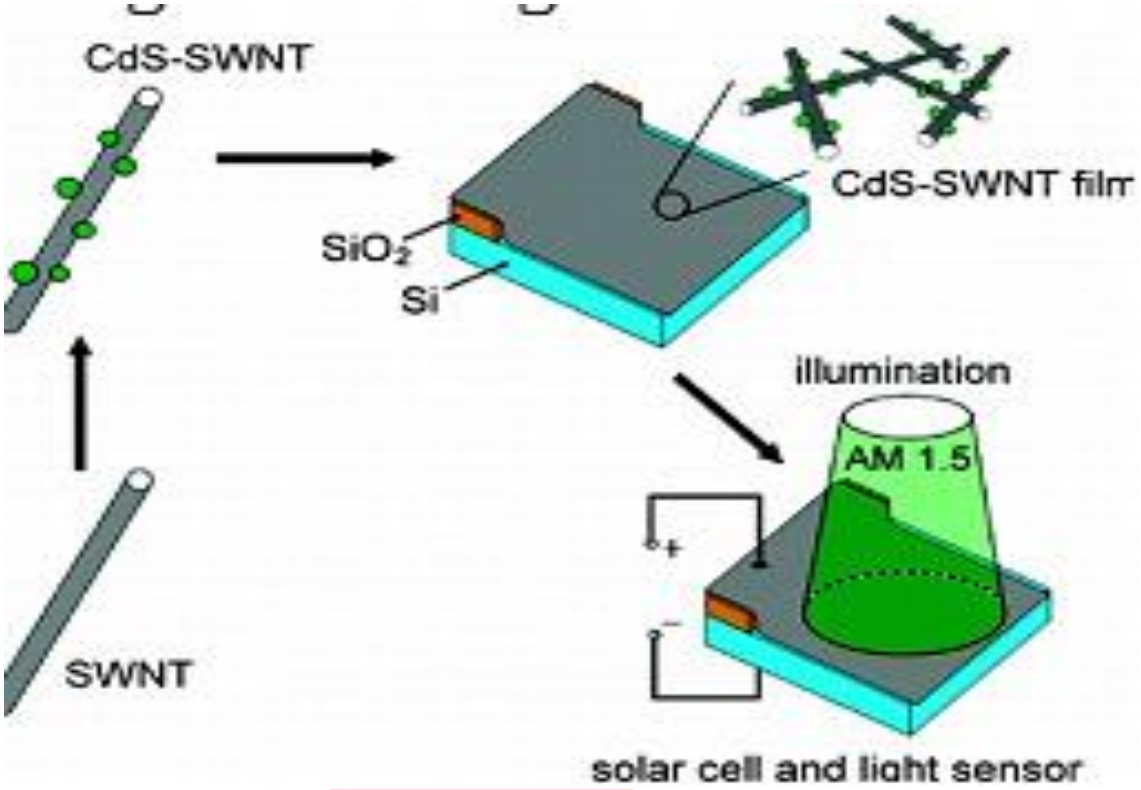
As process dimensions shrink further into the nanometer ranges, traditional methods for dynamic power reduction are becoming less effective due to the increased impact of static power. In general, leakage power is different depending on the applied input vector. Fig(1) shows the maximum and minimum leakage power for 32nm MOSFET and CNFET-based logic gates. The maximum leakage power of the MOSFET-based gates is 75 times larger than for CNFET gates. The minimum leakage power of the MOSFET is about three times larger than for CNFET. Fig(1)also shows that the maximum leakage power shows a similar trend for both CNFET and MOSFET-based gates, while the minimum leakage power shows somewhat different trends, because the stack effect is reduced in CNFET circuits .

		Delay(sec)	Power(watt)	PDP(joule)
MOSFET	Inverter	1.77E-11	1.39E-06	2.46E-17
	NAND2	2.26E-11	1.96E-06	4.41E-17
	NAND3	2.99E-11	2.77E-06	8.29E-17
	NOR2	3.97E-11	2.58E-06	1.02E-16
	NOR3	6.97E-11	4.04E-06	2.82E-16
CNFET	Inverter	2.42E-12	1.11E-07	2.69E-19
	NAND2	3.49E-12	1.89E-07	7.41E-19
	NAND3	5.06E-12	2.90E-07	1.47E-18
	NOR2	3.50E-12	1.85E-07	6.48E-19
	NOR3	5.08E-12	2.73E-07	1.39E-18



Applications

- SRAM using nanotubes are yet produced and optoelectronic applications such as light emitting nanotubes are yet produced by IBM company.
- considerable applications are yet investigated in the fields of sensing and energy conversions.



VII. CHALLENGES IN CNTFETs

- 1-High background noise.-Due to the inherent nature of carbon molecules the backgrounf noise goes higher which creates a trouble in operation of CNTFETs.
- 2-Parasitic capacitance and huge external resistance-many a times it has been seen that CNTFETs channel CNTs grow inherent capacitance due to which we get deviation in the performance.also due to the array of CNTs in the channel the resistance of channel increases and we have a very low charge mobility which reduces the precision of device.
- 3-Synthesis methods.-the methods of fabrication are very cumbersome and difficult.
- 4-lifetime-The CNTs have a very small lifetime when exposed in oxygenous environment so this is a big trouble for longer working devices.
- 5-Lesser control on the characteristics of CNT-we actually don't have any control on what will be the characteristics of the CNTs fabricated as they could be semiconductors or metals so what happens that we have to give a high drain voltage just after the fabrication of CNTFETs so that the metallic CNTs get destroyed and only semiconducting ones prevail in the channel.

VIII. CONCLUSION

As we see that the CNTFETs appear to be similar to that of CMOS and simple MOSFETs in their characteristics and have a better performance but come with some mind boggling challenges have all the potential to be the next generation basic devices for nano circuit fabrication. We also have seen the better performance of the CNTFET logic gates at smaller scales around 32 nm compared to that of CMOS and take lesser power. They also have an edge over the MOSFETs in terms of their frequency response as they allow a better frequency curve at a gain twice that of MOSFETs.

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