Analysis of switching transient and fault detection of strong power system using PLL

[1]Rajkumar Nagar, [2]D.K.Yadav
[1]M.Tech Scholar, [2]Associate Professor,
[1]Department of Electrical Engineering,
[1]University College of Engineering, RTU, Kota, India

***Abstract* – In power system to discriminate faults from switching transients a new method is proposed in this paper. In this method before the occurrence of first peak of the fault current, fast fault detection and fast fault clearing are essentially required for stable power system. An Example of this system is in an industrial system where bulk power is desired but there high short-circuit currents cannot be measured. Here we are proposing the method of Phase-Locked Loop (PLL) to perform the task of discrimination of Faults and transients. The power system model is developed and simulated for fault performance analysis. MATALB simulations have been performed and the output of the PLL is found completely different for a fault, as compared to a Switching Transient. This difference is being used in this work for discrimination between a fault and a Switching Transient. This capability of discrimination is useful for the safety and stability of the power system.**

***Index Terms* - Fault protection, phase-locked loop (PLL), power system, transients, fault current limiter.**

I. INTRODUCTION

Occurrence of faults and transients in a power system is a common phenomenon .The transient and faults current both are of the same order (value) and it becomes very difficult to distinguish between these. The protection system design starts to operate for the safety of system after occurrence of any one of these two disturbances in the absence of proper identification. But the transient are very frequent and of very small duration and the system should not be shut down during this disturbance so if some reliable scheme can be developed to distinguish these disturbances, it can be very helpful for the proper operation of protection system.

Power is often desired in an industrial system in order to connect and disconnect loads without causing disturbances to sensitive equipment or processes. With the high value of short-circuit power, a high fault current develops with the faults in the system. This high fault current has to be considered when designing the switchgear and other components that build up the power system. This is easily done in new installations but can be problematic when there is a need for higher short-circuit power in an existing system. In these cases, the installation of a fault current limiter could be an alternative to rebuilding the switchgear. The installation of a fault current limiter can also provide the opportunity to make connections in the power system that otherwise would not be possible due to fault currents that exceed the rating of the switchgear.In [1], a trend toward increased short-circuit power is reported, which is also illustrated by an experience of more than 2 800 installations of fault-current limiters throughout the world. In this paper, the need for fast and reliable protection is discussed. Fault-current limiters are an essential building block in many systems as well as the need for fast and reliable fault detection. It is demonstrated that a phase-locked loop (PLL) can be used for power system protection purposes as an alternative to other methods. An investigation on how to use a PLL for the purpose of discriminating between a fault and a switching transient has been performed. It is proposed that the protection relay will detect the current transient and that the PLL will determine whether the current transient is caused by a fault or a switching transient. This paper is structured in the following way: First, a background on fault-current limiters and fault protection is given. This is followed by a description of the PLL and how the PLL can be used in a method to detect faults and discriminate between faults and switching transients.

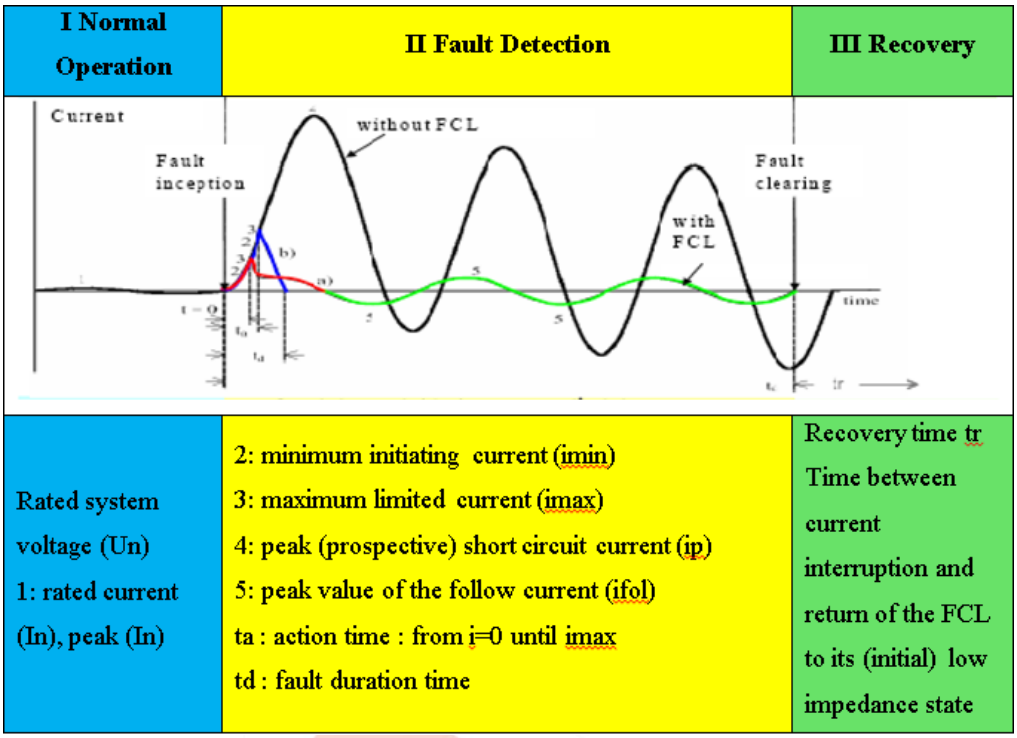


Figure 1 Fast protection scheme of power system

II. FAULT-CURRENT LIMITERS

One way of solving this contradiction is to use a fault-current limiter. A fault-current limiter is a device that during normal operating conditions allows a strong network but when a fault occurs, introduces enough impedance in the circuit so that the fault current can be limited. The prime objective of using a fault-current limiter is to fix the level of fault current so that its prospective peak value is never approached. The current limiting function can be achieved in various ways (e.g., using current limiting reactors [2]; fuses [3, 6]; triggered fuse [1]; superconductive fault–current limiters [4], [5]; and power-electronic-based current limiters [7]–[10].

III. POWER SYSTEM PROTECTION

The task of power system protection is essentially required and important issue. It is desired for safe operation of the power system so that faults can be detected and cleared automatically in a fast and reliable manner without disturbing the operation of the power system. The fault protection system components are circuit breakers (CBs), protection relays, and primary transducers, such as voltage and current transformers and auxiliary equipment. A large number of methods and algorithms available in the literature to detect short-circuit current in a power system. A simple and efficient method is to estimate the current from measured current samples. If the magnitude of the estimated current is larger than a predetermined threshold, it is assumed that a fault has occurred, and if more information is available, the estimation will become more accurate. On the other hand, if faster fault detection is required, the estimation becomes less accurate since less information is available. M. Öhrström presented fast fault detection and claimed to be in the range of 1–2 ms after fault inception [13]. This short detection time is needed for the fault-current limiters as mentioned in the previous section. Some methods suggested for use in transmission systems have the potential of being fast. These methods could be based on traveling waves [14], neural networks [15], wavelet transforms [16], and fault-generated noise [17]. Although it is sometimes possible to adapt the above mentioned techniques for fast fault detection in power distribution networks, new techniques have been explored [18]. In [9], a method for fast fault detection is described, which detects that a fault has occurred when five consecutive current samples are above a predefined threshold (i.e., the measured current samples are not fitted to a signal model). With proper signal processing (filtering), it was further demonstrated that it was possible to discriminate between a fault and common switching transient.

In this paper, a novel and unique method to perform the task of discrimination is proposed. Even though the detection of faults is the primary concern for fault protection devices (dependability), the ability to distinguish between a fault and a switching transient (security) is also important. Switching transients can, under certain circumstances, give rise to high currents, which are of larger magnitude than normal load currents. In existing relay protection schemes, capacitor energization have been detected by analyzing the measured current to find certain characteristics of the two types of current transients as described in [19]. The current transient typically contains a superimposed dc component, a superimposed second harmonic component and capacitor energization includes higher frequency harmonic components. The harmonic components in the measured current can be identified with Fourier-analysis methods, but that typically requires more time. For the purpose of fast fault detection, other methods have to be investigated. The PLL is proposed and used for the purpose of fast fault detection in this paper.

IV. PROPOSED METHOD

In this section, the proposed scheme of using a PLL for discrimination between faults and switching transients is being described. First, a short description of the basics of a PLL is given. Second, a well-known implementation of a PLL suitable for simulation purposes is described and the relevant signals that are used for the actual discrimination between a fault and a switching transient are identified. Third, the tuning of the parameters of the PLL implementation is discussed and suggestions for the first selection of parameters is given.

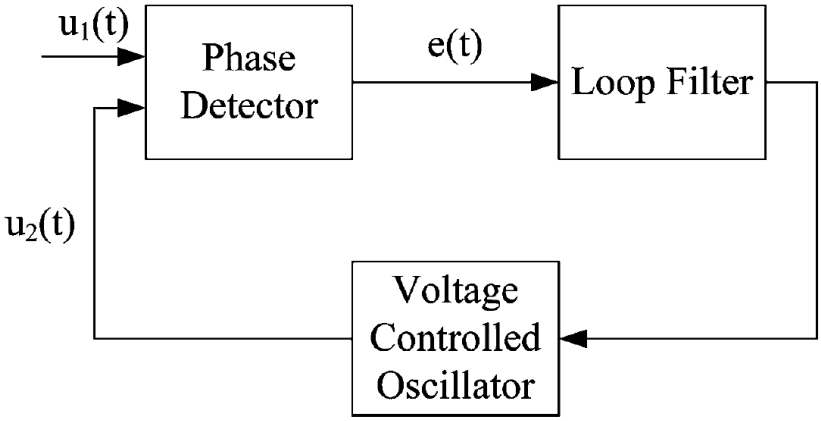


Figure 2 Block diagram of a Phase Locked Loop

Basics of a PLL

The PLL has been an important device in electronics and power system applications ever since the first implementation in the 1930s by de Bellescize, as mentioned in [20]. The first PLLs were analog devices but following the development in solid-state electronics and computer technology, the PLL has developed from an analog device via digital implementations to pure software implementations. A PLL is a circuit that is used to synchronize an input signal with a reference signal (an output signal that is generated by the PLL) with respect to phase and frequency. The function of the PLL can be explained from the block diagram of a simple PLL, as shown in Fig. 2. The input signal is compared with the reference signal in the phase detector (PD). The output of the phase detector is zero as long as the input signal and the output signal are equal in phase and frequency. If the phase or frequency of the input signal changes, the output of the phase detector will deviate from zero. The error signal is passed through a low-pass filter (LPF) and then through a voltage-controlled oscillator (VCO), which generates a reference signal (the output signal). If the error signal deviates from zero, the VCO will adjust the frequency of the reference signal so that the phase error becomes zero and makes the two signals in phase. When the input signal is in phase with the reference signal, the PLL is in its locked state; hence the name phase locked is used. Recent research related to PLLs has been from several research fields: general descriptions of PLLs [21], distributed generation applications [22], active power-line conditioner applications [23], servo controllers [24], as well as protection and control [25]–[27].]

Description of a PLL that is Suitable for the Discrimination between a Fault and a Switching Transient

The vector implementation, as shown in Fig. 3, of a PLL is described in this section. Compared to the block diagram of Fig. 2, the error signal corresponds to the output of the proportional-derivative (PD), whereas the proportional-integral (PI) regulator and the integrator corresponds to the loop filter and the voltage-controlled oscillator (VCO). We have set the phase of these signals as a variable. As s_2 is a function of cosine hence it is shifted by 90° from s_1.

$$s_3(t) = s_1(t)s_2(t) \quad (1)$$

$$s_1(t) = A_1 \sin[\omega t + \phi_1(t)] \quad (2)$$

$$s_2(t) = A_2 \cos[\omega t + \phi_2(t)] \quad (3)$$

The output of the multiplier is

$$s_3(t) = K_m A_1 A_2 \sin[\omega t + \phi_1] \cos[\omega t + \phi_2] \quad (4)$$

Where, K_m is the gain of the multiplier and A_1 and A_2 are constants. With a little trigonometric manipulation, this equation wrote in more descriptive manner

$$s_3(t) = \frac{K_d A_1 A_2}{2} \sin[\phi_1(t) - \phi_2(t)] + \frac{K_d A_1 A_2}{2} \sin[2\omega t + \phi_1(t) + \phi_2(t)] \quad (5)$$

$$s_e(t) = \frac{K_d A_1 A_2}{2} \sin[\phi_1(t) - \phi_2(t)] \quad (6)$$

Where $s_e(t)$ is error signal of PLL.

Here the multiplier signal consists of two parts, the first one (in blue) is function of only the phase difference of the two signals, and the second (underlined) term is at a frequency which is twice the signal frequency plus the sum of the two phases. We can use this equation to develop the PLL by recognizing that the output signal of the multiplier is a function of the phase difference of the two input signals. This is useful information and we can use it to synchronize the two signals. The second part of (5) at twice the signal frequency can be discarded by filtering it out since it does not offer any desired output. Thus, the error is zero exactly when the output angle of the PLL is in phase with the current of phase a. When a transient occurs in the system, the error signal will

deviate from zero. Depending on the characteristics of the transient, the deviation will have different magnitude and frequency. Since a fault is typically an ac fundamental power frequency character, the deviation will be different than a switching transient that contains non fundamental power frequency components. The behavior of the error signal of the PLL will also depend on the tuning of the PLL.

Tuning of the PLL

PLLs have been used for many years in HVDC transmission in order to synchronize the firing of the thyristors to the phase angle of the connected ac system. The PLL will be tuned to the power system frequency. It is thus a well-known procedure and it is advisable to use parameters from such an installation as a starting point for the tuning. Fine-tuning of the parameters can then be made by computer simulations or any other standard tuning method.

Fault Detection and Discrimination Using a PLL

The method that is used to detect a fault and discriminate the fault from a switching transient is described here. Two algorithms are executed in parallel in this scheme. The first algorithm is based on the estimation of the magnitude of the current. If the estimated magnitude is higher than a preselected threshold, a flag is set. The second algorithm is as previously mentioned, monitoring the error signal of a PLL. If this error signal exceeds a preselected threshold, a second flag is set. If both flags are set, it is determined that a fault has occurred.

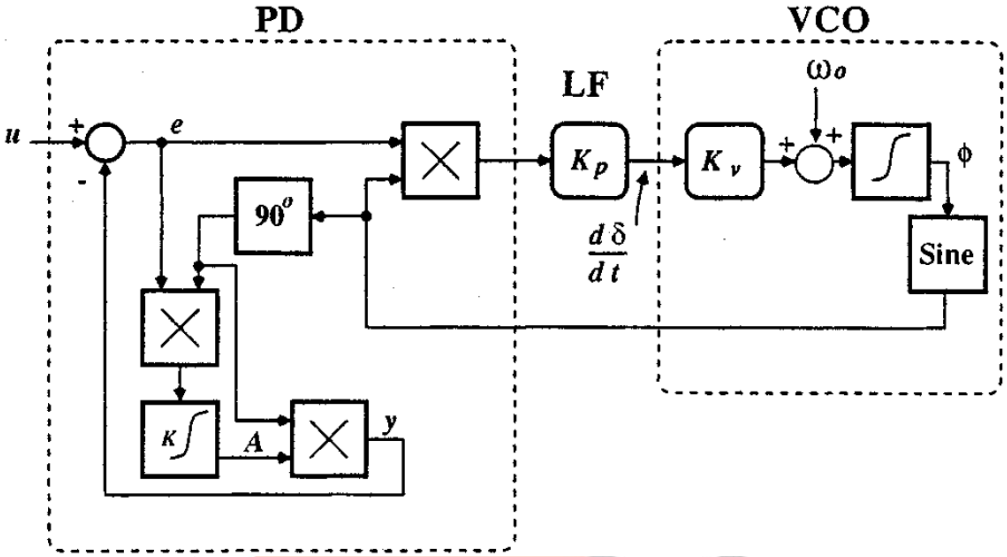


Figure 3 Implementation of PLL for discrimination of transient and fault.

V. SIMULATION

In order to test the proposed method, a simple test system has been developed and implemented in MATLAB Simulink.

1. The infinite source is modeled with a voltage source with series impedance. The supply voltage of the source has been chosen as V_h =12 kV. The series impedance is selected so that the power system will have a short-circuit power of approximately S_k = 831 MVA (R=12.2 mΩ, L= 0.55 mH). The supply frequency of the voltage source is selected to f = 50 Hz. A short-circuit power of S_k = 831MVA will give a short-circuit current of approximately I_k = 40 kA.
2. The load impedance is modeled by a resistor and an inductance connected in series. Their values are chosen so that the load current is approximately 630 A.
3. The fault selection arrangement is implemented by using a 3 phase fault block from the MATLAB simulink library. With this block, it is possible to simulate different types of faults (3 phase and 2 phase). At the start of the simulation, no fault is applied.
4. The shunt capacitor is modeled by a capacitance of C = 90.19μF. The shunt capacitor gives a reactive power supply of 4.08 MVAR at nominal voltage. The shunt capacitors connected to the power system by a CB which, at the time of starting the simulation, is open and uncharged.

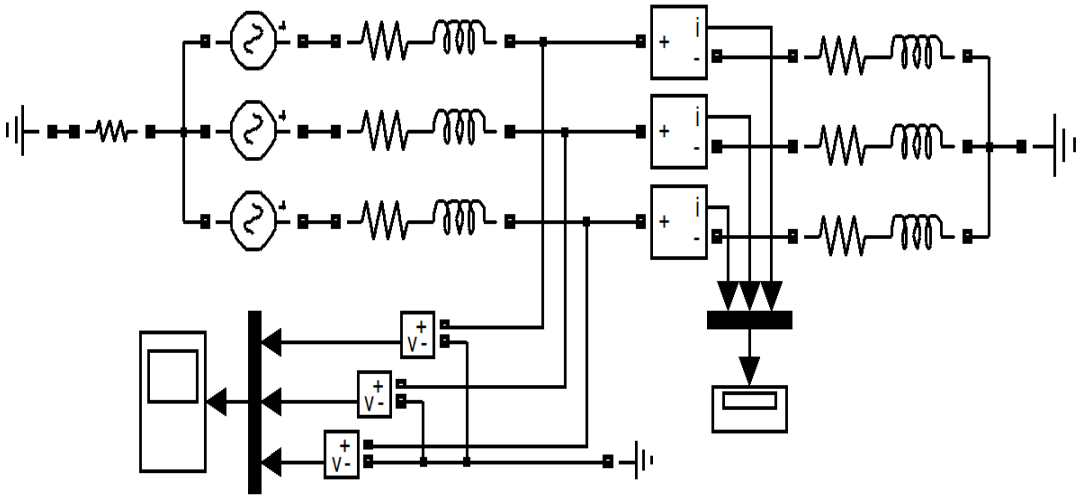


Figure. 4. MATLAB(Simulink) test system.

VI. SIMULATED EVENTS

A large number of shunt faults and capacitor energization cases have been simulated. The faults were simulated as three-phase faults and phase-to-phase faults with low impedance. For fault-current-limiting applications, this selection was made because these types of faults are occurring very commonly (most frequent) in real power system. Many distribution networks are using impedance earthing, which limits the magnitude of fault currents due to single-phase earth faults. The capacitor energizations have been simulated by closing the associated CB. All events have been simulated to occur at various times with respect to the phase angle of the supply voltage (the phase angle of phase voltage has been selected as a reference). The instant when the event occurs will determine some of the characteristics of the transient current such as, the magnitude and possible dc offset.

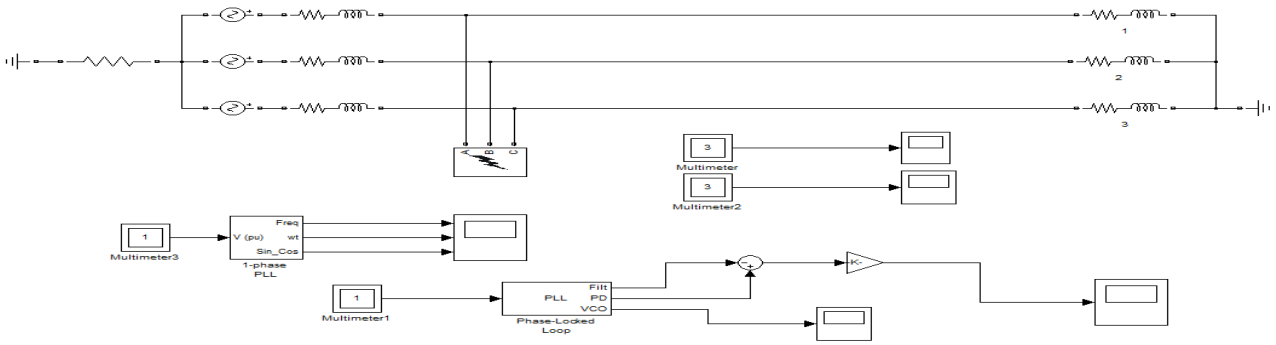
VII. RESULTS

A large number of results are available as a result from the simulations. A few selected results are presented here. The figures of this subsection contain plots of power system signals—mainly voltages and currents—but signals of the control system also, such as the error signal from the PLL, which has been taken as a measure on how much the measured current deviates from the pre fault load current.

Faults:

This section contains plots of signals caused by shunt faults in the power system. Both three-phase and two phase faults have been simulated and analyzed for peak overshoot of voltage and current. Typical phase voltages and currents due to a three-phase fault are plotted in Figure 6 and Figure 7. The error signal of the PLL for this fault is plotted in Figure 8. As can be seen from that figure, the error signal deviates largely from zero value (steady state) after the fault applied. However, after clearing the fault, the error signal returns to zero once the PLL has adjusted to the new conditions. Faults have been applied with different fault inception angles. The magnitude of the error signal of the PLL was found more than 10 p. u. for all the fault inception angles. Typical phase voltages and phase currents due to

a two phase fault are plotted in Figure 9 and Figure 10. The error signal of the PLL for this fault is plotted in Figure 11. As can be seen from Figure 11, the error signal again deviates from zero soon after the applied fault. Once the fault is cleared, the error signal returns to zero after a short transient period. In this case also faults have been applied with different fault



The Figure 5 Network Diagram of Three Phase Fault

inception angles. magnitude of the error signal of the PLL was well above 10 p. u. for all fault inception angles.

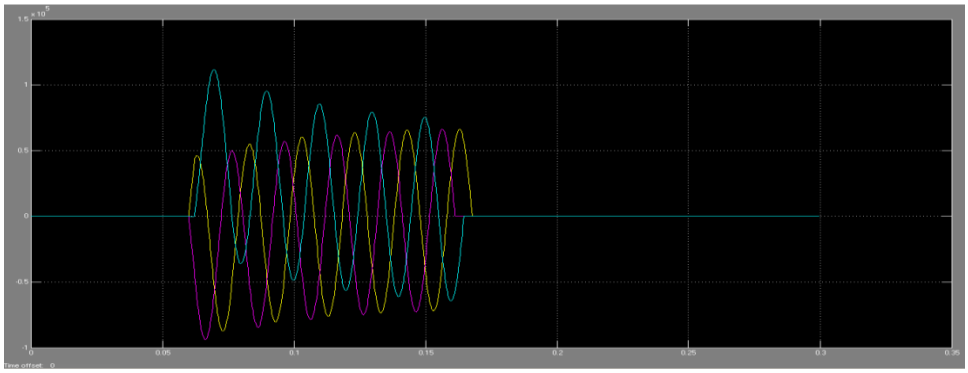


Figure 6 Phase Current Waveform For three phase fault

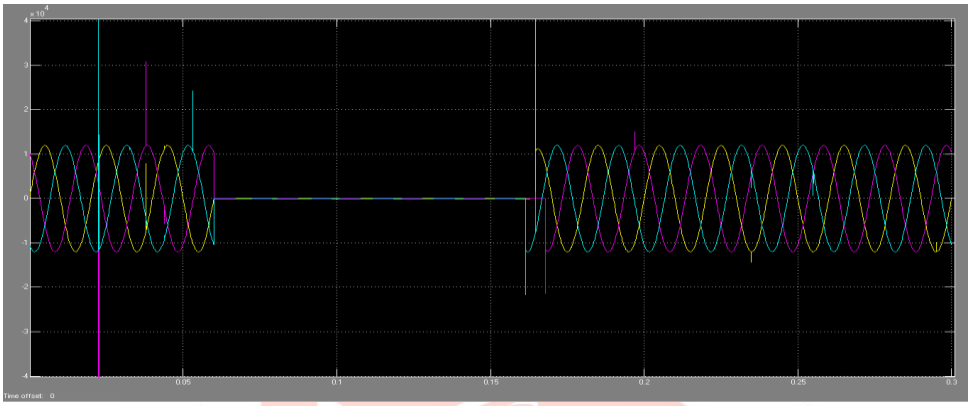


Figure 7 Phase Voltage waveform for three phase fault

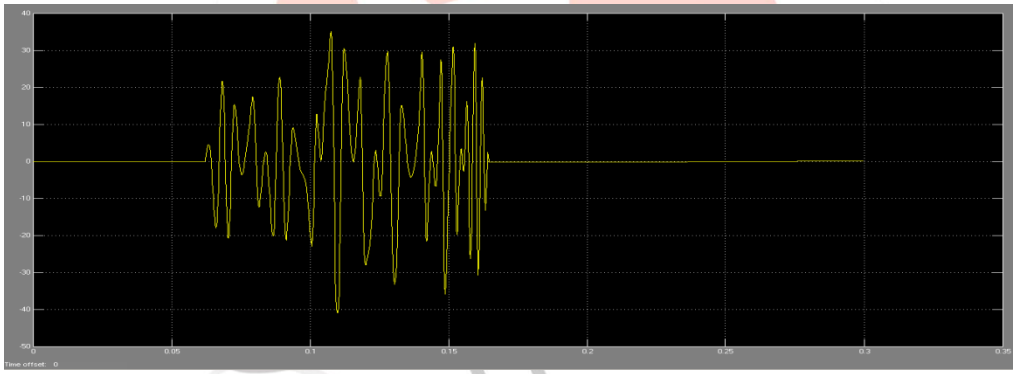


Figure 8 Error Signal Due to three phase fault

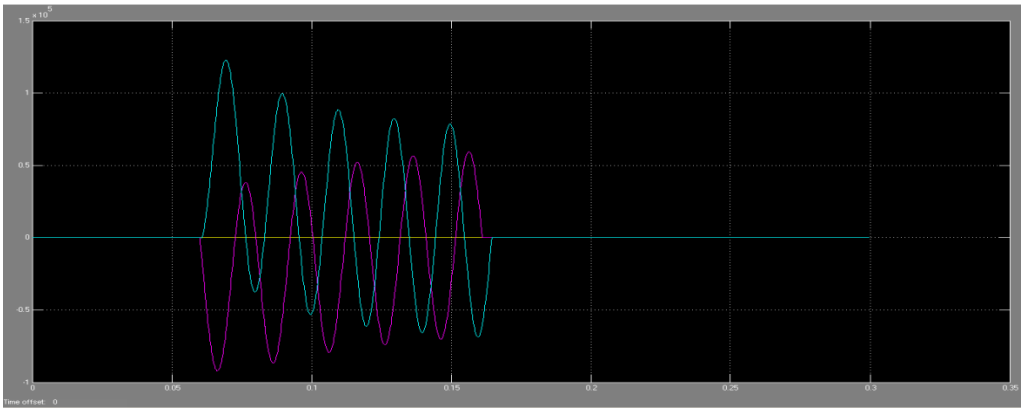


Figure 9 Phase Current Waveform For two phase fault

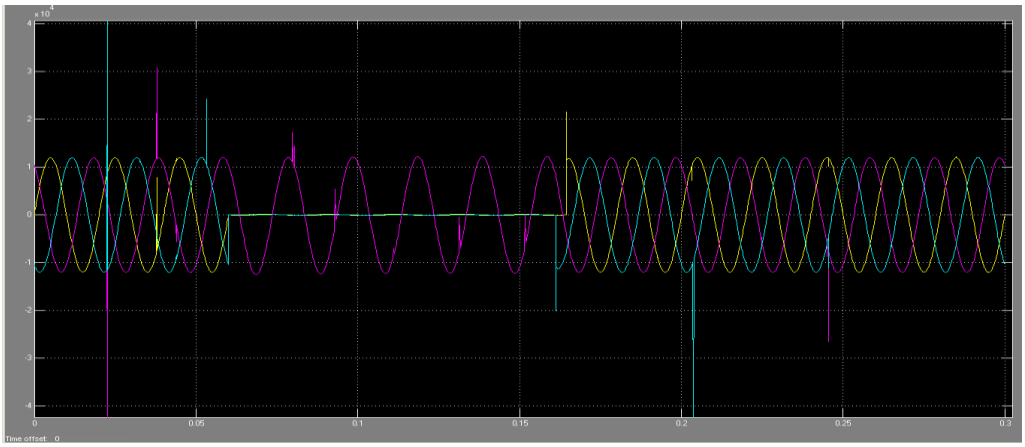


Figure 10 Phase Voltage waveform for two phase fault

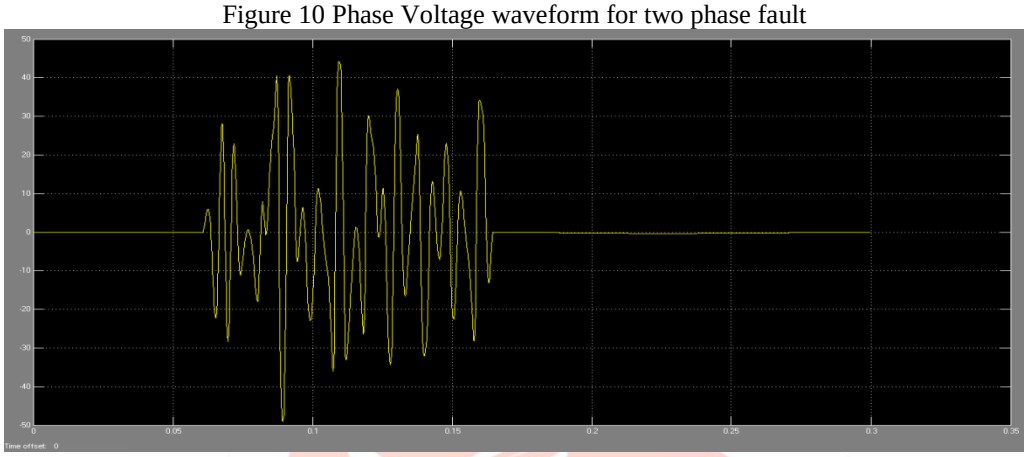


Figure 11 Error Signal Due to two phase fault

Capacitor Energization

In this section, plots of signals (voltages, currents, and error signal) caused by capacitor energization in the power system are presented in Figure 13, figure14 and Figure 15 respectively. As can be seen from the figure, the error signal deviates from zero shortly after the event has occurred but returns to steady state when the PLL has adapted to the new conditions. Different switching instants were investigated and the magnitude of the error signal was never reported above 5 p. u.

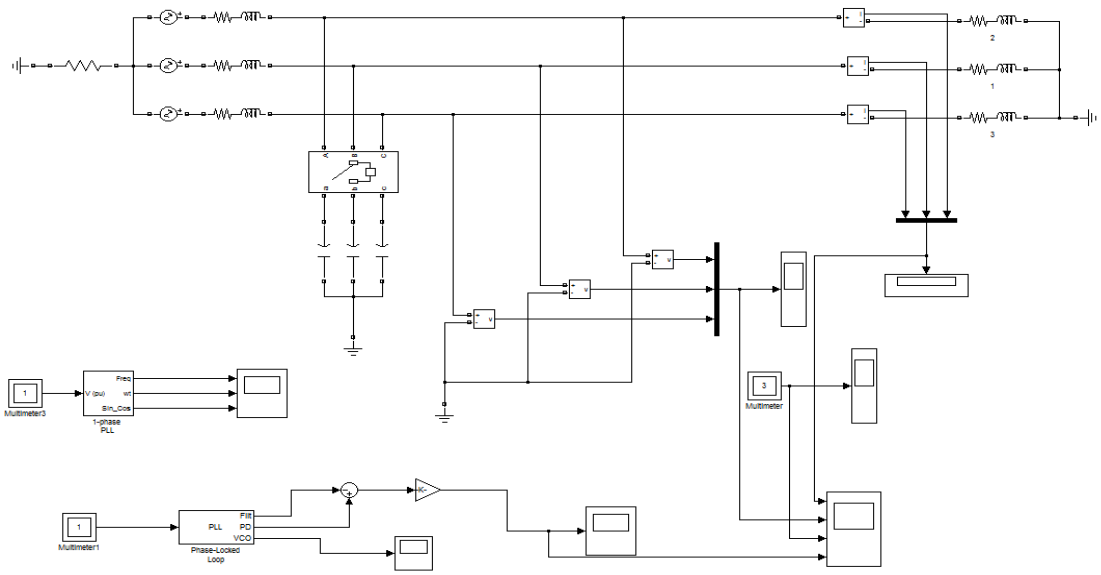


Figure 12 Network Diagram of Capacitor Energizations

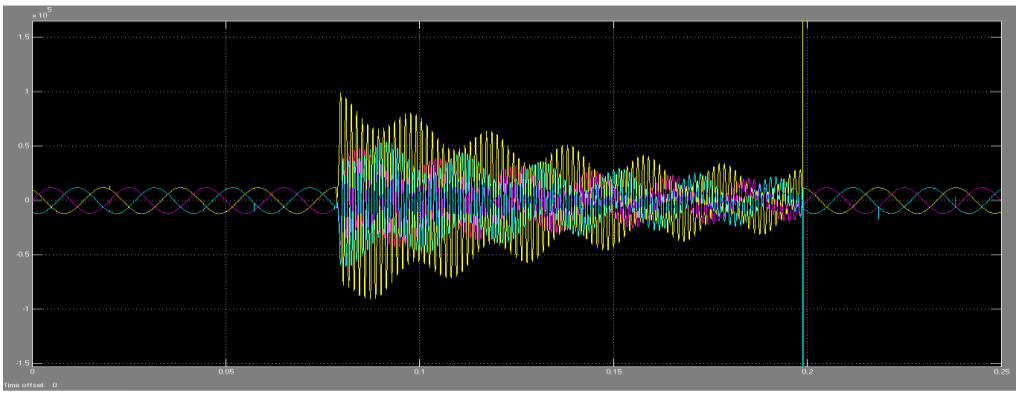


Figure 13 Phase Current Waveform For Capacitor energizations

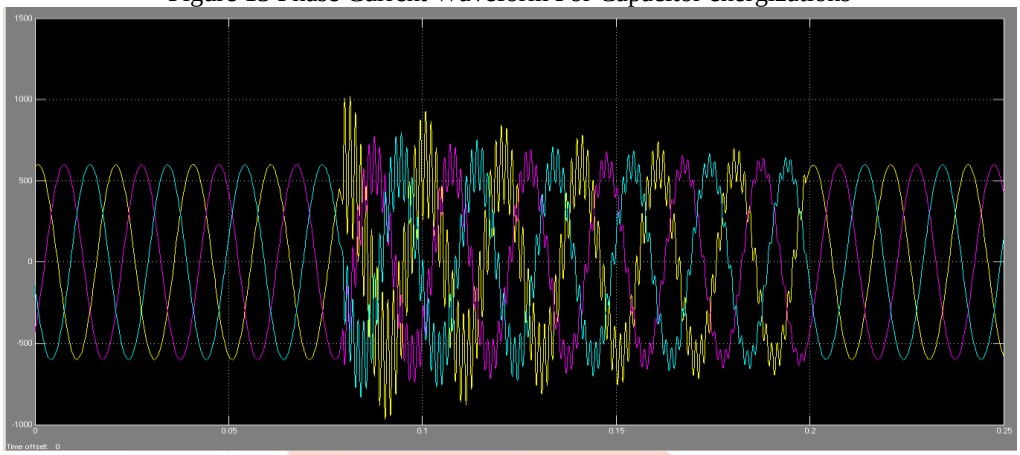


Figure 14 Phase Voltage waveform for capacitor energizations

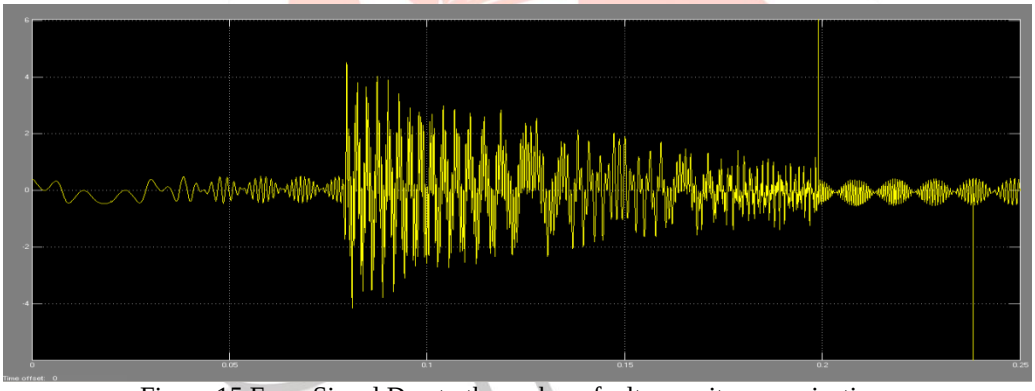


Figure 15 Error Signal Due to three phase fault capacitor energizations

VIII. CONCLUSION

This paper demonstrates that a PLL can be used to determine whether a current transient is due to a fault in the system or due to a switching transient. Capacitor switching has been specifically studied for the large occurrence of these switching transients in the power system. Simulations have been performed using a test system where faults and switching transients have been simulated. For all of these events, a large difference was observed in the error signal of the PLL when a fault or a switching transient was applied. This difference can be used to discriminate faults from switching transients. System have performed three phase fault analysis and simulation &, two phase fault analysis and simulation. The fault due to capacitor energizations is also demonstrated with the help of PLL detection technique.

REFERENCES

[1] K.-H. Hartung and V. Schmidt, "Limitation of short circuit current by an is-limiter," in *Proc. 10th Int. Conf. Electrical Power Quality and Utilisation*, Sep. 2009, pp. 1–4.

[2] CIGRÉ Working Group A3.10, Fault current limiters in electrical medium and high voltage systems, 2003.

[3] A. Wright and P. Newbery, *Electric Fuses*, 3rd ed. London, U.K.: Inst. Elect. Eng., 2004.

[4] M. Stemmle, C. Neumann, F. Merschel, U. Schwing, K.-H. Weck, M. Noe, F. Breuer, and S. Elschner, "Analysis of unsymmetrical faults in high voltage power systems with superconducting fault current limiters," *IEEE Trans. Appl. Superconduct.*, vol. 17, no. 2, pp. 2347–2350, Jun. 2007.

[5] K. Yasuda, A. Ichinose, A. Kimura, K. Inoue, H. Morii, Y. Tokunaga, S. Torii, T. Yazawa, S. Hahakura, K. Shimohata, and H. Kubota, "Research and development of superconducting fault current limiter in Japan," *IEEE Trans. Appl. Superconduct.*, vol. 15, no. 2, pp. 1978–1981, Jun. 2005.
[6] H.-S. Choi, S.-H. Lim, and D.-C. Chung, "Discharge and current limiting characteristics of a superconducting fuse," *IEEE Trans. Appl. Superconduct.*, vol. 15, no. 2, pp. 2360–2363, Jun. 2005.
[7] W. Fei, Y. Zhang, and Q. Wang, in *A Novel Bridge Type FCL Based on Single Controllable Switch*, Bangkok, Thailand, 2007, pp. 113–16.
[8] M. Komatsu, N. Ide, and S. Yanabu, in *Proc. olid-State Current Limiting Switch for Application of Large-Scale Space Power Systems Conf.*, Orlando, FL, 2007, pp. 1471–6.
[9] F. Huang and F. Flett, in *Proc. IGBT Fault Protection Based on di/dt Feedback Control*, Orlando, FL, 2007, pp. 1478–1484.
[10] W. Fei, Y. Zhang, and Z. Meng, in *Proc. Novel Single Self-Turn-off-Device Based FCL for Three-Phase Power Systems Conf.*, Taipei, Taiwan,
2007, pp. 1369–73.
[11] Arceliminator, Rapidelimination of Internal Arcing. ABB, 1999. [Online]. Available: http://www.abb.com
[12] R. Garzon, in *Arc Terminator an Alternative to Arc-Proofing*, Toronto, ON, Canada, 2001, pp. 185–9.
[13] M. Öhrström, "Fast fault detection for power distribution systems," presented at the IASTED Conf. Power and Energy Systems, Marina del Rey, CA, May 13–15, 2002.
[14] Z. Gui-bin and G. Hou-lei, "The current differential and travellingwave based algorithm for ultra high speed hybrid protection," in *Proc. 3rd*
Int. Conf. Electric Utility Deregulation and Restructuring and Power Technologies, Apr. 2008, pp. 1693–1697.
[15] T. Yang, "A method of fast fault detection based on arma and neural network," in *Proc. 6th World Congr. Intelligent Control and Automation*, Jun. 2006, vol. 2, pp. 5438–5441.
[16] A. Sinha and A. Yadav, "Design of hv transmission line protection and control system using wavelet transform for microcontroller application," in *Proc. IEEE Power India Conf.*, Apr. 2006, p. 5.
[17] J. Downes, B. Gwyn, A. Johns, R. Aggarwal, and Z. Bo, "Development and testing of a prototype fault generated noise protection," in *Proc. 6th Int. Conf. Developments in Power System Protection*, Mar. 1997, pp. 87–90, Conf. Publ. 434.
[18] M. Öhrström, "Fast fault detection for peak current limitation based on few samples," presented at the 17th Int. Conf. Electricity Distribution, Barcelona, Spain, May 12–15, 2003.
[19] A. G. Phadke and J. S. Thorp, *Computer Relaying for Power Systems*. New York: Wiley, 1988.
[20] R. E. Best, *Phase-Locked Loops—Design, Simulation and Applications*, 5th ed. New York: McGraw-Hill, 2003.
[21] G. C. Hsieh and J. C. Hung, "Phase-locked loop techniques—A survey," *IEEE Trans. Ind. Electron.*, vol. 43, no. 6, pp. 609–615, Dec.
1996.
[22] A. Timbus, T. Teodorescu, F. Blaabjerg, M. Liserre, and P. Rodriguez, "PLL algorithm for power generation systems robust to grid voltage faults," presented at the Power Electronics Specialists Conf., Jeju, South Korea, 2006.
[23] L. G. B. Rolim, D. R. da Costa, Jr, and M. Aredes, "Analysis and software implementation of a robust synchronizing PLL circuit based on the PQ theory," *IEEE Trans. Ind. Electron.*, vol. 53, no. 6, pp. 1919–1926, Dec. 2006.
[24] T. Emura, L. Wang, M. Yamanaka, and H. Nakamura, "A high-precision positioning servo controller based on phase/frequency detecting technique of two-phase-type PLL," *IEEE Trans. Ind. Electron.*, vol. 47, no. 6, pp. 1298–1306, Dec. 2000.
[25] M. Karimi-Ghartemani and M. R. Iravani, "A signal processing module for power system applications," *IEEE Trans. Power Del.*, vol. 18, no. 4, pp. 1118–1126, Oct. 2003.
[26] M. Karimi-Ghartemani and M. R. Iravani, "A nonlinear adaptive filter for online signal analysis in power systems: Applications," *IEEE Trans. Power Del.*, vol. 18, no. 4, pp. 1118–1126, 2002.
[27] H. Timorabadi and F. Dawson, in Proc. A Three-Phase Frequency Adaptive Digital Phase Locked Loop for Measurement, Control and Protection in Power Systems, Nagoya, Japan, 2007, pp. 183–90