Low Power High Speed Dynamic Latched Comparator

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***Abstract*- Two dynamic latched comparators with DC offset voltage compensation are presented. In this paper, the dynamic latched comparators demonstrates lower offset voltage and higher load drivability, with two different techniques one is on transistor resistance and other is on source degeneration. In these techniques different transistors are added to the input source, by which DC offset voltage and energy is improved. The proposed comparators are designed using 90 nm PTM technology and 1 V power supply voltage in cadence orCAD capture tool. It demonstrates less offset voltage and less sensitivity of delay to decreasing input voltage difference than the conventional double-tail latched type voltage sense amplifier at approximately the same area and power consumption.**

Keywords - Dynamic comparator, Latched comparator, Voltage sense amplifier (SA), Low-offset low-power high-speed

I. INTRODUCTION

Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. However, an input-referred latch offset voltage, resulting from threshold voltage Vth, current factor β (=μCoxW/L) and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of those comparators. A lower input-referred latch offset voltage can be achieved by using the pre-amplifier preceding the regenerative output-latch stage. However, the preamplifier based comparators suffer both from large power consumption for a large bandwidth and from the reduced intrinsic gain with the reduction of the drain-to-source resistance rds due to the continuous technology scaling. With the aforementioned advantages, the dynamic comparators presented is have been widely used. However, since this comparator has one tail transistor which limits the total current flowing through the both of the output branches, it shows strong dependency on speed and offset voltage with different common-mode input voltage Vcom. To mitigate this drawback, the comparator with separated input-gain stage and output-latch stage was introduced in. This separation made this comparator have a lower and more stable DC offset voltage over wide input common-mode voltage (Vcom) ranges and operates at a lower supply voltage (VDD) as well. However, since it requires both Clk and Clkb signals for its operation, high accuracy timing between Clk and Clkb is required because the second stage has to detect the voltage difference between the differential outputs of the first gain stage at very limited time. The comparator from without offset calibration technique resolved this problem by replacing Clkb signal with the differential outputs of the first gain stage. As a result, Clk load was lessened and the input-referred offset was reduced as well since the gain for the output-latch stage was improved. However, the current drivability of the output load was weakened (and hence increased delay) because Clkb signal was replaced with the output signal of the first gain stage that has a slower edge rate than Clkb, showing a slow exponential decaying shape, and the maximum drive current for each output was reduced to half of the single output tail current comparing to the comparator in. In this paper, we present two new dynamic latched comparators which shows lower input-referred latch DC offset voltage and higher load drivability than the conventional dynamic latched comparators. The remaining sections of the paper are organized as follows. Section II provides the operation principle of the proposed comparators and section III the performance comparisons with the previous works, section IV followed the conclusion.

II. PROPOSED CIRCUITS

In this paper two comparators are proposed which are based on source degeneration and on transistor resistance technique. These two proposed comparators are the modification of double-tail latch type voltage sense amplifier. By using these techniques result of the comparators are improved with respect to dc offset voltage, delay (rising and falling), energy, number of transistors and their total width.

Proposed comparator 1

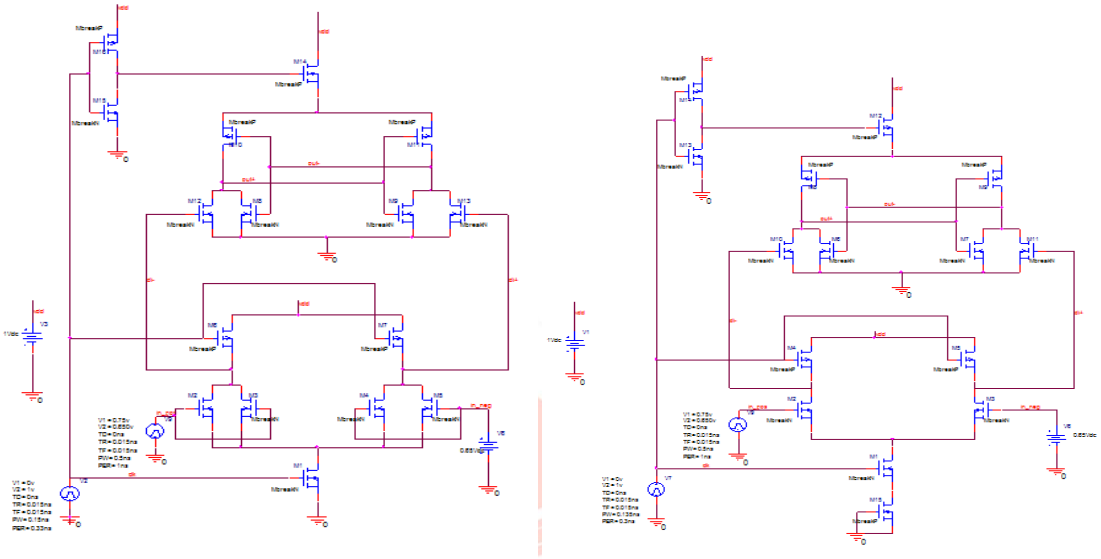
Circuit Diagram of Proposed Comparator 1 is shown in Figure 4.1. This circuit mainly is a modified version of the comparator 2. The on transistor resistance technique is used, in which two transistors are added parallel to the input of the circuit in which input is common. This technique has so many advantages over the all three previous comparators which are already mentioned above. It provides simpler biasing and higher linearity. Here our main purpose is to reduced the offset voltage and delay for which comparator has fast speed at low power.

Propose comparator 2

Circuit Diagram of Proposed Comparator 1 is shown in Figure 4.5. This circuit mainly is a modified version of the comparator 2. The on transistor resistance technique is used, in which one transistor is added serially with the tail transistor of the circuit in which input is grounded. This technique has so many advantages over the all three previous comparators which are already mentioned above. It provides simpler biasing and higher linearity. Here our main purpose is to reduced the offset voltage and delay for which comparator has fast speed at low power.

Operation

The circuit operates similar to other comparators with a precharge phase and evaluation phase. During the precharge phase (clk=0), transistors M4 and M5 are on and pre-charge the Di nodes to VDD, which in turn causes M10 and M11 to discharge the output nodes to ground (so there is no need for dedicated reset transistors at the output nodes).



(a) (b)

Figure 1 (a) proposed comparator 1. (b) Proposed comparator 2.

During the evaluation phase (clk=vdd), in this clk signal starts to rise, the tail transistors M1, M15 of the differential pair M2, M3 and M14 are turned on. The differential pair will discharge the Di nodes. At the Di nodes, the common-mode voltage then drops monotonically with a rate defined by IM9/CDi and on top of this, an input dependent differential voltage ΔVDi will build up. The intermediate stage formed by M10 and M11 passes ΔVDi to the cross-coupled inverters and also provides additional shielding between the input and output, with less kickback noise as a result. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Di nodes is no longer high enough forM10 and M11 to clamp the outputs to ground. The ideal operating point (Vcm) and the timing of the various phases can be tuned with the transistor sizes.

In this proposed comparator 1 two transistors M3, M5 are added parallel to the input transistors M2 and M5, by which Rload is increased and offset voltage is reduced, that's why offset voltage of this comparator is less than the dual tail latch type sense amplifier and also its delay and energy is reduced. This comparator is much better than other previous comparators. Proposed comparator 1's result analysis is shown below.

In this proposed comparator 2 one transistor M15 is added in series to the tail transistor, by which Rload is increased and offset voltage is reduced, that's why offset voltage of this comparator is less than the dual tail latch type sense amplifier as well as all the previous dynamic comparators and also its delay and energy is reduced. This comparator is much better than other previous comparators.

$$A_v = \frac{R_L}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

III. COMPARISON OF PREVIOUS AND PROPOSED COMPARATORS

	Number of transistors	∑(width) µm	DC offset voltage (mv)	Energy / Decision (fJ)	Delay (Ps)	
					Rising	Falling
Comparator 2	14	13.6	551.335	48.241	72.276	69.977
Comparator 3	15	13.5	513.428	44.914	89.316	77.074
Comparator 4	19	13.9	499.454	48.112	48.138	68.268

Proposed comparator 1	16	13.6	548.277	16.877	41.788	19.062
Proposed comparator 2	15	13.6	436.392	28.973	39.350	17.102

IV. CONCLUSION

New dynamic comparators using on transistor resistance and source degeneration technique which shows higher speed, lower power dissipation than the conventional dynamic latched comparators has been proposed & targeted for ADC application. The results are simulated in Cadence® OrCAD capture with 90nm PTM technology. The proposed designs are the modification of double tail latch type voltage sense amplifier in which we used on transistor resistance and source degeneration techniques, in which transistors are added to the input stage of the comparator. The proposed structure shows significantly lower power dissipation, higher speed compared to the dynamic comparators present in the literature. The transistor count in the proposed comparator is lesser or equal to among all the comparators analyzed.

V. REFERENCES

[1] Heung Jun Jeon, Yong Bin Kim and Minsu Choi, "offset voltage analysis of dynamic latched comparator," IEEE J. Circuits and Systems (MESCAS), vol. 54, pp. 1-4, August 2011.
[2] Pedro M. Figueiredo and Joao C.Vital, "Kickback noise reduction techniques for CMOS latched comparators", IEEE J. circuits and systems-II, vol. 53, pp. 537-540, July 2006.
[3] Heung Jun Jeon, Yong Bin Kim, "A CMOS low power, low offset, and high speed fully dynamic latched comparator," IEEE international, soc conference, pp. 285-288, September 2010.
[4] Chung-Hsun Huang and Jinn-Shyan Wang,"High performance and power efficient CMOS comparators", IEEE J. solid states circuits, vol. 38, pp. 254-262, February 2003.
[5] Moni D.J. and Jisha P,"High speed and low power dynamic latch comparator", IEEE international, devices circuits and systems conference, pp. 259-263, March 2012.
[6] Heung jun joen and yong bin kim, " A novel low power, low offset, and high speed CMOS dynamic latched comparator", Springer Science-analog integratd circuit and signal processing, vol. 70,pp. 337-346, March 2012.
[7] Raja Mohd. Noor Hafizi Raja Daud, Mamun Bin Ibne Reaz and Labonnah Farzana Rahman, " Design and analysis of low power and high speed dynamic latch comparator in 0.18um CMOS process", International journal of information and electronics engineering, vol. 2, pp. 944-947, November 2012.
[8] N. Naga Sudha, "High Speed and Low Power Dynamic Latched Comparator for PTL Circuit Applications", International Journal of Computer Science and Information Technologies, Vol. 3 ,pp. 2982 – 2991, March 2012.
[9] N.Naga sudha, V. Narasimha Nayak,Dr. Fazal Noor Basha, S. Rahil Hussain, "High Speed and Low Power Dynamic Latched Comparator for Air Craft Application", International Journal of Engineering Research and Applications (IJERA),Vol. 2 , pp.1301-1312, May 2012.
[10] Sweta Sahu & AJjay Vishwkarma, "Implementation of a low kickback noise latched comparator for high speed analog to digital design in 0.18", International Journal of Electronics, Communication & Instrumentation Engineering Research and Development (IJECIERD),Vol. 2, pp. 43-56, December 2012.
[11] Mayank Nema, Rachna Thakur, "Design of Low-Offset Voltage Dynamic Latched Comparator", IOSR Journal of Engineering, Vol. 2, pp. 585-590, April 2012.
[12] Sandeep K. Arya, Neelkamal, " A comparative study of dynamic latch comparator", International Journal of Advances in Electronics Engineering, vol.1, pp. 313-317, December 2013.
[13] Carlos J Solis, Gladys O. Ducoudray, "High Resolution Low power 0.6µm CMOS 40MHz Dynamic Latch Comparator," Circuits and Systems (MWSCAS), 53rd IEEE International , Department of Electrical and Computer Engineering, pp. 1045-1048, August 2010.
[14] Zhaohui Huang, PeixinZhong , "An adaptive analog-to-digital converter based on low-power dynamic latch comparator", Electro Information Technology, IEEE International conference, pp. 6, May 2005.
[15] Sougata Ghosh, Samraat Sharma, " Design of a novel high speed Dynamic comparator with low power dissipation for high speed ADCs", International Journal of Electronics and computer science Engineering, vol.2, pp. 411-426, December 2011.