Low power explicit type pulse-triggered FF (P-FF) design at Minimum Transistor

[1]Shashank Uniyal, [2]Rajeev Kumar, [3]Krishna Chandra, [4]Vishal Ramola
[1&3]M.Tech. Student of VLSI Design Department, UTU Dehradun, UK India
[2]Assist. Prof. Electronics Department UCST Dehradun, UK India [2]
[4]Assist. Prof. VLSI Design Department, UTU, Dehradun, UK India[4]

***Abstract* - The Flip flop circuit is one of the major component in VLSI Low power circuits. In this paper we modified (proposed) a Low power explicit type pulse triggered flip-flop (P-FF) design based on single feed through scheme. The modified design successfully solves the long discharging path problem in conventional flip flop designs to achieve better speed, power performance and avoids unnecessary Q_fdbk transistor. We also design 4-bit Shift Resistor using modified P-FF. The performance has been investigated using 90nm Technology at 1.8 voltage and evaluated by the comparison of the simulation result obtain from TSPICE.**

***Index terms* - Flip Flop-Ep-DCO, CDFF, Static SDFF, MHLFF, Propagation Delay, Power Consumption Power Delay Product**

I. INTRODUCTION

Low power design is the need of today's integrated systems. The low power design is also needed for the applications operated by batteries such as pocket calculators, wrist watches, mobile phones, laptops etc. Since the battery technology available does not advance at the same rate as the microelectronics technology, IC designers have encountered more constraints: high speed, small silicon area, and at the same time, low power dissipation. Hence, the research of establishing high performance adder cells is becomes feverish. The design of flip flop which forms the basic building blocks of all digital VLSI circuits has been undergoing to minimizing the transistor, minimizing the power consumption and increasing the speed [1-2].

Besides the speed advantage, its circuit simplicity is additionally helpful to lowering the ability consumption of the clock tree system. A P- FF consists of a generator for generating strobe light signals and a latch for knowledge storage. Since triggering pulses generated on the transition edges of the clock signal are terribly slim in pulse dimension, the latch acts like Associate in nursing edge-triggered FF. The circuit complexness of a P-FF is simplified since only 1 latch, as against 2 utilized in standard master–slave configuration, is needed. P-FFs additionally enable time borrowing across clock cycle boundaries and have a zero or maybe negative setup time. P-FFs are therefore less sensitive to clock noise [3].

In this paper a Low power Pulse Triggered Flip Flop is modified that has reduced the number of transistors and avoids unnecessary internal node transitions, as well as reduce power consumption and delay compared to conventional P-FF (like as Ep-DCO, SCCER Previous EPTL).

The paper is organized as follows: in Section II, previous work is reviewed. Subsequently, in section III, the modified Low power explicit type pulse triggered flip-flop (P-FF) design are presented. In section IV, the simulation results are given and discussed. The comparison and evaluation for modified and existing designs are carried out. Finally a conclusion will be made in the last section.

II. PRELIMINARIES

Conventional Explicit Type P-FF Designs

Conventional P-FFs, in terms of pulse generation, can be classified as an explicit type, the pulse generator and the latch are separate [6]. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shares a group of FFs. We will thus focus on the explicit type P-FF designs only. To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(a) shows a classic explicit P-FF design, named data-close to- output (ep-DCO) [6]. It contains a NAND-logic-based pulse generator and a semi dynamic true-single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node *X*. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node *X* is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been designed [7]–[8].

Fig. 1(b) shows a conditional discharged (CD) technique [9]. An extra nMOS transistor MN3 controlled by the output signal Q_fdbk is employed so that no discharge occurs if the input data remains "1".

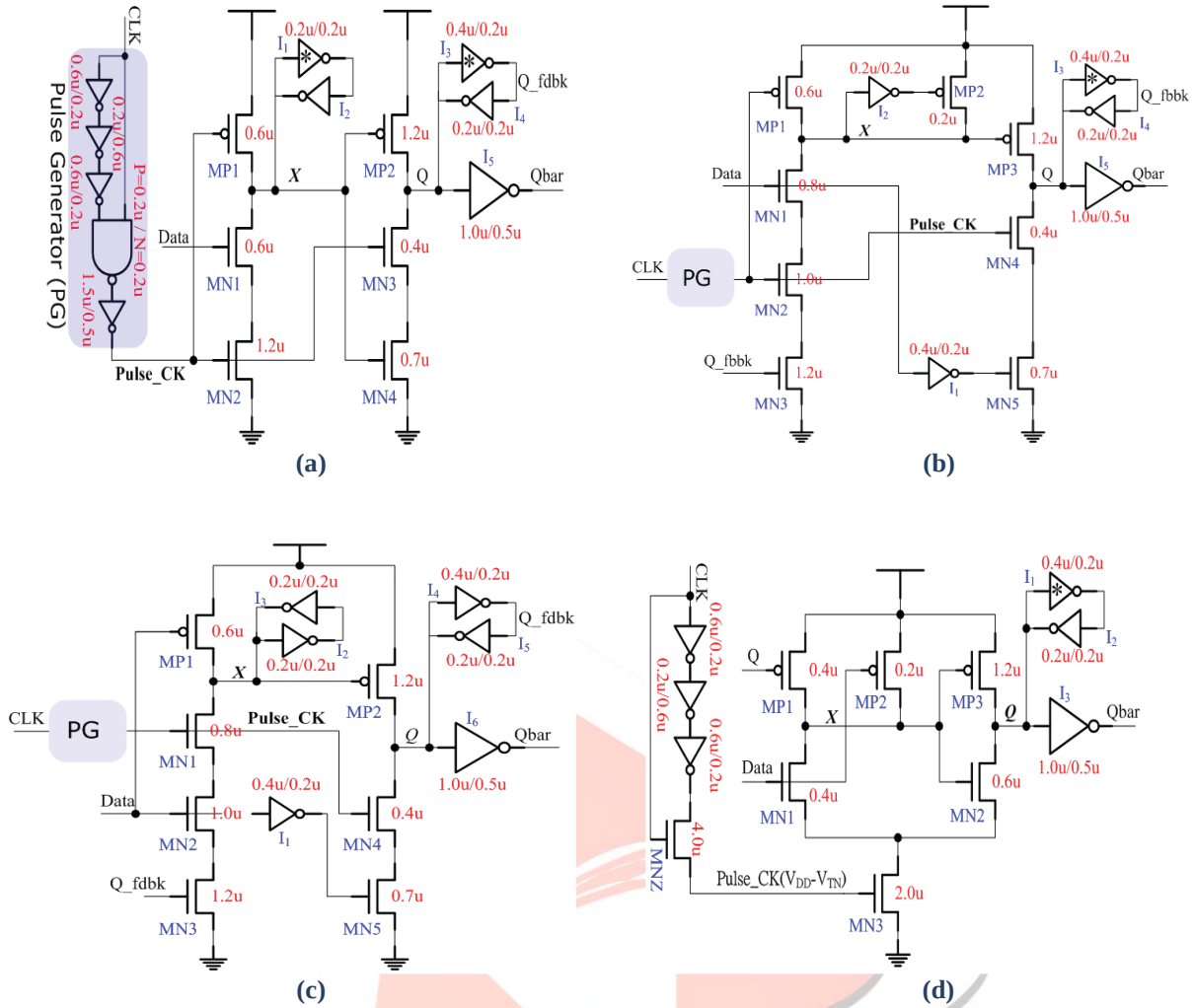

Figure.1 Conventional P-FF designs. (a) ep-DCO [7]. (b) CDFF [6] (c) Static-CDFF [17]. (d) MHLFF [19].

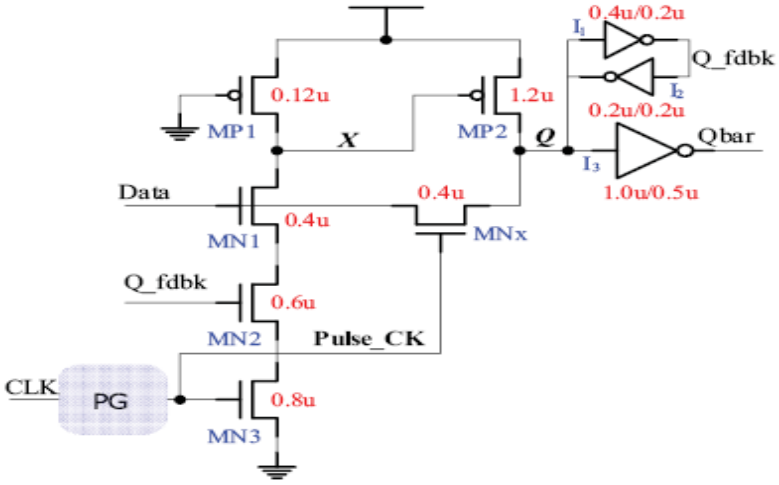

Figure. 2. Schematic of the proposed P-FF design.

Recalling the five circuits reviewed in Section II-A, they all encounter the same worst case timing occurring at 0 to 1 data transitions. Referring to Fig. 3 (proposed), Q-fdbk signal is not use modified circuit. The modified design adopts a signal feed-through technique to improve this delay. Similar to the conventional design, the modified design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the modified design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node *X* can be saved.

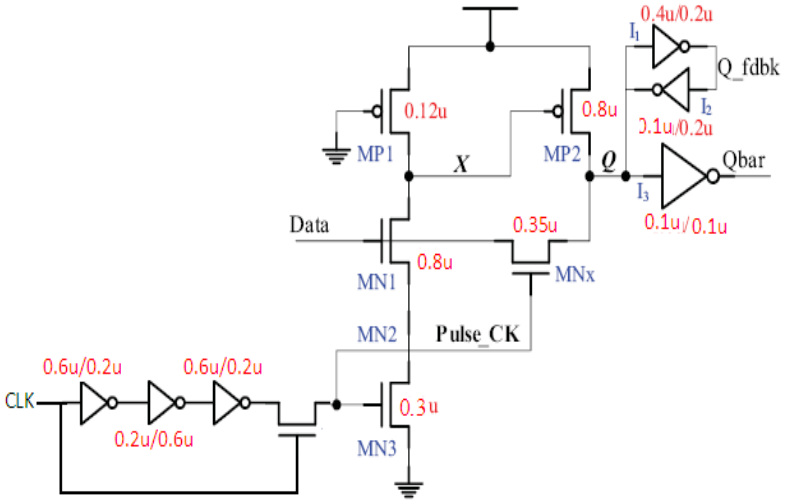

Figure 3. Modified (Proposed) DFF

In addition to the circuit simplicity, this approach also reduces the load capacitance of node *X* [4], [5]. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly. Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during "1" to "0" data transitions. Compared with the latch structure used in SCDFF design, the circuit savings of the modified design include a charge keeper (two inverters), a pull-down network, and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feed through. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. In comparison with modified design to the other FF designs such as ep-DCO, CDFF, and SCDFF, P-FF(Fig.2) design shows the most balanced delay behaviors.

The modified flip flop designs are explained as follows. When a clock pulse arrives, if no data transition occurs, i.e., the input data and node Q are at the same level, on current passes through the pass transistor MNx, which keeps the input stage of the FF from any driving effort. Therefore, no signal switching occurs in any internal nodes. On the other hand, if a "0" to "1" data transition occurs, node X is discharged to turn on transistor MP2, which then pulls node Q high. Referring to Figure. 1(b), this corresponds to the worst case timing of the FF operations as the discharging path conducts only for pulse duration. However, with the signal feed through scheme, a boost can be obtained from the input source via the pass transistor MNx and the delay can be greatly shortened. Although this seems to burden the input source with direct charging or discharging responsibility, which is a common pitfall of all pass transistor logic, the scenario is different in this case because MNx conducts only for a very short period. Referring to Fig. 1(c), when a "1" to "0" data transition occurs, transistor MNx is likewise turned on by the clock pulse and node Q is discharged by the input stage through this route. Unlike the case of "0" to "1" data transition, the input source bears the sole discharging responsibility. Since MNx is turned on for only a short time slot, the loading effect to the input source is not significant. In particular, this discharging does not correspond to the critical path delay and calls for no transistor size tweaking to enhance the speed. In addition, since a keeper logic is placed at node Q, the discharging duty of the input source is lifted once the state of the keeper logic is inverted.

III. SHIFT REGISTERS

Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flops are driven by a common clock. There are different kinds of shift registers.

Parallel in Parallel out Shift Register

For parallel in parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. The following circuit is a 4-bit parallel in parallel out shift register constructed by proposed EPTL D flip-flops and shown in figure. 4.

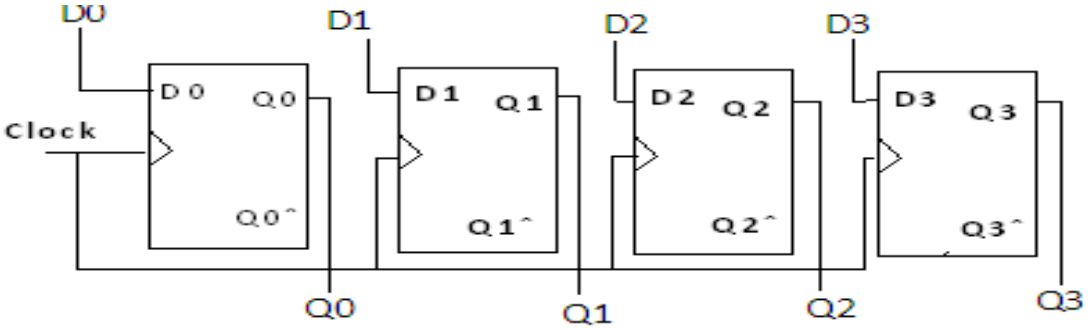

Figure:4. 4-Bit Parallel in Parallel out Shift Register

VI. SIMULATION RESULT

The comparison of result summarizes some important performance indexes of these P-FF designs as shown in Table 1. These include transistor count, Area, D to Q & D to Qbar propagation Delay, Power consumption and power delay product in 90-nm technology.

Table.1

Flip Flop	No. of Transistor	Propagation Delay of Q (n)	Propagation Delay of QBAR(n)	Power Consumption (f)	PDP of Q ($)	PDP of QBAR (&)
Ep-DCO	28	22.51	41.06	31.1	700.06	1276.96
CDFF	30	22.51	22.51	11.4	256.61	256.61
Static-CDFF	31	22.51	40.96	13.7	308.38	561.15
MHLFF	19	22.46	25.05	49.8	1118.50	1247.49
P-FF	19	22.40	25.50	15.18	340.03	387.09
Proposed P-FF	18	22.50	25.50	8.8	198	224.4
Units : $=n*f, &=n*f						

To evaluate the performance, flip flops discussed in this paper are designed using 180-nm CMOS technology. All simulations are carried out using Tanner Tools at 330GHz clock frequency is shown in figure 5, 6,7 & 8. Modified (proposed) Flip-flop based parallel in Parallel out Shift Register Schematic designed.

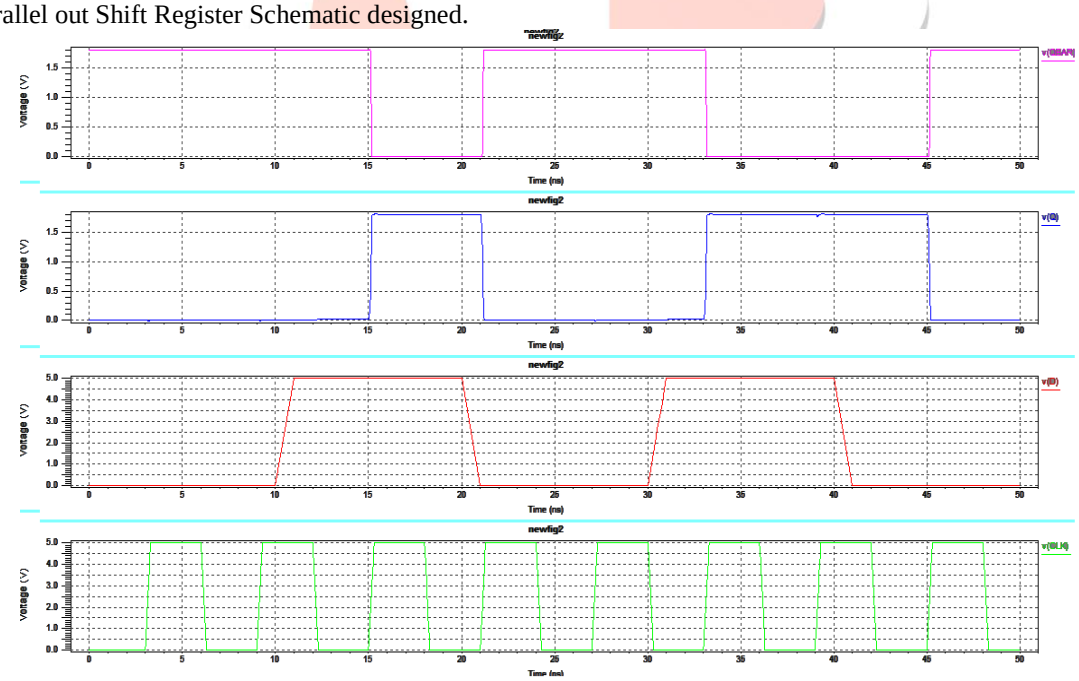

Figure: 5.Waveform of modified (proposed) Flip Flop

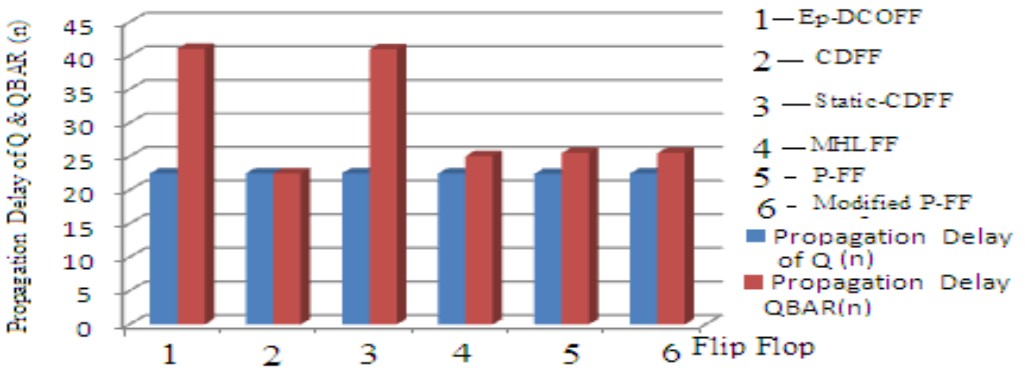

Figure 6. Propagation Delay of Q & QBAR

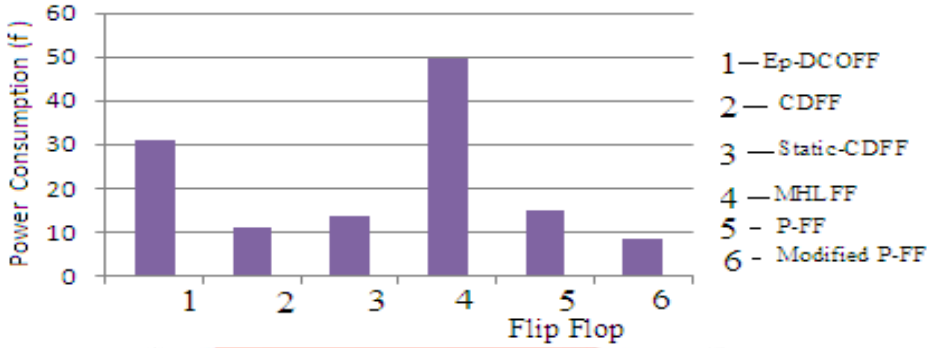

Figure 7.Power Consumption of flip flops

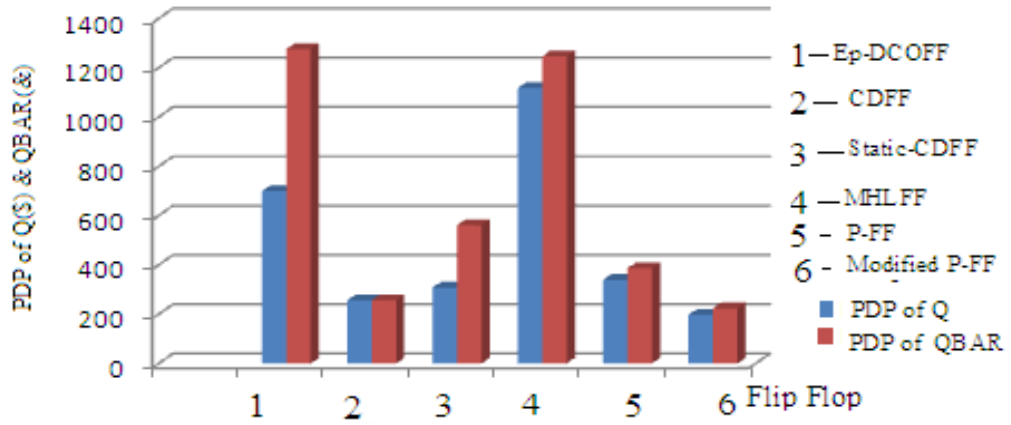

Figure 8.Power Consumption of flip flops

CONCLUSION

In this paper, we presented a flip flop design by employing a modified (proposed) explicit type pulse triggered flip flop (P-FF) structure incorporating a mixed design style consisting of pass transistor and pseudo-nMOS logic. The flip flop (P-FF) was to provide a signal feed through from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time, avoids unnecessary Q_fdbk transistor and enhance both power and speed performance. Simulation results indicate that the modified design excels rival designs in performance indexes such as power, D-to-Q delay, and PDP.

REFERENCES

[1]A. G. M. Strollo, D. De Caro, E. Napoli, and N. Petra, "A novel high speed sense-amplifier-based flip-flop," IEEE Trans. Very Large Scale Integer. (VLSI) Syst., vol. 13, no. 11, pp. 1266–1274, Nov. 2005.

[2] C. K. Teh, M. Hamada, T. Fujita, H. Hara, N. Ikumi, and Y. Oowaki, "Conditional data mapping flip-flops for low power and high-performance systems," IEEE Trans. Very Large Scale Integer. (VLSI) Systems, vol. 14, pp. 1379– 1383, Dec. 2006.

[3] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors, " in Proc. ISPLED, 2001, pp. 207–212.

[4] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low power clocking scheme using energy recovery and clock gating," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 1, pp. 33–44, Jan. 2009.

[5] P. Zhao, J. McNeely, S. Venigalla, G. P. Kumar, M. Bayoumi, N. Wang, and L. Downey, "Clocked-pseudo-NMOS flip-flops for level conversion in dual supply systems," IEEE Trans. Very Large Scale Integr. (VLSI)
Syst., vol. 17, no. 9, pp. 1196–1202, Sep. 2009.
[6] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De, "Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in Proc. ISPLED, 2001, pp. 207–212.
[7] M.-W. Phyu, W.-L. Goh, and K.-S. Yeo, "A low-power static dual edge triggered flip-flop using an output-controlled discharge configuration," in Proc. IEEE Int. Symp. Circuits Syst., May 2005, pp. 2429–2432.
[8] Y.-T. Hwang, J.-F. Lin, and M.-H. Sheu, "Low power pulse triggered flip-flop design with conditional pulse enhancement scheme," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp. 361–366, Feb. 2012.
[9] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 12, no. 5, pp. 477–484, May 2004.
[10] T. Indira, Ch. Jayaprakash"A Pulse Triggered flip flop using conditional pulse enhancement method for low performance application" International Conference on Recent Trends In Science And Technology-RTET-29th Sep 2013 – ISBN: 987-9381361-18-9.
[11] Y.-H. Shu, S. Tenqchen, M.-C. Sun, and W.-S. Feng, "XNOR-based double-edge-triggered flip-flop for two-phase pipelines," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 53, no. 2, pp. 138–142, Feb. 2006.
[12] V. G. Oklobdzija, "Clocking and clocked storage elements in a multigiga-hertz environment," IBM J. Res. Devel., vol. 47, pp. 567–584, Sep.2003.
[13] S. H. Rasouli, A. Khademzadeh, A. Afzali-Kusha, and M. Nourani, "Low power single- and double-edge-triggered flip-flops for high speed applications," IEE Proc. Circuits Devices Syst., vol. 152, no. 2, pp. 118–122, Apr. 2005.
[14] K. Chen, "A 77% energy saving 22-transistor single phase clocking D-flip-flop with adoptive-coupling configuration in 40 nm CMOS," in Proc. IEEE Int. Solid-State Circuits Conf., Nov. 2011, pp. 338–339.
[15] N. Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power- efficient dual-edge clocking," in *Proc. Int. Symp.Low-Power Electron. Design*, Monterey, CA, Aug. 12–14, 2002, pp. 56–59