p-mean Model impact on VLSI Placement

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***Abstract*- In this paper we compare the impact of of p-mean Half-perimeter wirelength (HPWL) model on analytical placement of VLSI. against logarithm-sum-expontial (LSE) wirelength model, weighted average(WA) [3]and (γ,p)[8] wirelength models.. Deployment of the wirelength model in analytical placement engine produces 12%, 10% and 1% shorter wirelength than widely used LSE and recently proposed weighted average(WA) [3]and (γ,p)[8] wirelength models.**

***Keywords*- VLSI; placement; wirelength; simulated annealing**

I. INTRODUCTION

Placement problem of vlsi can be solved in varieties of ways such as mincut approach, simulated annealing approach and analytical placement approach. Analytical placer uses HPWL objective function to place blocks optimally within the chip. Various smooth HPWL models including LSE, WA[3] and *(γ,p)* models are available in the literature.
The art of analytical placers include Aplace [5], mPL6 [2], FastPlace [10], NTUPlacer [1], Kraftwerk[9] and SimPL[6]. Among those placers, the placers that use HPWL objective are Aplace [5], mPL6 [2],NTUPlacer [1]. The model p-mean for HPWL discussed in [2] takes less computational time for two variables function compare to other wirelength models.The authors in [9] also discussed the error bounds, convergence properties and numerical stability of this model. But its impact on analytical placement was not discussed. Since p-mean model is compuationally efficient, thus it is interesting to study its impact on analytical placement as oppose to the existing art of wirelength models. In this paper, we have studied the impact of p-mean wirelength model and compared its placement result with LSE, WA and *(γ,p)* models. Our experimental results on ISPD 2004 benchmarks ensure the p-mean model achieves 12%, 10% and 1 % shorther wirelength than LSE, WA and *(γ,p*) models respectively. The rest of the paper organization as follows. Section II briefs HPWL formulation and existing wirelength models. Analytical formulation of placement problem is given in Section III. Section IV highlights computer simulation results and finally the conclusions are offered in Section V.

II. HPWL FORMULATION AND REVIEW OF EXISTING WIRELENGTH MODELS

The circuits of a placement are denoted by a hypergraph H(V, E), where V is the set of fixed or movable blocks or pads, and E is a set of nets. If we denote the bottom left corner of a block in chip by (xi, yi)($1 \le i \le |V|$), then the HPWL of a net e is given by

$$HPWL_e = \max_{i\in e}\{x_i\} - \min_{i\in e}\{x_i\} + \max_{i\in e}\{y_i\} - \min_{i\in e}\{y_i\} \quad (1)$$

Then the total HP W L of a placement is given by sum of the HPWL of all nets.

$$HPWL = \sum_{e\in E} HPWL_e \quad (2)$$

A. Review of Existing HPWL Wirelength Models

The wirelength function given by (Eqn(1) and (2)) is hard to minimize due to the presence of max and min functions, as these functions are not differentiable. Analytical placer reformulates HPWL by replacing these functions by their smooth approximations before the placement problem is solved by non linear mathematical programming techniques. There are many smooth approximations for max and min functions. Some of them are discussed below.

1. Logarithm-Sum-Exponential Wirelength Model(LSE)[11]

For real parameter $\gamma \to 0$, smooth approximation to HPWL of a net e is given by

$$LSEWL_e = \gamma \ln(\sum_i e^{x_i/\gamma}) + \gamma \ln(\sum_i e^{-x_i/\gamma}) + \gamma \ln(\sum_i e^{y_i/\gamma}) + \gamma \ln(\sum_i e^{-y_i/\gamma}) \quad (3)$$

This is a popular wirelength model for HPWL and is used by analytic placers discussed in [1], [5], [2].

2. Weighted Average Wirelength Model (WAWL)[3]

If x and y coordinates of blocks of a net e are denoted by xe and ye respectively, then the weighted average HPWL of a net is given by

$$WAWL_e = (X_{\max}(x_e) - X_{\min}(x_e)) + (Y_{\max}(y_e) - Y_{\min}(y_e)) \quad (4)$$

Where

$$X_{\max}(x_e) = \frac{\sum_{v_i \in e} x_i \exp(x_i / \gamma)}{\sum_{v_i \in e} \exp(x_i / \gamma)}$$

$$X_{\min}(x_e) = \frac{\sum_{v_i \in e} x_i \exp(-x_i / \gamma)}{\sum_{v_i \in e} \exp(-x_i / \gamma)}$$

$$Y_{\max}(y_e) = \frac{\sum_{v_i \in e} y_i \exp(y_i / \gamma)}{\sum_{v_i \in e} \exp(_i / \gamma)}$$

$$Y_{\min}(y_e) = \frac{\sum_{v_i \in e} y_i \exp(-y_i / \gamma)}{\sum_{v_i \in e} \exp(-y_i / \gamma)}$$

and $\gamma \to 0$.

The authors in Theorem 2[3], proved that the errors upper bounds of WAWL model were less than the errors upper bounds of LSE wirelength model.

3. (γ, p)-**Wirelength Model[8]** If x and y coordinates of blocks of a net e are denoted by x_e and y_e respectively, then for real parameters $\gamma \to 0$, $p \to \infty$, (γ, p)-wirelength model of a net *e* is given by

$$WAWAL = (X^{(\gamma,p)}(x_e) - X^{(-\gamma,-p)}(x_e) + (Y^{(\gamma,p)}(y_e) - Y^{(-\gamma,-p)}(y_e)) \quad (5)$$

Where

$$X^{(\gamma,p)}(x_e) = \frac{\sum_{v_i \in e} x_i^{\,p} \exp(x_i / \gamma)}{\sum_{v_i \in e} x_i^{\,p-1} \exp(x_i / \gamma)}$$

$$X^{(-\gamma,-p)}(x_e) = \frac{\sum_{v_i \in e} x_i^{-p} \exp(-x_i / \gamma)}{\sum_{v_i \in e} x_i^{-p-1} \exp(-x_i / \gamma)}$$

$$Y^{(\gamma,p)}(y_e) = \frac{\sum_{v_i \in e} y_i^{p} \exp(y_i / \gamma)}{\sum_{v_i \in e} y_i^{p-1} \exp(y_i / \gamma)}$$

$$Y^{(-\gamma,-p)}(y_e) = \frac{\sum_{v_i \in e} y_i^{-p} \exp(-y_i / \gamma)}{\sum_{v_i \in e} y_i^{-p-1} \exp(-y_i / \gamma)}$$

The authors in Theorem 5[8], proved that the errors upper bounds of (γ, p)-wirelength model were less than the errors upper bounds of WAWL model and LSE wirelength model. Interestingly, (γ, p)-wirelength model reduces to WAWL model, when p = 1.

4. p-mean Wirelength Model[]

Let $\underline{x_e} = (x_1, x_2, \ldots x_n)$ and $y_e = (y_1, y_2, \ldots y_n)$
be x and y be coordinates of net e respectively and E is the set of nets. Then for real $p \to \infty$, total HPWL if the circuit is given by

$$\sum_{e \in E} (X^{p}(x_e) - X^{-p}(x_e) + Y^{p}(y_e) - Y^{-p}(y_e))$$

Where $X^p(x_e) = \frac{\sum_{i=1}^{n} x_i^p}{\sum_{i=1}^{n} x_i^{p-1}}$ is the x-mean of x-cordinates of net 'e' and this expression corresponds to max $(x_1, x_2, \ldots x_n)$. For min $(x_1, x_2, \ldots x_n)$, one has to replace p by –p.
Similarly max max and min of $(y_1, y_2, \ldots y_n)$ can be defined.

III ANALYTICAL FORMULATION OF PLACEMENT PROBLEM

The mathematical formulation of global placement problem as follows.

For a given circuit $G = (V, E)$, let $V = \{v_1, v_2, \ldots, v_n\}$ be a set of vertices and $E = \{e_1, e_2, \ldots, e_n\}$ be a set of nets. Let x_i and y_i be the x and y co-ordinates of the center of block v_i and a_i be the area of block v_i. In the circuit we might have some preplaced blocks and remaining are movable blocks. The placement problem is to find optimal positions of movable blocks within the chip so that blocks do not overlap and total wirelength is minimum. The global placement problem with non-overlapping constraint is given by:

Minimize $W(x, y)$
such that
$$D_b(x, y) \leq M_b \quad (6)$$

for each bin b. Where $W(x,y)$ is the half perimeter wirelength function, $D_b(x, y)$ is the potential or density function which represents the total moveable area of blocks in bin b. M_b is the maximum movable area in the bin b such that

$$M_b = t_{density}(w_b h_b - P_b) \quad (7)$$

The target density is the user defined value for each bin and P_b is the preplaced base potential equal to the area of the preplaced block in bin b. Since $W(x, y)$ is nonsmooth and nonconvex, smooth approximations to wirelength function are used to solve the optimization problem by nonlinear optimization techniques. In this work, the HPWL is replaced by LSE, WA, (γ, p)-mean and p-mean wirelength functions, density function is replaced by bell shaped function discussed in [1]. Then using l_2 penalty mehod,

conjugate gradient method for local search and mulilevel placement algorithm discussed in [1] the global placement problem is solved. After Global placement, look ahead legalization and detail placement are used to produce the final placement. For detail discussion on legalization and detail placement, the work reported in [1] may be referred.

IV. IMPLEMENTATION AND RESULTS

A. HPWL Accuracy

For comparing accuracy of approximations of various wirelength models we choose circuits from IBM ISPD 2004 benchmark suite. The number of cells in this benchmark varies from 12K to 210K. We obtain global placement for each circuit using widely used placement tool NTUPlacer [1]. We read the placement result and calculate the HPWL for each net. To compare the different approximation schemes, we picked $\gamma = 0.02$, $\beta = 60$ [7] (satisfies the condition $K\gamma = \beta\gamma - 1 = 1.2 - 1 = 0.2 > 0.177$) and $p = 50$. Here p is chosen as inverse of γ. We then scaled down the chip dimension to 4×4, calculate the approximated HPWL and scale it back to the original dimensions by multiplying the result with $\frac{W+H}{8}$. The results from ABSWL, LSEWL, WA, (γ,p)-mean and pmean approximations are presented in columns 3, 4, 5, 6 and 7 of Table I. It is evident from the table that (γ, p)-mean and our p-mean wirelength models give closest approximation to HPWL compared to the other schemes with an average less than 5% and 13% absolute error respectively, in the total wirelength.

B. Performance of Wirelength Models on Analytical Placement

In this subsection, we use International Symposium on Physical Design(ISPD 2004) placement benchmark circuits to study the performance of (LSE, WA, (γ, p)-mean and pmean) wirelength models on analytical placement. We implemented all these wirelength models in C++ and integrated them into NTUPlacer[1], which is a multilevel analytical placer based on nonlinear programming techniques. Note that the NTUPlacer source code available online does not use Whitespace allocation procedure discussed in [1]. All experiments were conducted on the same PC with intel Core Duo CPU 2.20 GHz and 1 GB memory. For p-mean we set $p = 150$. For LSE, WA and (γ, p)-mean wirelengths we set $\gamma = 0.001\times$ chip width and $p = 150$. Thogh NTUPlacer[1] uses $\gamma = 1\%\times$ chip width, we smaller values for better accuracy. For fair comparison we did not do any manual parameter tuning for an individual circuit. Table II shows the results of HPWL and run times for benchmark circuits by different wirelength models. There are following observations that can be drawn.

1) Compared to LSE, our p-mean achieves 12% shorter wirelength and is 0.1× slower.

2) Compared to WA, our p-mean acheives 10% shorter wirelength and is 0.1× slower.

3) Compared to (γ, p)-mean, our p-mean acheives 1% shorter wirelength and is 2×faster.

V. CONCLUSIONS

We discussed the HPWL accuracy of p-mean model along with existing wirelength models. Analytical placement results on ISPD 2004 benchmarks for p-mean model are promising in terms of wirelength and runtimes as oppose to the existing wirelength models.

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TABLE I: HPWL Measured on Global Placements Using Different Approximation Schemes A: Actual L:Logsum W:WA B:ABSWL G:(γ, p)-mean P:p-mean	Total HPWL (×107)					%Absolute Error in Approximation					
Circuit	A	B	L	W	G	P	B	L	W	G	p
ibm01 .	.170	.184		4.56			8.04			2.9	10.3
ibm02	.371 .496	.393	.188	7.46	.165	.153	5.90	10.6	2580	2.13	
ibm03 ibm04 ibm05 ibm06 ibm07	.592	.529	.399	11.2	.363	.342	6.62			2.38	7.60
ibm08 ibm09 ibm10 ibm11	1.03		.54	15.30		.457	7.20	7.74	1910	2.64	
ibm12 ibm13 ibm14 ibm15 ibm16	.525	.635		13.40	.485		4.15			1.44	8.03
ibm17	.873 .963	1.08	.648	14.90		.538	9.44	8.67	2160	3.35	
ibm18	.980 1.84	.574	1.09	26.1	.577		11.2			3.7	9.18
	1.42 2.40	.971	.59	29.7		.986	11.6	9.44	2480	3.7	
	1.77 3.36	1.07	1.0	37.30	1.02		14.40		1200	4.80	4.72
	4.08 4.35	1.12	1.11	60.3		.468	11.8	5.41	2740	4.33	10.9
	6.65 4.53	2.05	1.16	58.1	.507	.778	15.8		2890	5.014	10.9
		1.65	2.12	62.6	.841	.858	8.87	12.4	2980	3.39	
		2.62	1.71	75.3	.927	.84	16.2	14.5	3710	5.4	10.9
		2.06	2.68	1580	.933	1.59	19.8	15	3180	6.21	14.3
		4.03	2.15	1840	1.76	1.22	20.3	18.7	3980	6.35	13.5
		4.91	4.22	2140	1.35	2.13	24.8	15.4	2510	7.07	14.5
		5.43	5.15	2360	2.32	1.49	16.7	20.3	4140	5.32	11.3
		7.75	5.73	2390	1.68	2.80	27.1	11.7	4590	7.66	15.8
		5.76	8.08		3.15	3.41		21			16.6
			6.10		3.82	3.58		25.5	4410		16.4
					4.04	5.69		26.1	4820		17.8
					6.29	3.68		31.8	3450		14.4
					4.18			21.5	5190		18.7
								34.7			
Average Error (in %)							13.3			4.3	
								17.2	3270		12.5

TABLE II: HPWL Comparison of LSE, WA, (γ, p)-mean and p-mean Smoothings on ISPD 2004 Placement Contest Benchmarks

	LSE		WA		(y,p)-mean		p-mean	
Circuit	HPWL(×107)	CPU(sec)	HPWL(×107)	CPU(sec)	HPWL(×107)	CPU(sec)	HPWL(×107)	CPU(sec)
Ibm01	.180	26	.177	28	.170	59	.17	34
Ibm02	.389	56	.382	60	.359	144	.354	60
Ibm03	.529	69	.523	77	.480	155	.481	79
Ibm04	.621	90	.614	92	.573	239	.572	120
Ibm05	1.07	154	1.06	159	1.01	253	1.01	136
Ibm06	.55	146	.55	116	.49	229	.49	131
Ibm07	.92	198	.91	163	.83	303	.82	179
Ibm08	1.01	271	1.0	189	.92	387	.90	205
Ibm09	1.04	235	.93	213	.93	417	.94	238

ibm10	2.02	356	2.0	387	1.75	825	1.65	370
ibm11	1.58	301	1.57	239	1.41	582	1.40	320
ibm12	2.55	384	2.53	434	2.21	857	2.20	390
ibm13	1.88	410	1.88	347	1.69	822	1.70	453
ibm14	3.60	833	3.60	873	3.22	1831	3.11	880
ibm15	4.48	1151	4.33	1179	3.88	2522	3.87	1211
ibm16	5.06	1306	4.81	1074	4.37	3835	4.39	1284
ibm17	7.13	1390	6.91	1455	6.21	4063	6.13	1813
ibm18	4.81	1133	4.57	1455	4.46	4023	4.35	2034