UART design using FIFO ram and LCR circuit with BIST capability at different baud rate

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***Abstract* - The way integrated technology is growing becomes very difficult to apply circuit testing using Automatic TEST Equipment of complex circuit for this BIST (Built In Self test) is the solution of complex IC. Here we are applying BIST for UART which is considering as a low speed, low cost data exchange between computer and peripherals. Hence this paper shows implementation of UART with BIST capability using FIFO RAM, LCR at different baud rate, which solve the complex circuit testing with different baud rate it speed up the data handling capabilities of UART.**

***Keywords* - ATE, LCR, FIFO RAM, ATPG, BILBO, BIST, LFSR, and UART**

I. INTRODUCTION

The technology plays an important role in the fast growing world. Out of the different technologies available to cope with the changing world, digital technology is best in all sorts. Most of the systems including a small device like a television remote to a large one like metro train each employ digital technology for their functioning. So it becomes very important to test and diagnose the digital system time to time during its lifetime [1]. The process of Testing and diagnosing must be quick and have very high fault coverage. Since testing is being specified as system functions so it should have ability of self testing. Software implementation is used to get highest level of system testing [2]. Initially digital systems employed self test facility using software for maintenance and repair. Although having flexibility in this approach, the method has many demerits like long, slow, expensive and resolution of fault coverage and diagnose are not much high thus does not indicate the faulted part. This increases the need for self test function into the hardware.

One of the popular test techniques employing self test function into hardware used is Built-in-Self-Test (BIST). A BIST with universal asynchronous receive transmit (UART) has two important function first one to realise the specified testability requirements and second is to generate the low cost with the proper performance [1]. UART is usually important for input/output tools for decades and is still used commonly.

Serial port is responsible for transmission of serial data. A serial port is one of the main parts of a computer. Connector connects the serial line with the peripheral devices such as keyboard, mouse, modem, and printer and even to another computer. In different to parallel communication, these peripheral devices communicate with a serial bit stream. Main concentration of this method is on the design of embedded BIST capability UART and Very Large Scale Integrated (VLSI) testing problems followed by the behaviour of UART circuit using Very High Speed Integrated Hardware Description Language (VHDL) [2].

Now BIST techniques are generally used in industry, the BIST circuit that enlarge the hardware overhead increase time of design and degradation in performance is become the reason of the limited use of BIST in the implementation phase, the BIST technique contain the design of UART before the whole design is synthesized through repositioning the existing design to match testability requirements.

II. REQUIREMENT OF USING BIST TECHNIQUE

To identify a reliable testing method which reduces the cost of test equipment, a research which verifies each problem of VLSI testing has been performed. Following the problem mostly detected is given:

a) Test generation problems
b) The input combinatorial problems and
c) Gate to I/O pin ratio

Test generation problems

The VLSI circuits having large number of gates takes weeks or months for computation of automatic generation test. The length of test patterns becomes too large to handle by external testers that result in high computation cost and reasonable available time for production testing has been outstripped. Due to requirement of large memory for computation of sequential logic circuits which is not in combinational logic circuits creates problem for Automatic Test Pattern Generation (ATPG), hence take more time for Sequential circuits must be evaluated [1][3].

The input combinatorial problem

An N input combinatorial logic circuit has 2^N total set of possible input vectors. out This is the number of test vectors needed for exhaustive test of circuit in which some of these customer might use, where as in MSI (Medium-Scale-Integrated) circuits, like 32 bits microprocessor exhaustive test is to be prevented for VLSI circuit. To follow economic rules of production, finite numbers of vectors are applied [2][4]. The full exhaustive test needed large size of vectors than finite number of vectors test.

The Gate to I/O Pin Ratio Problem

It is quite difficult to access the internal nodes directly by any pin for the large gate count ICs package. Since gate counts go much faster than pin counts negatively affecting the controllability and observability by signal respectively from input and output pin, thus making internal node testing difficult.These difficulties inspired the designer to adopt reliable test method for VLSI testing. Hence with the insertion of special test circuitry on the VLSI circuit cover solution of all problems related to testing [4]. The best example is the VLSI circuit with implementation of BIST technology.

III. UART

A UART (Universal Asynchronous Receiver/Transmitter) is the microchip; when programmed and connected to serial device behave as a controller for computer interface. Normally to connect RS-232C Data Terminal Equipment (DTE) interfaces with computer help to "talk" and data exchange with modems and other serial peripheral devices [3].

In Serial transmission, basically modem is used to make connection among the computers, terminals and other devices for non-networked Communication. One computer exchange data with other computer and its parts required a communication link whether it is serial or parallel. Through printed circuit track, wires, optical fibre cables parallel link transfer several data streams (whereas some stream of particular bits results bytes) and single data stream is to be send through serial link.

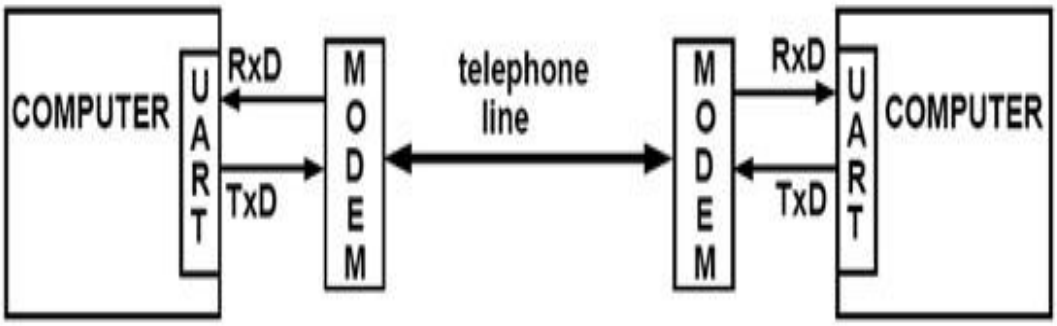

Figure1. Block diagram of Serial data transmission [3]

IV. BIST (BUILT IN SELF TEST)

BIST is nearly same as off-line testing using AUTOMATIC TEST EQUIPMENT (ATE) where the test response analyzer and the test pattern generator are on the same chip circuitry (instead of equipments). As circuitry is implemented in place of TESTING EQUIPMENT so it is quite clear to design the compressed implementations of test pattern generator and response analyzer are on the same circuitry [6]. The basic architecture of BIST is shown in Figure3.1.

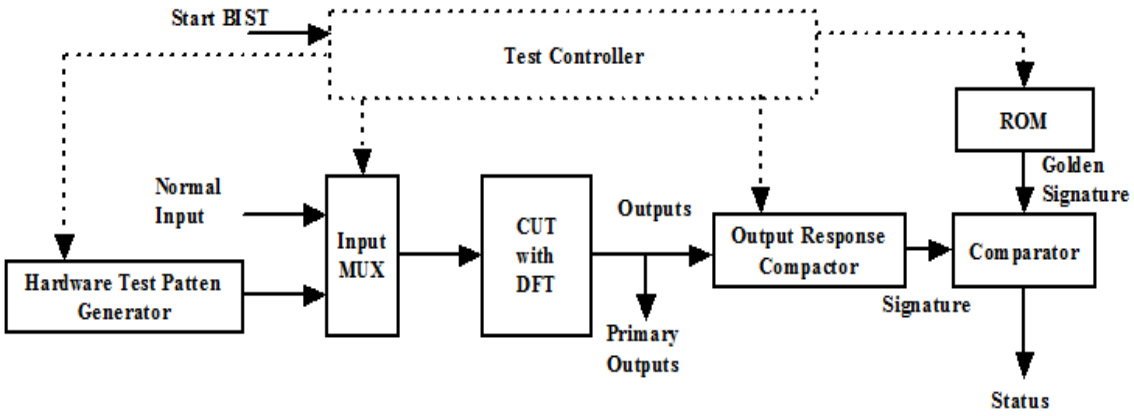

Figure2. Basic architecture of BIST [6]

V. RTL OF BIST

Figure3. RTL of BIST

VI. SIMULTIION RESULT OF BIST WITH DIFFERENT BAUD RATE

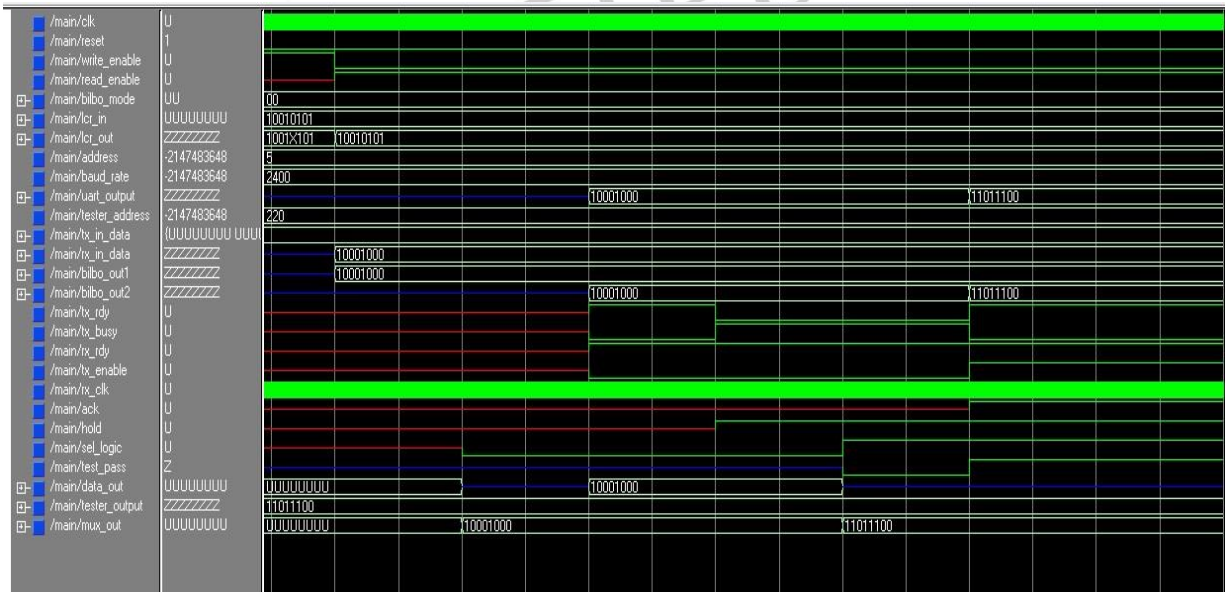

Figure4. Simulation Result of BIST

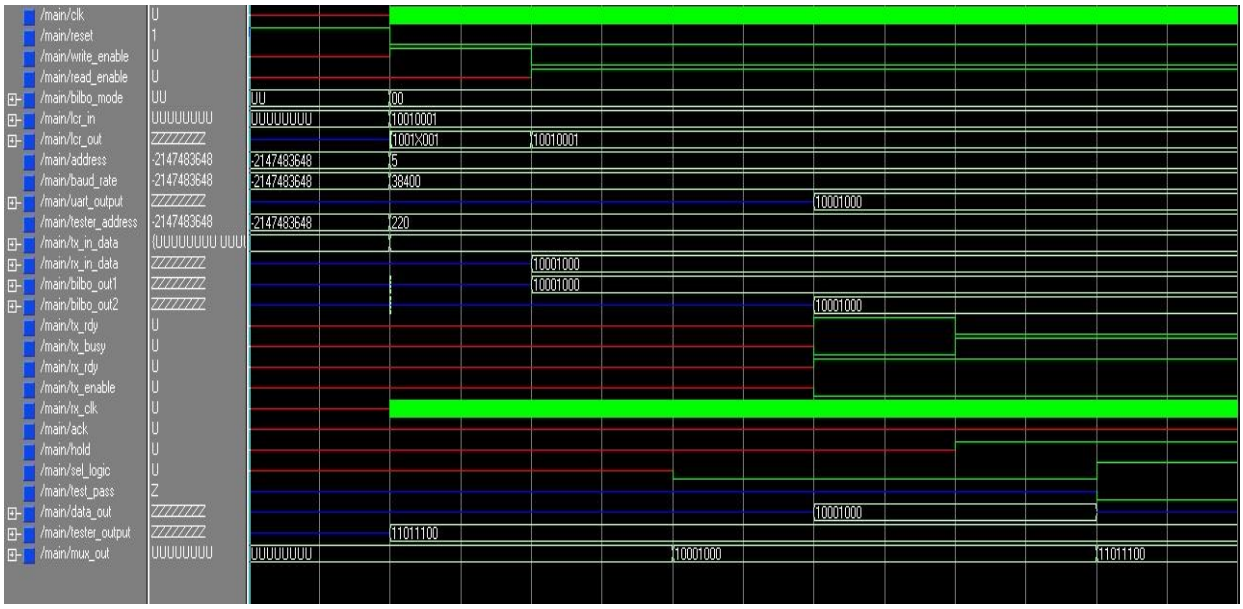

Figure5. Simulation Result of BIST

VII. CONCLUSION

Simulation result shows that at different baud rate with different data bits is very beneficial fo shows implementation of UART with BIST capability using FIFO RAM, LCR at different baud rate, which solve the complex circuit testing with different baud rate it speed up the data handling capabilities of UART. the BIST circuit that enlarge the hardware overhead increase time of design and degradation in performance is become the reason of the limited use of BIST in the implementation phase, the BIST technique contain the design of UART before the whole design is synthesized through repositioning the existing design to match testability requirements.

VIII. REFERENCES

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