Reduction of Leakage Power in D-Flip Flop using LC nMOS Technique

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***Abstract* - In CMOS circuits, Leakage Power dissipation is the major problem in front of the designers. There are various techniques introduced in the past decade to reduce the leakage power technique. One technique discussed in this paper. We propose a technique called LCnMOS for designing D- Flip Flop which significantly reduce down the leakage current without increasing the switching power dissipation. LCnMOS, a technique to tackle the leakage problem in all digital circuits, uses single additional leakage control transistor LCT, driven by the output from the pull up and pull down networks, which is placed in a path from pull down network to ground. This LCT provides the additional resistance thereby reducing the leakage current in the path from supply to ground. All the performance has been investigated using 90nm and 180nm Technology at 1 voltage as power supply and evaluated by the comparison of the simulation result obtain from TSPICE.**

***Keywords* - Leakage control Transistor nMOS, Delay, leakage power, LECTOR Technique, D- Flip Flop**

I. INTRODUCTION

With the increasing prominence of portable systems, it is important to enhance the life of battery as much as possible, since it is the limited battery life time that typically imposes strict demands on the overall power consumption of such systems. Although the battery industry has been making efforts to develop batteries with a higher energy capacity than that of conventional Nickel-Cadmium (NiCd) batteries, a revolutionary increase of the energy capacity does not seem imminent. Therefore, portable applications have led to rapid and innovative developments in low-power circuit designs. Power dissipation is also crucial for Deep Sub- Micron (DSM) technologies [1]. To further improve the performance of the circuits and to integrate more functions on a chip, the feature size has to continue to shrink. As a result, the power dissipation per unit area grows, increasing the chip temperature. Although power dissipation is important for modern VLSI design, performance, speed and area are still the main requirements of a design. However, low-power design usually involves making tradeoffs such as timing versus power and area versus power. Increasing performance, while the power dissipation is kept constant, is also considered to be a low-power design problem.

In fact, higher performance-per-watt is the new technique for micro-processor chip manufacturers today. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this trend, transistor leakage power has increased exponentially. The reduction of the supply voltage is dictated by the need to maintain the electric field constant on the ever shrinking gate oxide.

The paper is organized as follows: in Section II, previous work problems are reviewed and methodology is explained. Subsequently, in section III, the conventional D-flip flop and D Flip flop with LCnMOS approach are presented. In section IV, the simulation results are given and discussed. The comparison and evaluation for modified and existing designs are carried out. Finally a conclusion will be made in the last section.

II. PRELIMINARIES

Sleep Transistor Technique is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique is MTCMOS, which adds high-Vth sleep transistors between pull-up networks and Vdd and pull down networks and Gnd while for fast switching speeds, low-Vth transistors are used in logic circuits [2]. This technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values. These values impact the wakeup time and energy significantly due to the requirement to recharge transistors which lost state during sleep. **Sleepy Keeper Technique** consists of sleep transistors connected to the circuit with NMOS connected to Vdd and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuitis active [3]. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately, increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously monitor the circuit state and control the sleep transistors even though the circuit is in an idle state. **LECTOR Technique [10]** consists of two self controlled transistors which increases the resistance in the path from source to ground, which increases the area of the circuit, one of the most important constraint in the design of VLSI circuits. **LCPMOS Technique [4]** In this paper to design LCPMOS technique and achieves the reduction in leakage power compared to other leakage reduction techniques, such as LECTOR, sleepy stack, sleepy keeper, etc,

along with the advantage of not affecting the dynamic power, since this technique does not require any additional control and monitor circuitry shown in figure 1.

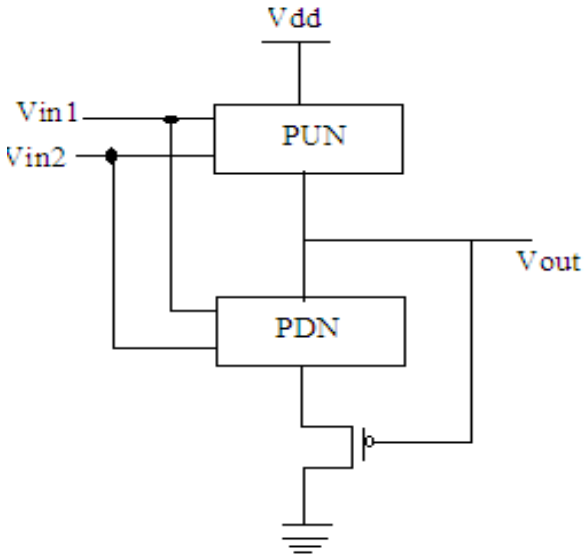

Figure.1 LCPMOS technique

(E) Proposed LCnMOS

In this proposed technique, we introduce a single leakage control transistor within the logic gate for which the gate terminal of leakage control transistor (LCT) is controlled by the output of the circuit itself. Which increases the resistance of the path from pull down network to ground thereby increasing the resistance from Vdd to ground, leading to significant decrease in leakage currents? The main advantage as compared to other techniques is that LCnMOS technique does not require any additional control and monitoring circuitry, thereby limits the area and also the power dissipation in active state.

Leakage Control nMOS (LCnMOS) technique is illustrated in detail with the case of an inverter. A LCnMOS inverter is shown in Figure 2. An nMOS is introduced as LCT between M1 and Gnd nodes of inverter. When Vdd=1V, input A=0, the output is high. As the output drives the LCT the LCT goes to ON state hence provides high resistance path between Vdd and Gnd. When A=1, the output is low; hence LCT will be in OFF state hence output is low. LCnMOS inverters for all possible inputs are tabulated in Table 1.

Table-1

Transistor Reference	Input Vector (A)	
	0	1
M1	ON state	OFF state
M2	OFF state	ON state
LCT (nMOS)	ON state	OFF state

In the sleep related technique, the sleep transistors have to be able to isolate the power supply and/or ground from the rest of the transistors of the gate. Hence, they need to be made bulkier dissipating more dynamic power. This offsets the savings yielded when the circuit is idle. Sleep transistor technique depends on input vector and it needs additional circuitry to monitor and control the switch in sleep transistors, consuming power in both active and idle states. In comparison, LC nMOS generates the required control signals within the gate and is also vector independent.

Single transistor is added in LC nMOS technique in every path from Vdd to Gnd irrespective of number of transistors in pull-up and pull-down network. The loading requirement with LCT is a constant which is much lower.

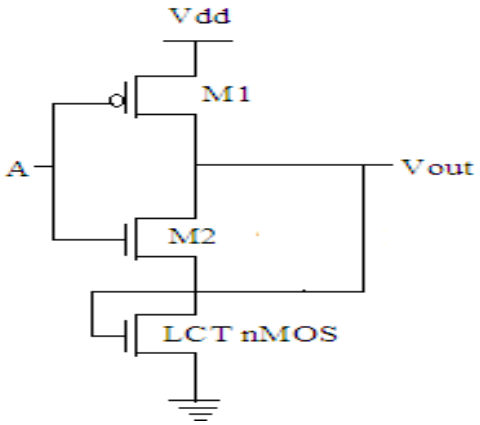

Figure 2: LCnMOS NOT Gate

III. D- FLIP FLOP CIRCUITS

D flip flop is explored in this section first conventional than LCnMOS D flip flop in this section. The LCnMOS technique is applied to the CMOS sequential circuit and also the base case is implemented to calculate the amount of leakage power reduced in LCnMOS technique.

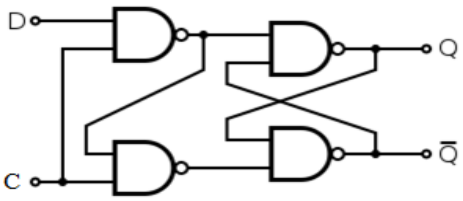

Figure 3: D-type transparent latch based on an SR NAND latch

The working of this D latch is according to the table 2 which is shown below

Table-2

INPUTS		OUTPUT		COMMENTS
C	**D**	**Q**	**$\overline{Q}$**	
0	X	Q_{prev}	$\overline{Q}_{prev}$	No change
1	0	0	1	Reset
1	1	1	0	Set

(A) CONVENTIONAL D Flip Flop

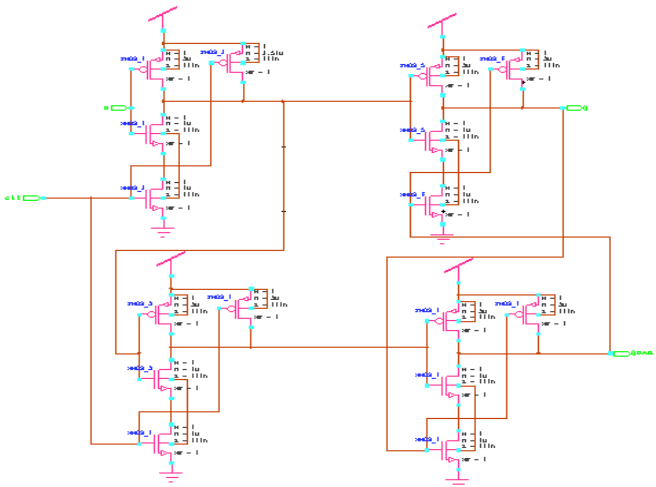

Figure 4: Tanner Tool Schematic of Conventional D-Flip Flop

The conventional tanner tool schematic is designed according to the gate level diagram in figure 3. And the figure 5 will show the simulated output of the conventional D Flip flop.

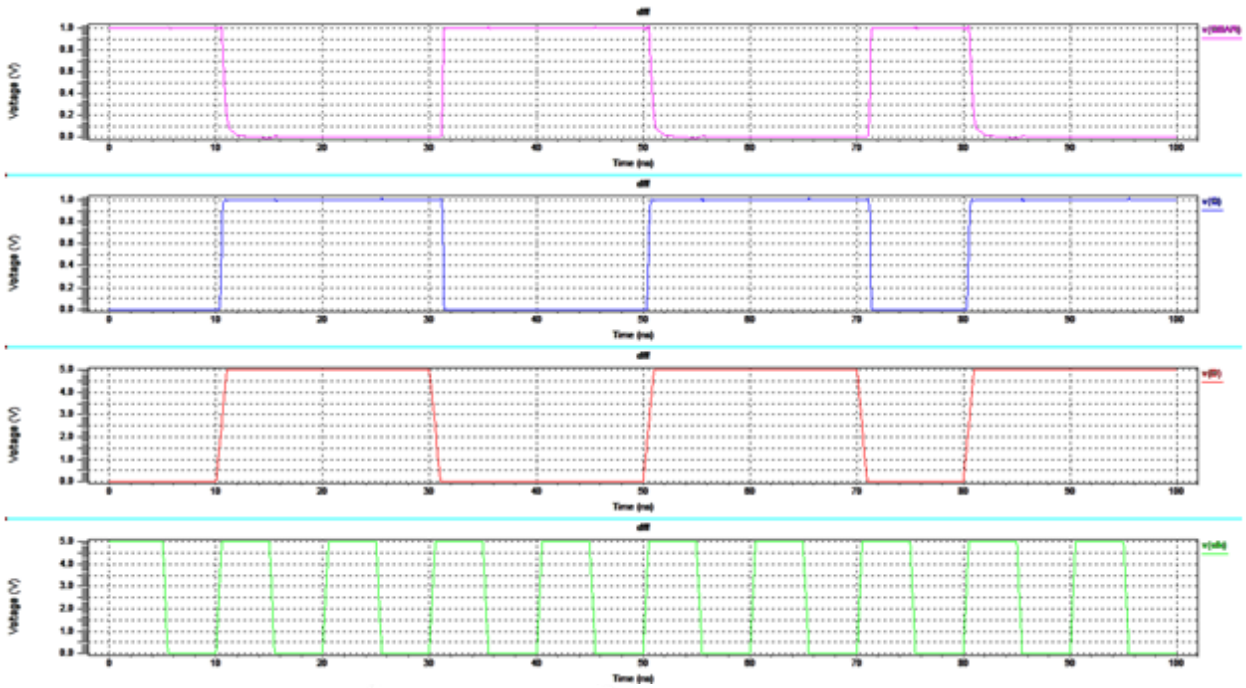

Figure 5: Simulation Waveform of conventional D flip flope

(B) LCNMOS based D flip flop.

The 2-input CMOS D Flip Flop in Figure6 with the one LCT added between pull-down network and gnd. The simulation wave form of LCnMOS D Flip Flop is shown in the Figure8, which show that the basic characteristics of D Flip Flop as described in table 2.

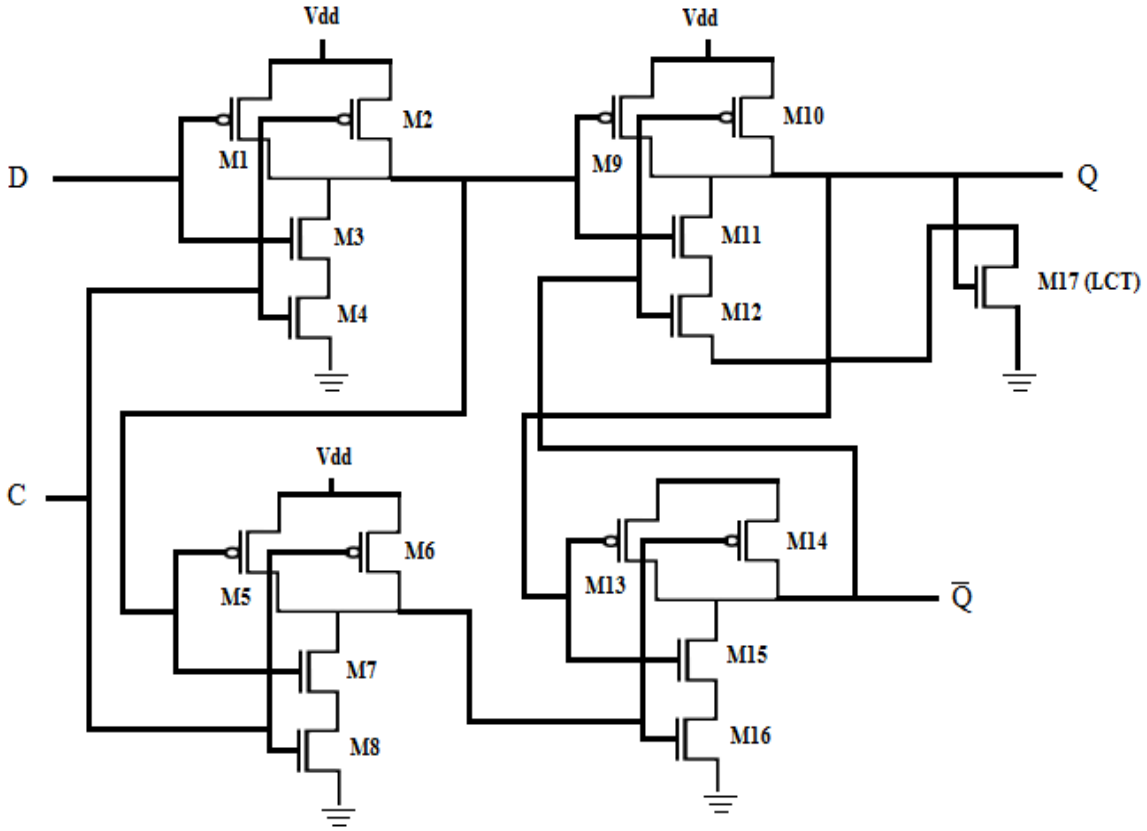

Figure6: Transistor Level Schematic of LCNMOS D-Flip Flop

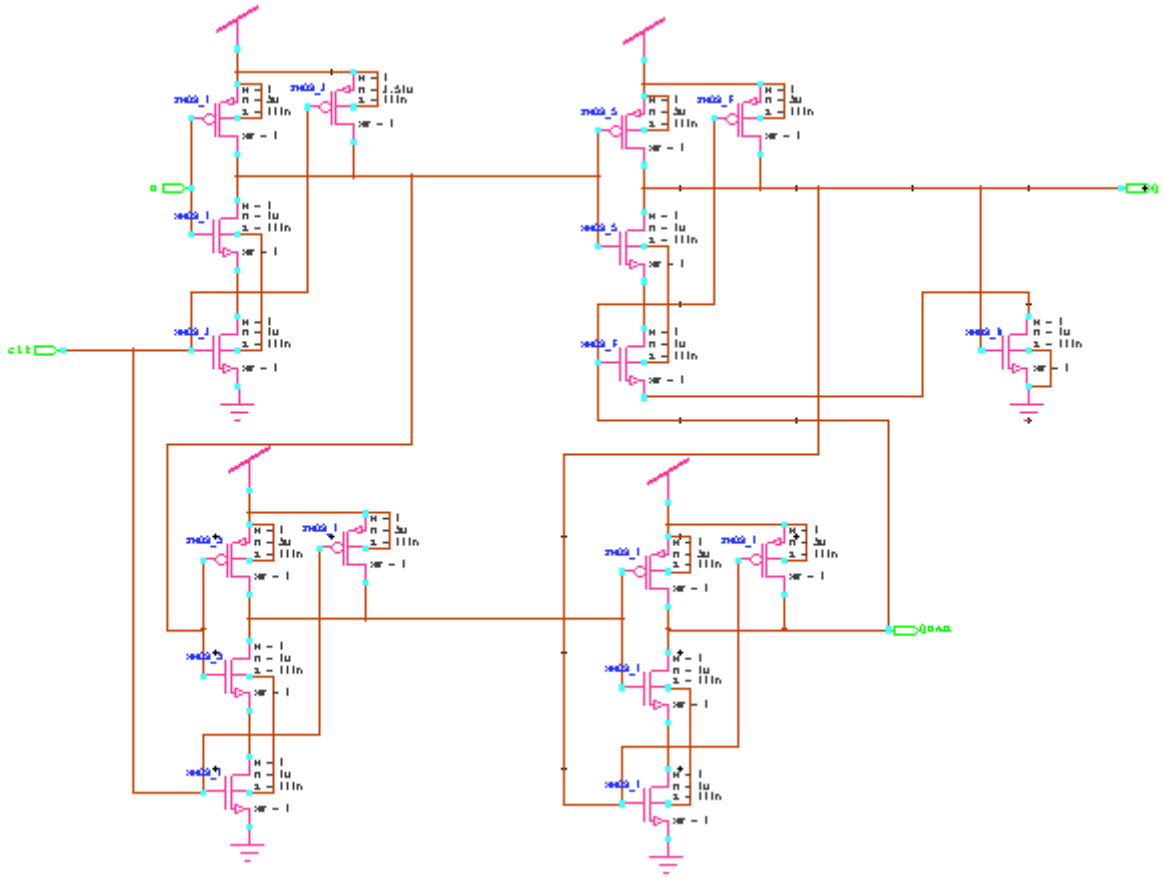

Figure 7: Tanner Tool Schematic of LCNMOS D-Flip Flop

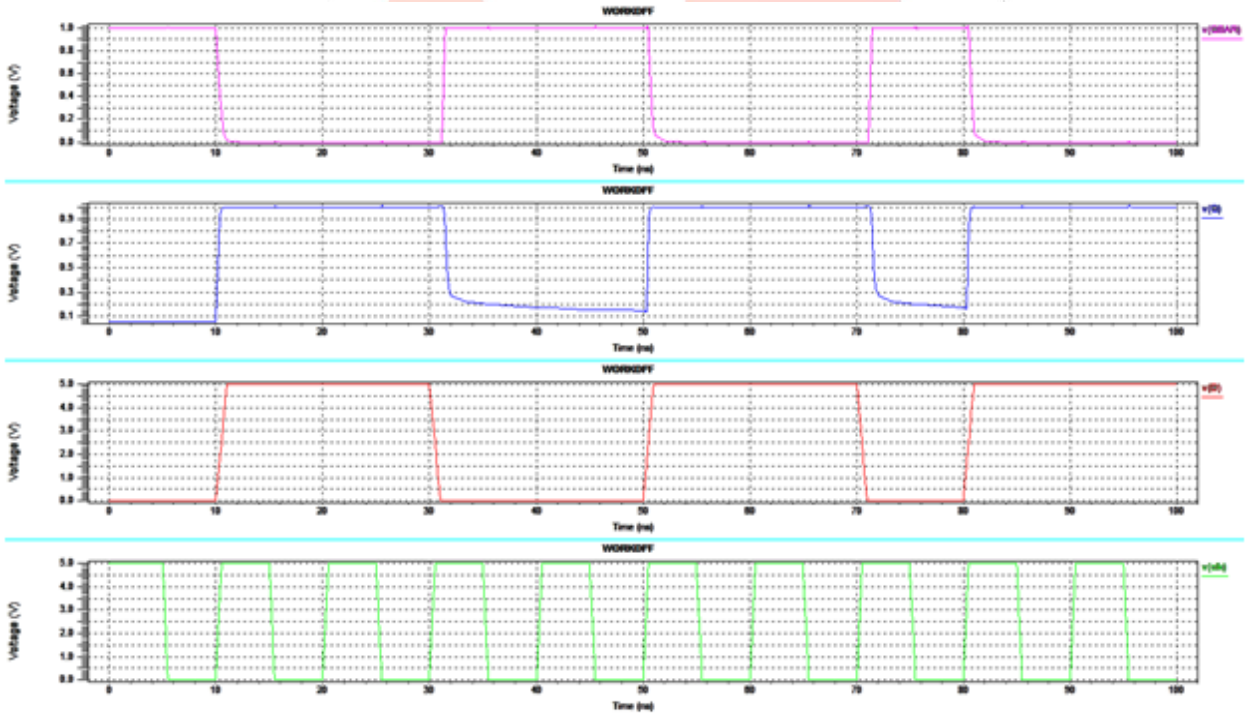

Figure.8:Simulation waveforms of LCnMOS D Flip Flop

All the simulation is done taking V_{dd} as 1V. For all the input combinations it can be seen that the Q and $\overline{Q}$ output is according to the table 2 Showing the Q and complementary Q at the outputs for the inputs D(data) and C(control) or clock.

(C) LCnMOS D Flip Flop Layout

Layout of D flip flop is designed in the L-edit tool using 180nm technology, where all the NMOS and PMOS are arranged according to the transistor level architecture. In layout design all the NMOS and PMOS are placed in two parallel rows, all the poly-silicon lines are laid out vertically and area between the n-type and p-type diffusion is utilized for interconnections (routing).

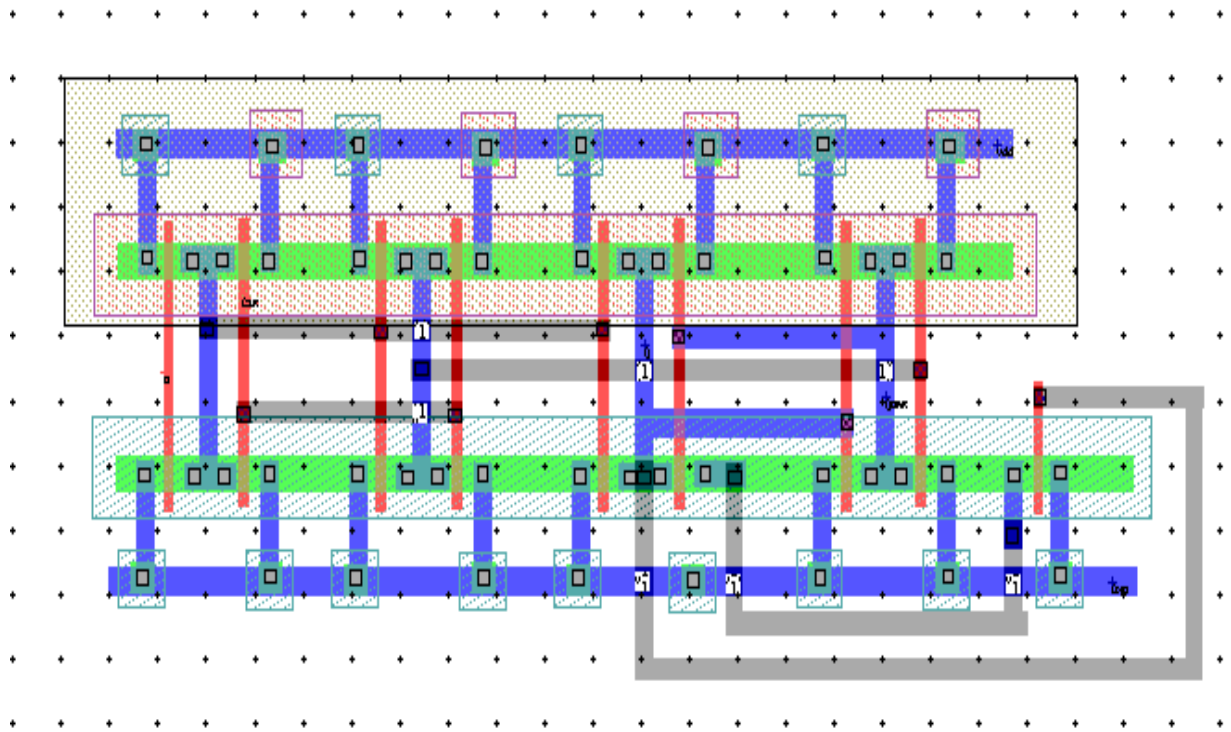

Figure.9:Layout of LCnMOS D Flip Flop

IV. EXPERIMENTAL RESULTS

The leakage power is measured using the Tanner Tool S-EDIT simulator. The results obtained through the technique for logic gates are shown in Table 2. Simulation for the logic gates are performed by taking two different process parameters Viz.180nm, 90nm CMOS Technology.

Table-3

Technology	Conventional D Flip Flop	LCnMOS D Flip Flop	Percentage reduction in power dissipation
90nm	$3.46*10^{-15}$ watts	$2.64*10^{-15}$ watts	24%
180nm	$3.53*10^{-15}$ watts	$2.88*10^{-15}$ watts	19%

V. CONCLUSION

In this paper we have presented leakage power reduction LCnMOS technique. It becomes a great challenge to tackle the problem of leakage power. LCnMOS uses one LCT which is controlled by the output of circuit itself. LCnMOS achieves the reduction in leakage power compared to other leakage reduction techniques, such as LECTOR, sleep transistor, sleepy keeper, etc. The performance has been investigated using 180nm & 90nm Technology and evaluated by the comparison table 3 of the simulation result obtain from TSPICE.

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