Modified Design of High Speed Baugh Wooley Multiplier

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***Abstract* - Multiplication plays a very important role in the implementation of signal processing and arithmetic unit. Several researchers proposed various technologies and implemented and verified their designs with the present techniques and their merits and demerits are evaluated. In this paper Baugh Wooley multiplier is implemented in which the ripple carry adder is replaced with the carry select adder. In order to further reduce the area carry select adder is designed using the gated architecture which further improves the timing constraint also. The results show a significant improvement in the speed of multiplication by applying the proposed approach.**

***IndexTerms* - Baugh Wooley, Carry Select Adder, Ripple Carry Adder**

I. INTRODUCTION

Multipliers are the important unit in digital systems and other applications related to digital processing [1]. Several researchers have tried designing the multipliers which met either one of the two constraints i.e. low power consumption and low area utilization and the high speed or a combination of them. The multiplication algorithm uses add and shift methodology [2]. Variety of partial product values is superimposed on the parallel numbers to enhance the performance of the multipliers. To implement speed constraint Baugh Wooley multiplier algorithm is used.

Field programmable gate array is a powerful device which enables programmers to design hardware for the specific software or program [3]. Day by day the prices of the FPGA are decreasing and the logic capability is increasing which gives an upper edge for the designers to use FPGA in their applications. Many designers also use soft core processors with FPGA to enhance their application capability and flexibility [4].

FPGAs are reconfigurable devices i.e. they are configured easily every time and ant type of hardware can be implemented in these devices. They are very effective for the implementation of a number of architectures [5]. In the last few years there is a vast increment in the resources of the FPGA which enables the designers to implement devices like memories, peripherals on a single chip.

II. BAUGH WOOLEY MULTIPLIER

The Baugh-Wooley multiplication is one amongst the economical ways to handle the sign bots. This method has been developed so as to style regular multipliers, suited to 2‘s complement numbers [5]. Let 2 n-bit numbers, number (A) and number (B), to be increased. A and B are often pictured as

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i \quad (1)$$

$$B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i \quad (2)$$

Where the ai’s and bi’s area unit the bits during A and B, severally, and a_{n-1} and b_{n-1} area unit the sign bits. Figure 1 shows the architecture of baugh wooley Multiplier. The product, P = A x B, is provided by the equation:

$$P = A \times B = \left(-a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i\right) \times \left(-b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i\right)$$

$$= a_{n-1}b_{n-1}2^{2n-2} + \sum_{i=0}^{n-2} a_i 2^i \sum_{j=0}^{n-2} b_j 2^j - 2^{n-1}\sum_{i=0}^{n-2} a_i b_{n-1}2^i$$

$$- 2^{n-1}\sum_{j=0}^{n-2} a_{n-1}b_j 2^j \quad (3)$$

The final product is often generated by subtracting the last 2 positive terms from the primary 2 terms.

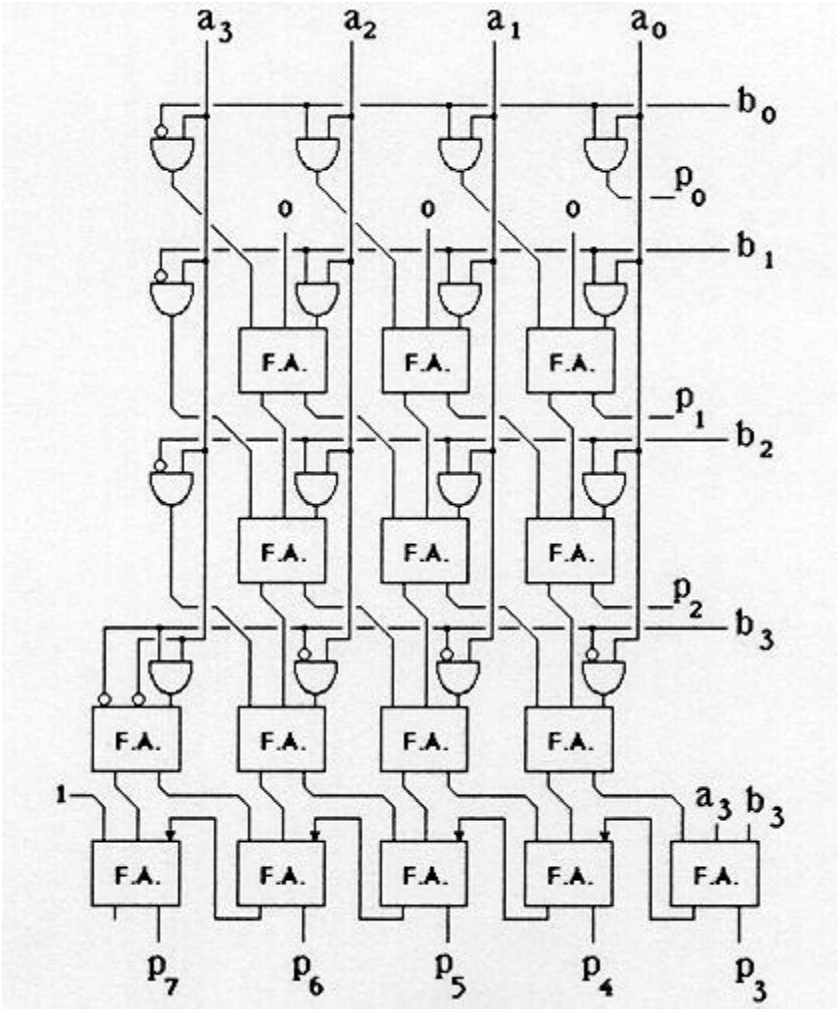

Figure 1: Baugh Wooley Multiplier Architecture

Baugh-Wooley Two's Signed numbers: Baugh-Wooley Two's compliment Signed numbers is that the best better-known algorithm for signed multiplication, as a result of it maximizes the regularity of the multiplier and permits all the partial products to own positive sign bits. Baugh–Wooley technique was developed to style direct multipliers for Two's compliment numbers [8]. When multiplying the two's compliment numbers directly, every of the partial product to be superimposed could be a signed numbers. so every partial product must be sign extended to the dimension of the ultimate product so as to create an accurate total by the Carry Save Adder tree [10]. According to the Baugh-Wooley approach, an economical methodology of adding additional entries to the bit matrix advised to avoid having modified the negatively weighted bits within the partial product matrix.

III. METHADOLOGY

Baugh Wooley multiplier can be implemented by changing the ripple carry adder unit of the baugh wooley multiplier with the carry select adder unit. Also to make the area of the carry select unit optimized, it must be implemented using only logic gates. Initially the carry select adder can be realized using the two ripple carry adders. In the proposed technique the carry select adder can be divided into three units i.e. half adder unit which sum and carry for all the operands and then carry generation unit in which we produce carry for both inputs of carry in i.e. 1 and 0. And finally we take ex-or of both the sum and the carry. Figure 2 and 3 shows the architecture of both the half adder unit and the carry generation unit.

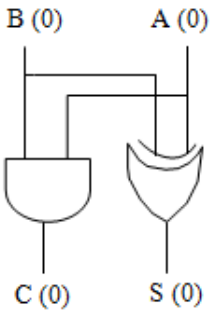

Figure 2: Simple Half Adder Unit

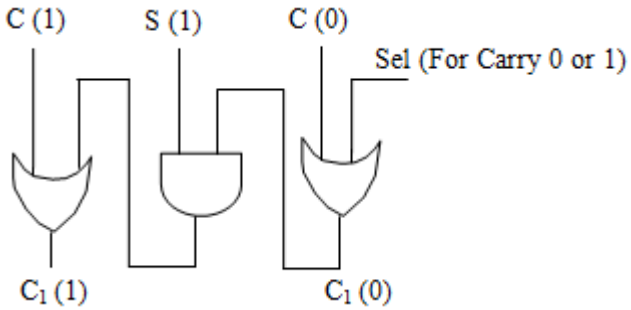

Figure 3: Carry Generation Block

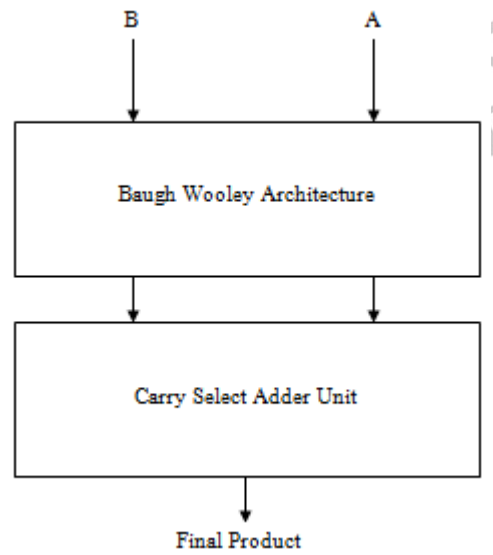

Figure 4: Proposed Methodology

Figure 4 shows the proposed technique in which the ripple carry adder of the baugh wooley multiplier of figure 1 can be replaced with the carry select adder. The carry select adder can be designed using the above proposed methodology.

IV. RESULTS

The above methodology is implemented using the Xilinx ISE software on Spartan 6 FPGA. The hardware description language used for the design is Verilog. Figure 5 shows the top module implementation of the proposed architecture and the synthesis results shows good improvement in speed of the circuit as the delay reduces from **8.807ns** from the base paper implementation to the **2.713ns** from the proposed methodology implementation.

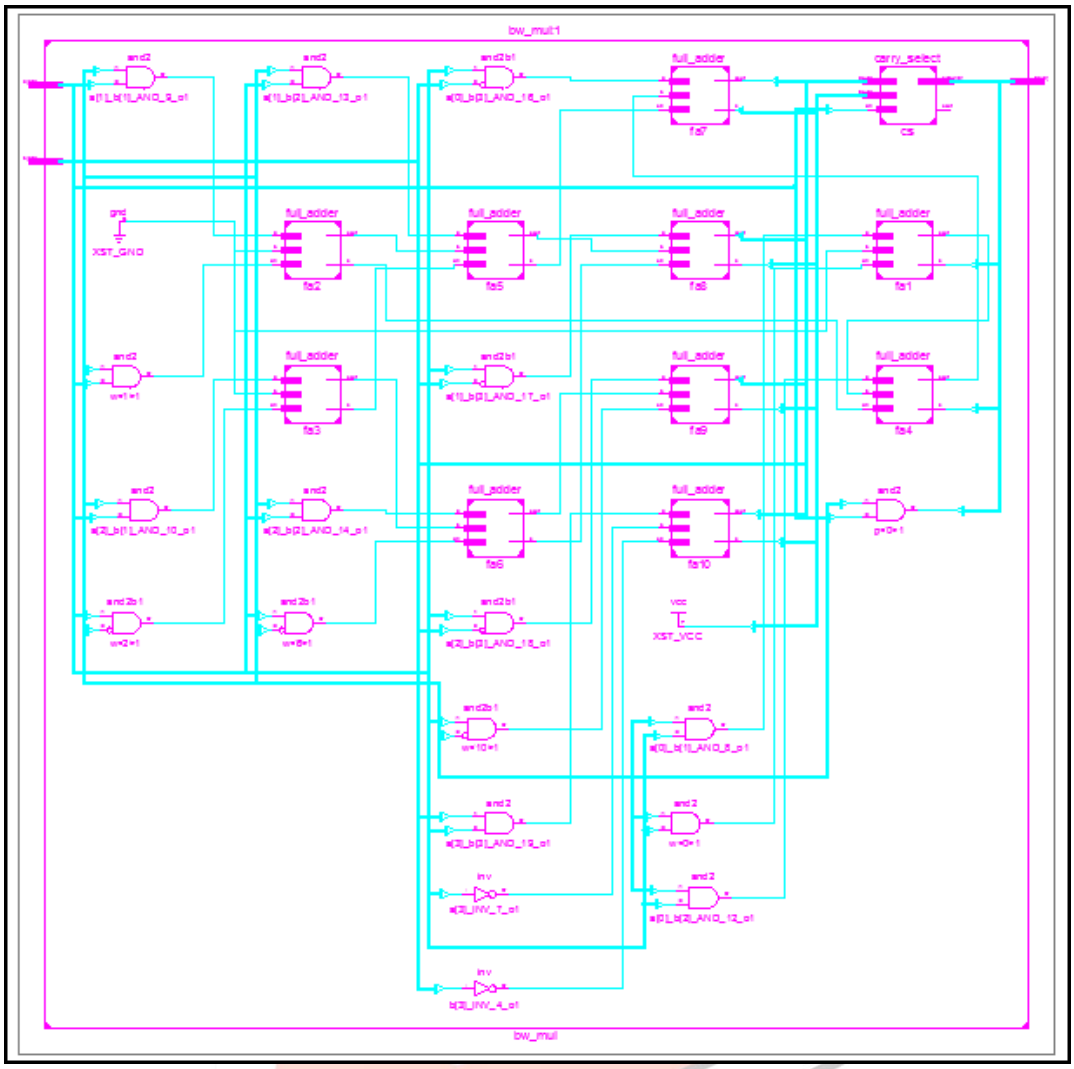

Figure 5: Top Module Implementation of Proposed Methodology

Figure 6 shows the simulation results waveform of the proposed methodology.The input numbers taken are **A = 0101** and **B = 0100** the result comes out to be **P = 00010100.** .

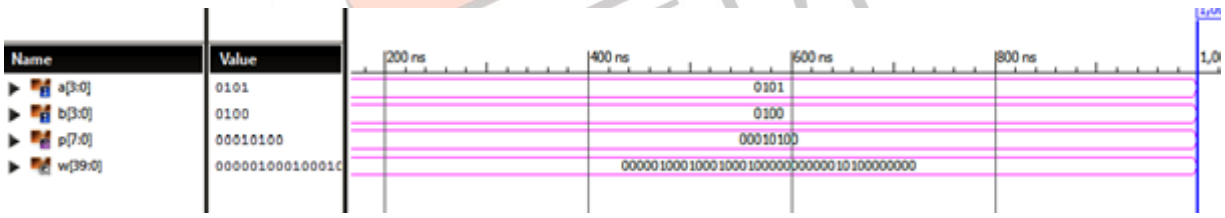

Figure 6: Simulation of the proposed methodology

V. CONCLUSION

Binary Multipliers play a significant role in digit system designing. The fast multiplication operation is a widely researched topic in recent times. There are many methodologies used by the researchers to implement the multipliers. In this work a novel methodology of designing the carry select adder is proposed which is implemented in the Baugh Wooley architecture. The results show the promising improvement in the delay values. In future other multipliers must be tested with the implementation of the fastest known adder in literature i.e. carry select adder.

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