Design of High performance and Low Power 8T Full Adder Cell Using Double Gate MOSFET at 45nm Technology

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***Abstract* - Design of complex arithmetic logic circuits considering active power and delay is an important and challenging task in deep submicron circuits. Double gate transistor circuit consider as a promising candidate for low power application domain as well as used in Radio Frequency (RF) devices. In this paper we designed full adder with the help of double gate transistor, the used parameters value has been varied significantly thus improving the performance of full adder. Power Gating is one of the most used circuit techniques to reduce the leakage current in idle circuit. In this paper different parameters are analysed on Power Gating Technique. Power Gating technique achieves 93% reduction of leakage current, active power is reduced by 65% and delay is reduced by 24% as compared with conventional double gate full adder. Simulation results of double gate full adder have been performed on cadence virtuoso with 45nm technology.**

***Keywords* - Power Gating, Double-gate MOSFETs, full adder, Power, Delay.**

I. Introduction

Life of battery is the most important factor in portable electronics devices. An adder is the most important component of an arithmetic unit. The efficiency of arithmetic unit is depending on the efficiency of adder. To improve the performance in terms of low power and high speed of an adder many structure are designed. Adder is the critical and most essential building blocks in DSPs and microprocessors. In this paper we present a 8T full adder circuit by using double gate MOSFET which consume low power and give faster response. In the proposed adder circuit we use 8 double gate transistors so it is called 8T adder cell. We used 8T adder because it required less area as compared to the higher gate count full adders, lower power consumption and low operating voltage 5v-7v. It is difficult to keep full voltage move forward and backward operation with transistor count and low power consumption are pursued. In transistor logic circuit, the output voltage move forward and backward may be degraded due to threshold problem. The disadvantage of 8T full adder circuit is loss of threshold voltage in transistors. To overcome this drawback circuit design in this paper. Double gate MOSFET technique reduces power consumption, area and transistor stack height. In double gate MOSFET, there are two electrically independent gates, which give more flexibility in design of low power. To reduce short channel effect of scaled device Double gate transistor is used due to their better electrostatic control on channel charges. As compared to the conventional structure 8T structure saves up to 84% of the number of transistor involved in the conventional full adder so the area required by 8T structure is reduced. The power consumption for CMOS circuit is given by the following equation :

$$P_{avg} = P_{dynamic} + P_{leak} + P_{short\ circuit} \quad (1)$$

$$= CLV_{dd}.V.f_{clk} + I_{leak}.V_{dd} + I_{sc}.V_{dd}$$

We clearly say that the power depend on the different parameter as well as on the supply voltage. Lowering the supply voltage would significantly lower the power consumption of the circuit. This basic concept of would be used to improve the performance of adder circuit.

II. STRUCTURE OF DOUBLE GATE AND BENEFITS

In double gate MOSFET (DGMOSFET), Si channel is very small in width and can be controlled by applying gate control on both sides of channel. In double gate device both gate are coupled each other and this reduce the short channel effect and leakage. By using two gates circuit with double gate transistor can be operated as low input voltage as compared to the planer CMOS circuit and these means low power consumption. Gate leakage is also low in double gate device. It is occur due to gate tunnelling and overlap tunnelling current. Here short channel effect is controlled by two gates so there is no need to heavy doping. Since very light doped or undopped channel can be used in double gate transistors.

III. FULL ADDER

Full adder is a combinational circuit addition operation of input bits. Full adder contains three inputs and two outputs. The input variables are A, B and Cin. The two output variables are SUM and carry (Cout). The Boolean expression for full defined below:

$$SUM = (A\ xor\ B\ xor\ C) \quad (2)$$

$$CARRY = (A\ and\ B)\ or\ (A\ and\ C)\ or\ (B\ and\ C) \quad (3)$$

IV. PROPOSED FULL ADDER

In this we have proposed full adder circuit which shows better results as compare to given circuit. The four-transistor XNOR module has been used in this full adder. XNOR signal is used as the selector of two static multiplexer. XNOR signal has V_t threshold loss. Output multiplexers have V_t threshold loss too. COUT and SUM generator circuits are two multiplexers that each uses only two transistors. There are not any VDD and GND in these components therefore these components consumes low power. Simplicity of the carry generator and sum generator circuits are another reason to decrease power and delay in these circuits. The main problem of the circuit is output threshold loss problem. The total number of transistors used in this circuit is ten. There is semi inverter to invert input A. This inverter should work only when XNOR signal is equal to logic 0. Therefore, we use XNOR signal as GND of the inverter to decrease short circuit and leakage power in the inverter. On the other hand, switching activity on the node X will be reduced by using XNOR signal in the mentioned inverter. Input C, drive one transistor gate and two transistor junctions. The schematic of 4T XNOR circuit is shown in Figure 1 and Figure 2 shows a truth able of XNOR circuit. This is heart of full adder circuit.

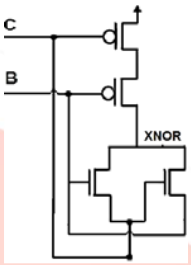


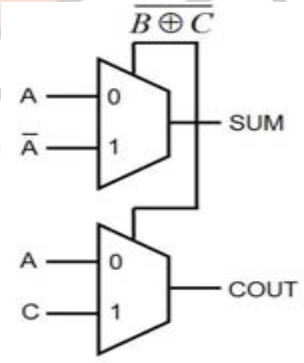
Fig.1:4T XNOR circuit

CB	*OUT*
0 0	$VDD\text{-}V_T$
0 1	*GND*
1 0	*GND*
1 1	*VDD*

Fig.2: Truth table

a) Block diagram and truth table

The block diagram and truth table for proposed circuit is shown in this section. The block diagram tells how the circuit works and implementation of proposed circuit is verified by given truth table. The Figure 3 and 4 shows block diagram and truth table respectively.



Fi.3: Block diagram

C	B	A	$B \oplus C$	$\overline{B \oplus C}$	COUT	SUM
0	0	0	0	1	C	A
0	0	1	0	1	C	A
0	1	0	1	0	A	$\bar{A}$
0	1	1	1	0	A	$\bar{A}$
1	0	0	1	0	A	$\bar{A}$
1	0	1	1	0	A	$\bar{A}$
1	1	0	0	1	C	A
1	1	1	0	1	C	A

Fig.4: Truth table for proposed circuit

V. STRUCTURE OF DOUBLE GATE AND BENEFITS

In double gate MOSFET (DGMOSFET), Si channel is very small in width and can be controlled by applying gate control on both sides of channel. In double gate device both gate are coupled each other and this reduce the short channel effect and leakage. By using two gates circuit with double gate transistor can be operated as low input voltage as compared to the planer CMOS circuit and these means low power consumption. Gate leakage is also low in double gate device. It is occur due to gate tunnelling and overlap tunnelling current. Here short channel effect is controlled by two gates so there is no need to heavy doping. Since very light doped or undoped channel can be used in double gate transistors .

Double gate 10t full adder circuit

Double gate Transistor can be constructed by connecting two transistors in parallel as a manner that their source and drain are connected together. Double gate transistor can be designed by two gate structure, based on gate biasing, first one is achieved by independent gate control and it is described as four terminal devices. When the front and back gate are connected together second one is implemented abd it is described as three terminal devices, this structure is used for direct replacement of single gate transistor.

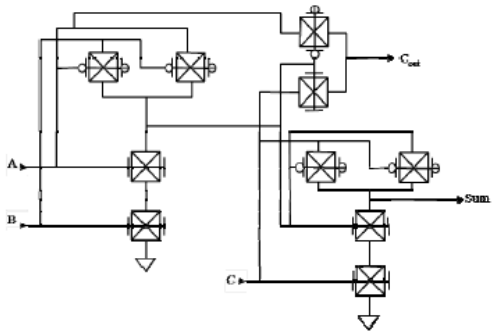


Fig 5:Double gate 10T transistor full adder

VI. REDUCTION TECHNIQUE

Power Gating

Power Gating, it reduces the leakage by inserting n-MOS and p-MOS to the circuitry. Figure shows the power Gating circuit. This technique is very popular for reducing leakage in the circuits. Because of simplicity implementation of the technique, power gating has been used to minimize leakage energy in circuits at architectural level. The effectiveness of power gating required following

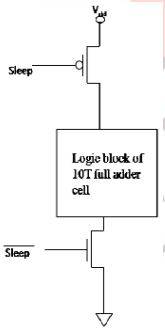


Fig.6: Power Gating Circuit.

- It provides the switches for turning off and on of the functional units at circuit level.
- These switches controls the power g ate at various parts of the circuit can be provided as handles at the system software or the level thereby giving the system compiler the ability to control them.

A sleep control mechanism is used for efficient power management. In the active mode, sleep is set to low and sleep controlled transistor is turned on. Since their resistance is small the supply voltage Vdd and Vss(gnd) function as real power line. In standby mode, sleep is set to high and transistors are turned off, and leakage current is low. In fact only one type of transistor is enough for leakage control. Power gating is a technique that can be easily implemented on existing circuits. Power Gating can reduce the stand by leakage power and

inserted MOSFET can increase the area and delay .For p-mos(n-MOS) insertion, applied voltage on gate 0v is active mode and virtual Vdd line is connected to the supply Vdd. figure shows the Power Gating technique diagram

Schematic design of proposed circuit

The schematic design of proposed circuit is shown below in Figure7. The circuit consists of 8Transistor. This counts for low power dissipation and area.

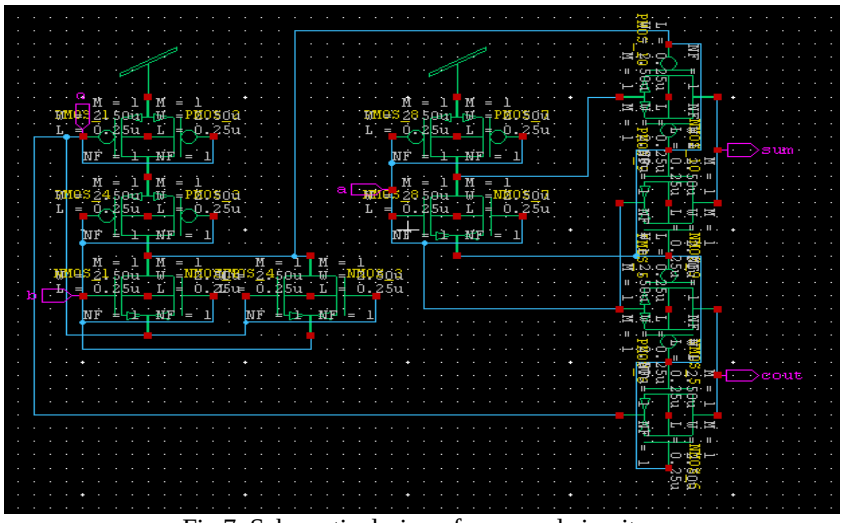


Fig.7: Schematic design of proposed circuit

VI. SIMULATION AND RESULTS

A bit full adder circuit based on double gate MOSFET technique is proposed. Simulation of the propose circuit is done by using the Cadence virtuoso tools. It is used for measurement of power consumption, leakage, and delay of circuit at 45nm technology with different supply voltage. The simulations have been done for different supply voltage and temperature. The proposed circuit is simulated for voltage range of 0.3 to 0.7 at room temperature.

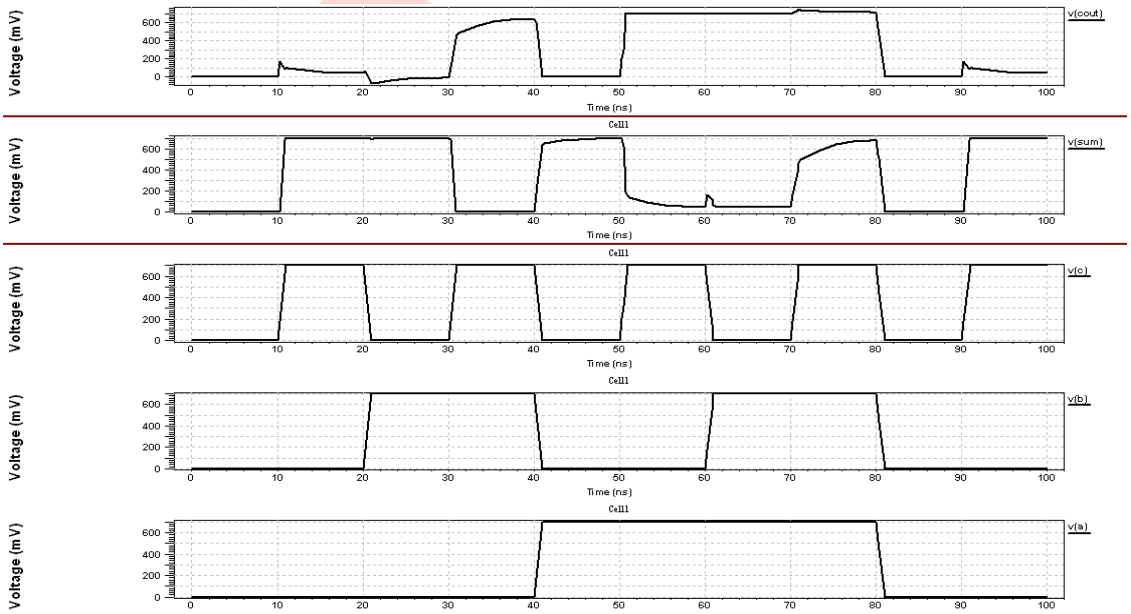


Fig 8: Input and Output waveform for proposed circuit

The table I show power dissipation of proposed circuit for given range of supply voltage which is from 0.3 to 0.7 V. This table shows that circuit can perfectly for low power. The delay for given circuit is 10 nsec. This table also reveals that this circuit work for wide range of supply voltage. The table II shows variation power with temperature and this table tells that power dissipation is increased with increasing temperature. This is due to affects like phonon scattering at high temperatures.

Table 1: Power dissipation

Serial no	Power supply(mV)	Power dissipation (nW)	Power delay product($\times e^{18}$)
1	300	6.1	61
2	400	9.8	98
3	500	17.0	170
4	600	28.0	280
5	700	43.8	438

Table 2: Variation power with temperature

Serial no.	Temperature(degrees)	PDP ($\times e^{18}$)
1	0	47
2	10	49
3	20	55
4	30	65
5	40	76
6	50	93

DELAY

Propagation delay is the required by a digital signal to travel from that input of the circuit to the output. The propagation delay is related to the speed of the architecture as inversely in nature and hence it is important performance parameter. The basic equation of delay in presence of sleep

transistor is shown in Eq. below

$$d_{sleep} = \frac{K.C_l.V_{dd}}{V_{dd}-2\,V_x-V_{tl}^2} \quad (4)$$

Where, V_X is the potential of the virtual rails, and K is the proportionality constant, C_L is the load capacitance at the gate output; V_{tL} is the low-voltage threshold. Fig.9. Delay Comparison Graph for different technology

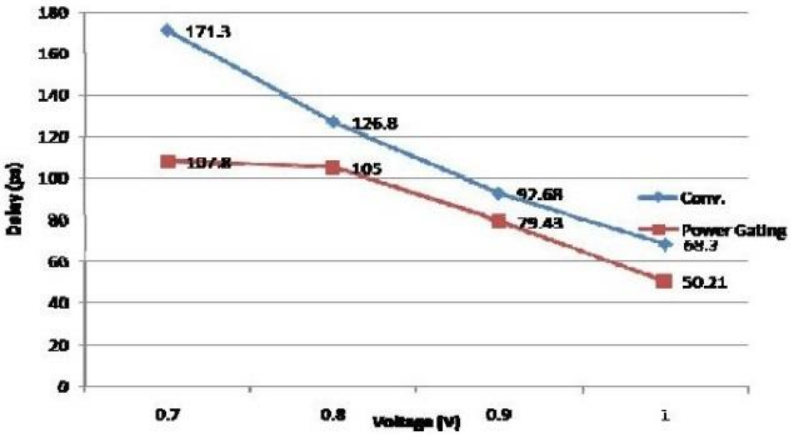


Fig9: Delay comparison graph for different technology

VII. CONCLUSION

In this paper we designed the double gate full adder with Power Gating technique. Double Gate MOSFET technology achieves low leakage and high performance operation with high speed. The Power Gating technique reduces the leakage current in standby mode. Different parameters are analysed at various voltage supplies. The active power is reduced by 64% and delay is reduced by 14% respectively as compared to conventional double gate full adder. Simulation results of double gate full adder have been performed on cadence virtuoso with 45nm technology.

Table 3: Comparison for existing and proposed circuit

Serial no.	Parameters	Existing circuit	Proposed circuit
1	Supply voltage	0.7	0.7
2	Power dissipation	7.2 uwatts	43.8 nwatts
3	Power Delay product	$784\times e^{18}$	$438\times e^{18}$
4	No. of transistors	13	10

The table 3 shows a comparison for existing and proposed circuit. The table III shows a comparison between exiting and proposed. This table shows that 98% power reduction in proposed circuit. The overall power delay product is reduces by 46%. Although the delay is increased but still PDP is low as compare to base paper. Again there is lower number of transistors are used the proposed circuit has 10 transistors whereas the existing circuit has 13 transistors. The proposed circuit shows overall improvement for designing full adder circuit.

VIII. ACKNOWLEDGMENT

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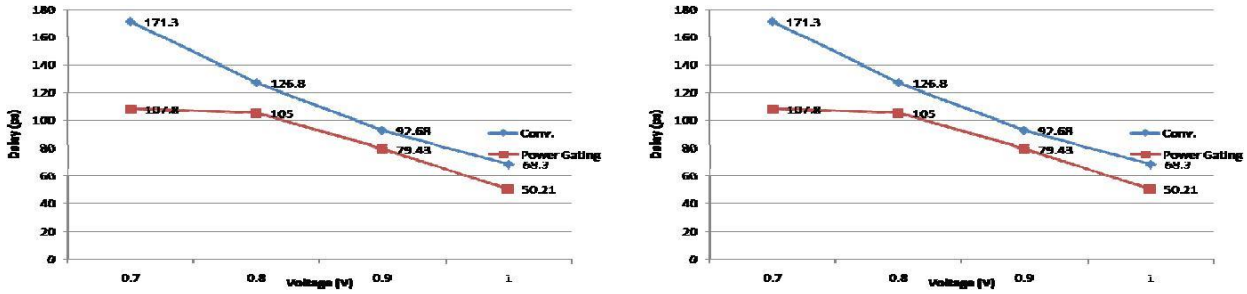

180
160
140
120
100
80
60
40
20
0
Delay (ps)
171.3
126.8
105
92.68
79.43
50.21
Conv.
Power Gating
0.7
0.8
0.9
1
Voltage (V)

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