Development of embedded webserver using soft core processor

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***Abstract* - Demand for High speed portable networks impels compulsory optimization in various aspects. A common web server is to act as a central control point which responds to the user request, and employing a high sophisticated computer for this purpose is not obligatory. The web server has the capability to adapt multipurpose operation, a client can share the web content not only the HTML files but also can control a device operated in a remote place through this web server.In this Project to design Embedded Web Server 1) Configuration of Embedded processors on the Field Programmable Gate Array (FPGA's) with Soft core technique. 2) Building Embedded Real Time Operating System (RTOS) on the soft core based Processor. 3) Developing and testing the networking based application on the NIOS II Soft core processor and to make this DE2 Board as a Embedded Web Server.**

***Keywords* - HTML, FPGA, RTOS, NIOS II**

1. INTRODUCTION

Embedded Systems are hardware and software components working together to perform a specific application. They can be found in places such as our automobiles, in the medical field, in industrial control systems, and in entertainment electronics. "An embedded system is a system that has software embedded into computer-hardware, which makes a system dedicated for an application (s) or specific part of an application or product or part of a larger system".
An Embedded Web Server (EWS) is a Web server which runs on an embedded system with limited computing resources to serve embedded Web documents to a Web browser. By embedding a Web server into a network device, it is possible to provide a Web-based management user interface, which are user-friendly, inexpensive, cross-platform, and network-ready.

2. METHODOLOGY

2.1 SOC Based Embedded System

A system on a chip (SOC) is an integrated circuit (IC) that integrates all components of a computer or other electronic system into a single chip. SoC (System-on- Chip) can be considered as a particular case of Embedded System.

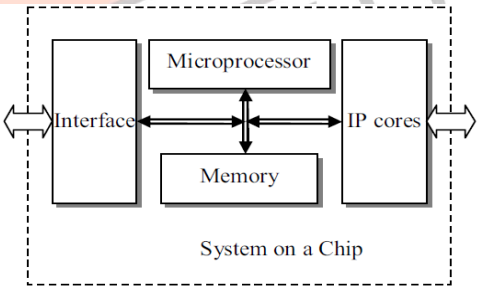


Fig: 2.1 SOC Based Embedded System

SoC design covers a lot of different viewpoints including as much the application modeling by the aggregation of functional components, as the assembly of existing physical components, as the verification and the simulation of the model system, as the synthesis of a complete end-product.

Advantages

- SOC designs usually consume less power and have a lower cost.
- Higher reliability than the multi-chip systems that they replace.
- Fewer packages in the system, assembly costs are reduced as well.

2.2 Block Diagram of NIOS II System

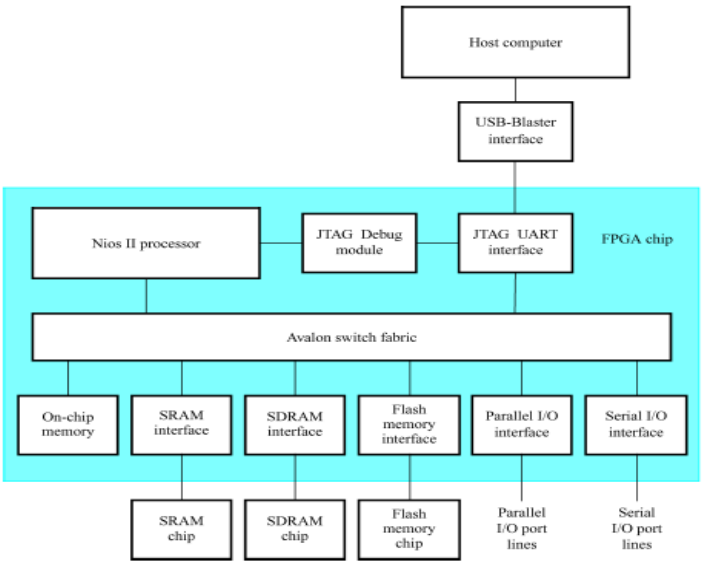


Fig. 2.1:- Block Diagram of NIOS II Soft core Processor

The NIOS II processor and the interfaces needed to connect to other chips on the DE2 board are implemented in the Cyclone II FPGA chip. These components are interconnected by means of the interconnection network called the Avalon Switch Fabric.
The memory blocks in the Cyclone II device can be used to provide an on-chip memory for the NIOS II processor. The SRAM, SDRAM and Flash memory chips on the DE2 board are accessed through the appropriate interfaces. Parallel and serial input/output interfaces provide typical I/O ports used in computer systems.

2.3 Operating System (µCLinux)

Except for simple applications, the usage of embedded operating systems assists in the design and implementation process. Embedded operating systems offer support for scheduling, task switching and I/O handling. Embedded operating systems (EOS) are essentially operating systems for embedded devices.
The typical characteristics of an embedded operating system are:-
1. Configurability
2. Lack of Protection Mechanisms
3. Limited I/O Drivers

3. TOOLS AND PLATFORM

3.1 ALTERA DE2 BOARD

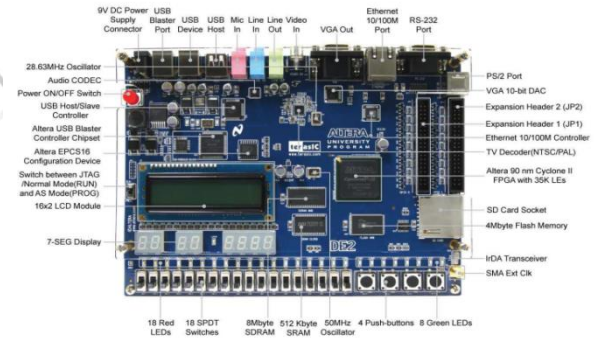


Fig.3.1 ALTERA DE2 board.

The purpose of this board is to provide the ideal vehicle for learning about digital logic, computer organization, and FPGAs. It uses the state-of-the-art technology in both hardware and CAD tools to expose students and professionals to a wide range of topics. The board offers a rich set of features that make it suitable for use in a laboratory environment for university and college courses, for a variety of design projects, as well as for the development of sophisticated digital systems.

3.2 ALTERA'S QUARTUS II

The Quartus II system includes full support for all of the popular methods of entering a description of the desired circuitinto a CAD system. This software uses the VHDL design entry method, in which the user specifies the desired circuit in the VHDL hardware description language. Two other methods available in this software are using Verilog hardware description language and defining the desired circuit in the form of a schematic diagram.

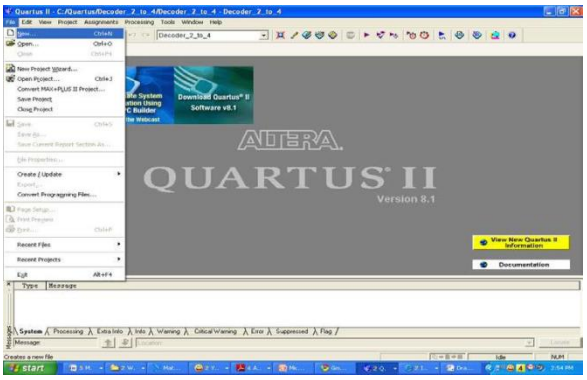


Fig.3.2 The Quartus II display

3.3 ALTERA'S SOPC BUILDER

The SOPC Builder is a tool used in conjunction with the Quartus II CAD software. Altera's Nios II is a soft processor is defined in a hardware description language. It can be implemented in Altera's FPGA devices by using the Quartus II CAD system. To implement the system in Fig., we have to instantiate the following functional units:

1. NIOS II processor, which is referred to as a Central Processing Unit (CPU).
2. On chip memory, which consists of the memory blocks in the Cyclone-series chip. we will specify a 4-Kbyte.
3. Two parallel I/O interfaces
4. JTAG UART interface for communication with the host computer.

4. DESIGN AND IMPLEMENTATION

System Design

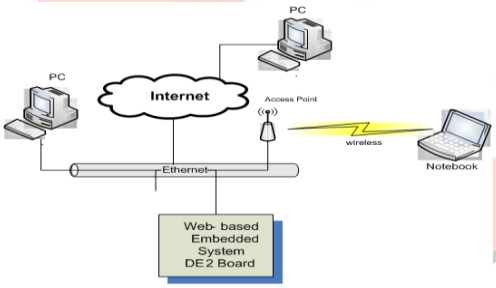


Fig.4.1: Web-based Embedded System on the Network.

A web server consists of three components: hardware, software, and content. The hardware component of a web server can be implemented with a solution as simple as a Ethernet-enabled microcontroller and a RJ45 connector with integrated magnetics. The microcontroller provides a glue less interface to the most popular implementation–twisted pair wiring. The processor integrated into the microcontroller provides the necessary processing performance to provide web services while also processing the application and interfaced devices.

Embedded Web server

This System diagram shows how to build a web server using DE2 board by using a NIOS II processor. The above figure describes the demo setup and connections. The NIOS II processor is running LWIP (Light Weighted TCP Internet Protocol) on the MICROC LINUX/OS-II RTOS. The web server uses the industry standard sockets interface to TCP/IP Protocol. It uses DHCP protocol to requests an valid IP from the Gateway. Users can use a web browser using LAN connection to examine the web page content stored in the Flash memory on the ALTERA DE2 board.

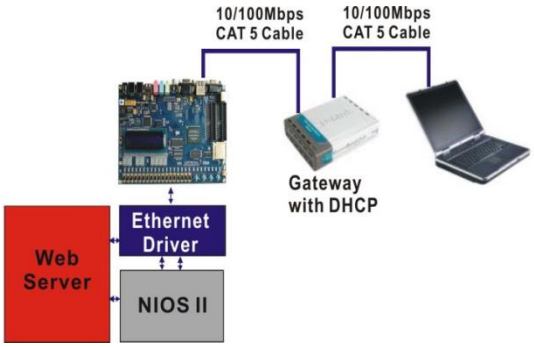


Fig.4.2:-System Architecture of WEB Server Design on DE2 Board

NIOS II System Development Flow

The Nios II development flow consists of three types of development: hardware design steps, software design steps, and system design steps, involving both hardware and software.

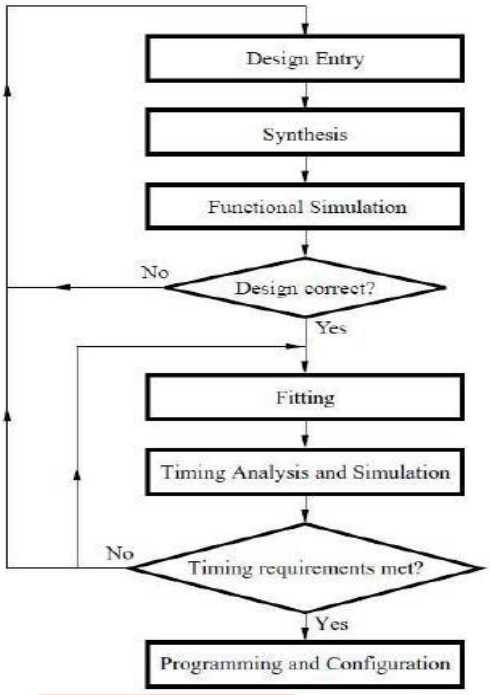


Fig. 4.3 :- NIOS II System Hardware design flow

1. Design Entry – the desired circuit is specified either by means of a schematic diagram, or by using a hardware description language, such as Verilog or VHDL.
2. Synthesis – the entered design is synthesized into a circuit that consists of the logic elements (LEs) provided in the FPGA chip.
3. Functional Simulation – the synthesized circuit is tested to verify its functional correctness. this simulation does not take into account any timing issues.
4. Fitting – the CAD Fitter tool determines the placement of the LEs defined in the netlist into the LEs in an actual FPGA chip; it also chooses routing wires in the chip to make the required connections between specific Les.
5. Timing Analysis – propagation delays along the various paths in the fitted circuit are analyzed to provide an indication of the expected performance of the circuit.
6. Timing Simulation – the fitted circuit is tested to verify both its functional correctness and timing.
7. Programming and Configuration – the designed circuit is implemented in a physical FPGA chip by programming the configuration switches that configure the LEs and establish the required wiring connections.

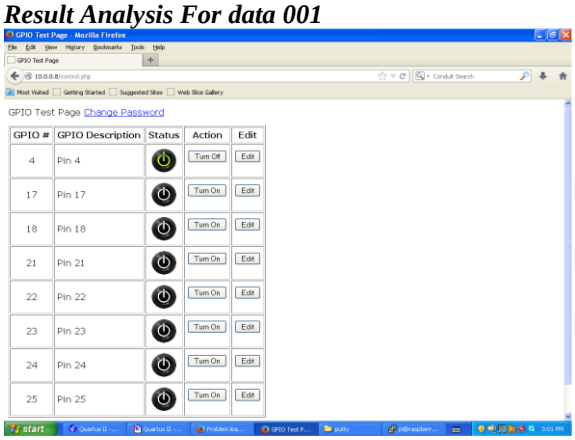
5. RESULT AND DISCUSSION

Testing of Embedded Webserver

Fig 6.1: Monitor Interfacing with DE2 Board for web server application

The above figure6.1 shows the interfaced monitor with the Altera's DE2 Board. In this figure DE2 Board is connected to the monitor with the help of LAN connection. By using IP Address the output will be shown on the monitor Screen. This VHDL code is compiled with QUARTUS II software provided.

Result Analysis For data 001



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CONCLUSION

This Project presents the development of WEB Server based on µCLINUX KERNEL in the NIOS II Core processors of ALTERA Cyclone II family FPGA board. To build a Embedded web server using DE2 board based on NIOS II Soft core processor. The NIOS II processor is running LWIP (Light Weighted TCP Internet Protocol) on the MICROC LINUX /OS-II RTOS.

The web server uses the industry standard sockets interface to TCP/IP Protocol. It uses DHCP protocol to requests an valid IP from the Gateway. Users can access the web browser using LAN connection to examine the web page content stored in the Flash memory on the ALTERA DE2 board. This FPGA DE2 Board can be used for distributed embedded systems. This board can be used for providing Ethernet communication to the system in which Ethernet support is not available.

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