# Implementation of 4-bit R-2R DAC on CADENCE Tools

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***Abstract*** **-An analog audio signal is continuously sampled; quantized and measured the height over time, and then the converted information is stored as series of numbers on the hard disk or in flash memory of an audio player. This series of numbers stored is known as** digital **audio signal. A compact disc (CD) stores these samples as 16-bit binary (1s and 0s) "words" 44K times a second, but digital audio data can be stored in a different sample rates, word sizes, and encoding or compression formats, and are brought to us on everything from our smartphone to your laptop. But in every case, the final thing that happens is the digital numbers get converted back into an analog electrical signal that can be sent to our headphones. The device that does this conversion is called a digital to analog converter (DAC).In this paper R-2R DAC converter is implemented on CADENCE tools with 180nm technology.**

***Index Terms*** **- DAC; CD; CADENCE; Technology.**

## I. INTRODUCTION

A Digital to Analog Converter plays an important role digital signal processing. The DAC converts a digital code to an equivalent analog signal such as a voltage, current, or electric charge. Signals can easily be stored and processed in digital form; a DAC is used for the signal to be recognized by human senses or non-digital systems.

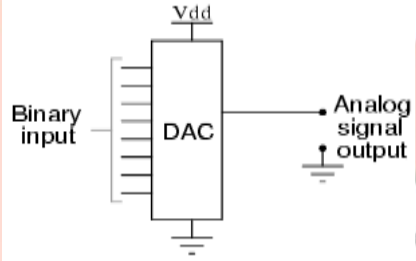


Fig 1: DAC block diagram

## II IMPLEMENTED ARCHITECTURE

To overcome huge range of resistor used in weighted resistor D/A converter, R-2R ladder D/Converter is introduced. In this paper a 4-bit R-2R ladder resistor DAC is implemented.

The basic theory of the R-2R ladder network is that current flowing through any input resistor (2R) encounters two possible paths at the far end. The total resistances of both paths are the same (also 2R), so the incoming current splits equally along both paths. The half-current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage. The half that takes the path towards the op amp along the ladder can affect the output. The inverting input of the op-amp is at virtual earth. Current flowing in the elements of the ladder network is therefore unaffected by switch positions. The output voltage equation of DAC is given by

$V0 = V_R*(R_F/R)[b1/2^1 + b2/2^2 + b3/2^3 + b4/2^4]$

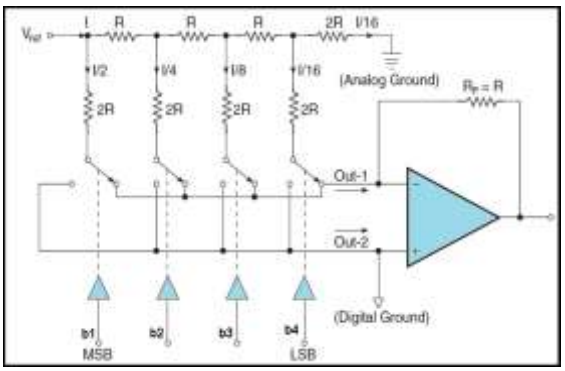


Fig 2: Implemented R-2R DAC

***A.OP-AMP***

The OP-AMP implemented in this paper is a two stage OP-AMP to get high gain.

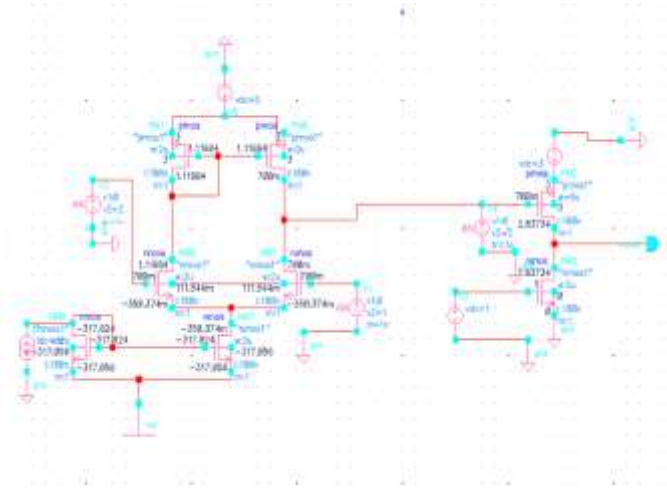

Fig 3: A two-stage OP-AMP

The first stage of OP-AMP consist of differential amplifier with current mirror is used to yield high gain, this stage rejects common mode signals like noise and amplifies differential signal.

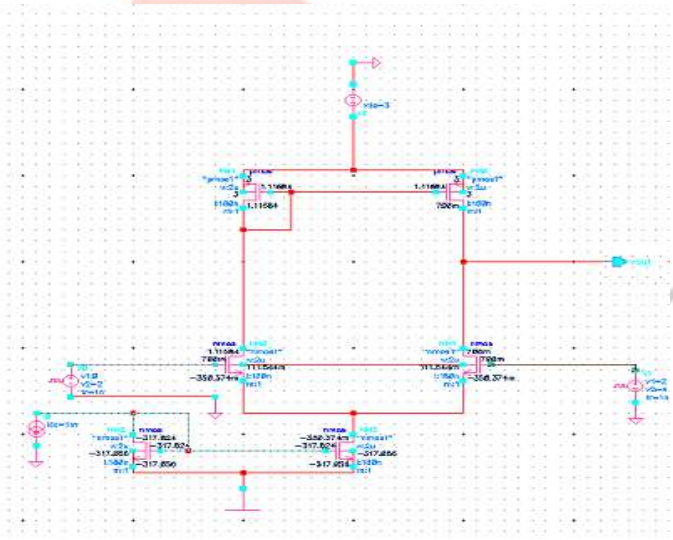

Fig 4: Differential amplifier stage

The second stage of is consists of common source amplifier. The output of differential l amplifier is connected to input of the common source amplifier. This stage increases the output swing and gain of differential stage. It acts a load. The load impedance can be increased by gain. Increasing the output impedance limits the gain.

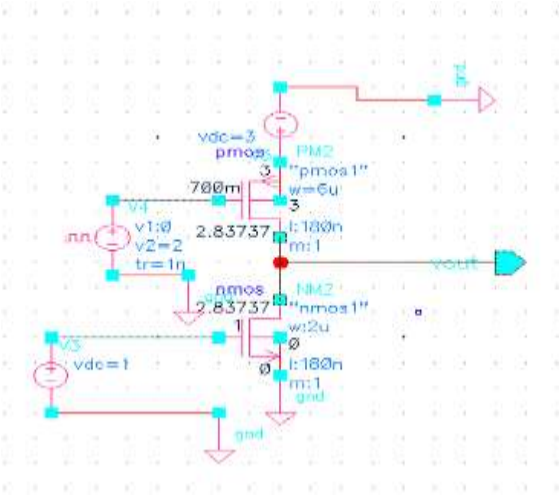


Fig 5: CS amplifier

**III DESIGN OF R-2R LADDER RESISTOR DAC**

Design of R-2R ladder resistor DAC starts with two stage OP-AMP. So, Op-amp with power consumption in the order of few microwatts is to be designed. Beginning with this given power, and using supply voltage of 1.8V in 180nm n-well CMOS technology, value of total current flowing through the op-amp is calculated. Input transistors are designed so that maximum current flows through them, as the input transistors decide the gain of op-amp. Since, digital to analog converter is designed for 4-bit resolution; hence, minimum op-amp gain required is given by 2N+1 i.e. 42dB and phase margin greater than 600 for system to be stable.

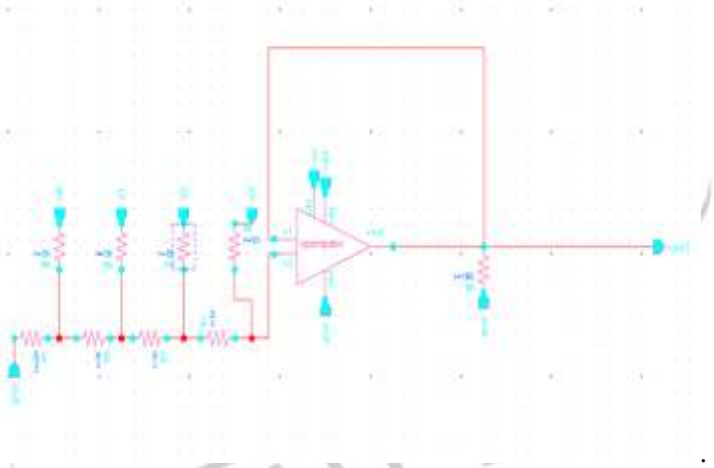

Fig 6: Design of R-2R ladder resistor DAC

***A Design of OP-AMP***

The op-amp is designed to meet high gain requirements.

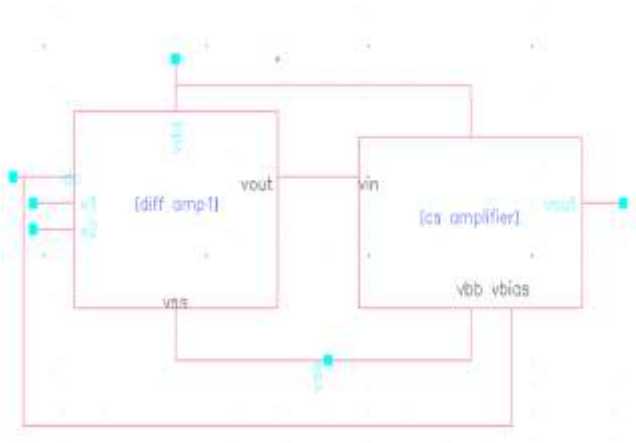


Fig: Schematic of OP-AMP

***Equations***

From slew rate and capacitance we can find current flowing through transistor

$$slew\ rate\left(\frac{dv}{dt}\right) = \frac{I}{CL} \quad \text{.....(1)}$$

As M1 and M2are in saturation region using equation Vds>Vgs-Vt, as Vt=0.4v
The current equation in saturation region is

$$Ids = \frac{\beta}{2(Vd - Vs)^2} \quad \text{.....(2)}$$

$$Ids = \frac{\mu Coxw}{2L(Vd - Vs)^2} \quad \text{.....(3)}$$

$$gm = \frac{\partial Ids}{\partial Vgs} \quad \text{.....(4)}$$

$$\text{Gain bandwidth} = \frac{gm}{2\pi fCl} \quad \text{.....(5)}$$

$$\frac{W}{L} = \frac{gm^2}{2Ids\mu Cox} \quad \text{.....(6)}$$

For calculating (W/L) ratio of M3 &M4 eq. (1&2) will used. M1 & M2 eq.(3,4,5,6) will used and for M5,M6 eq.3 will used.

## IV SIMULATION RESULTS

***Differential amplifier results***

***CS amplifier results***

***Op-amp results***

***R-2R ladder resistor DAC results***

**V PERFORMANCE SUMMARY**

| Input(binary) | Output voltage(v) |
|---|---|
| 0000 | 0.00 |
| 0001 | -1.25 |
| 0010 | -2.50 |
| 0011 | -3.75 |
| 0100 | 5.00 |
| 0101 | -6.25 |
| 0110 | -7.50 |
| 0111 | -8.75 |

Table 1 Performance summary

## CONCLUSION

In this paper R-2R ladder resistor DAC is implemented and investigated .The DAC is designed to verify the characteristics. A DAC with two stages OP-AMP is designed to get high gain. The designed DAC is simulated using CADENCE 180nm technology with a gain of 50dB is achieved. Power dissipation is achieved by 480µw.

## FUTURE WORK

In this paper 4-bit R-2R DAC is designed, this can be increased further and power dissipation can also be reduced.

## ACKNOWLEDMENTS

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