Pseudo Linear Enhanced Phased-Locked Loop (PL-EPLL) based Control Algorithm for Three-Phase DSTATCOM in Three -Wire Power Distribution System

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***Abstract*- This paper presents an implementation of pseudo linear enhanced phased-locked loop control algorithm in three-leg Voltage Source Converter (VSC)-based Distribution Static Compensator (DSTATCOM) in three-wire power distribution system. This control algorithm is used for withdrawal of load fundamental active and reactive power components of distorted load currents for estimation of reference source currents. The PWM signals for the VSC based DSTATCOM are derived from the estimated reference source currents. The proposed control algorithm is implemented for mitigating multiple power quality issues such as load unbalancing, reactive power and current. The performance of the DSTATCOM is found satisfactory with the proposed control algorithm under non linear load. The dc bus voltage of the VSC of DSTATCOM has a negligible effect on varying loads.**

***IndexTerms* - Distribution Static Compensator (DSTATCOM), Pseudo Linear Enhanced Phased-Locked Loop (PL-EPLL) Control Algorithm, Voltage Source Converter, Power Quality**

I. INTRODUCTION

The proliferation of power-electronics-based equipment linear, nonlinear or mixed type of loads has provoked power quality problems in the distribution systems. They cause various types of power quality disturbances such as poor power factor, wave form distortion, fluctuations in voltages or currents in supply systems [1], [2]. Power electronics –based shunt custom power device, called the distribution static compensator (DSTATCOM), injects currents at point of common coupling (PCC) so that load balancing, power factor correction and harmonic filtering can be achieved. There are different topologies reported in the literature for three-phase three wire Voltage Source Converter (VSC) based DSTATCOM [3],[4].The operation of VSC is supported by a dc storage capacitor with proper dc voltage across it. One important aspect of compensation is extraction reference currents from distorted load currents to monitor and eliminate power quality problems. Traditionally, control of a VSC based DSTATCOM utilizes the standard decoupled d-q vector controlled approach for power quality improvement. The performance of the controller has not been analyzed when converter operates beyond the linear modulation limit.

One of the researches focuses on the control algorithm based on instantaneous symmetrical component theory for estimation of reference compensator currents [5]. The researcher had not given attention to reactive power compensation, load balancing and harmonic elimination. Pinaki Mitra et al [6] discuss an adaptive control strategy for DSTATCOM applications in an electric ship power system in order to maintain the voltage at the point of common coupling. The optimal parameters of the controller are obtained by using particle swarm optimization algorithm. An area of adaptive control provides an automatic tuning procedure in a closed loop for the controller parameters [7]. The ability of the control algorithm to extract necessary information from real on line data in order to tune the controller is also used for grid synchronization. Bhim Singh et al.[8] have discussed a comparative study of adaptive control algorithms for DSTATCOM. An adaptive theory based algorithm provides an approach for self control of controllers in real time to achieve a desired level of performance. The selection of parameters for the control algorithm is a vital issue in the works aiming for controlling and mitigating the power quality problems.

In this paper, pseudo linear enhanced phased –locked loop based control algorithm is implemented in three –phase DSTATCOM for mitigation of power quality problems such as load balancing, reactive power compensation and harmonic elimination in three- phase three wire distribution system. The advantages of this algorithm are that it is not affected with the input signal magnitude variation. Also it is considerably fast, accurate and robust with double frequency ripples available in the input signal. PL-EPLL exhibits high structural robustness with respect to real time implementations using field programmable gate arrays (FPGAs) for fast, accurate and reliable performance. Moreover, it provides direct computation of fundamental active and reactive power components from distorted load currents. Further, it is able to achieve harmonic mitigation as per IEEE-519 standard with various loads under steady state and dynamic performance [9].

II. CONFIGURATION OF DSTATCOM AND CONTROL ALGORITHM

Fig.1. shows a three-phase, three-wire compensated system using VSC topology based DSTATCOM with non linear load. The DSTATCOM consists of six insulated-gate bipolar transistor (IGBT) switches each with an anti parallel diode; three interface inductor *(L_f)* and dc storage capacitor C_{dc}. A small resistance R_f and capacitance C_f are connected in series represent the ripple filter installed at point of common coupling (PCC) to attenuate the high frequency switching noise. The source voltages are considered as a stiff source with negligible feeder impedance. The VSC based DSTATCOM operate under the PI control mode due to their simplicity, fast response in order to tack the desired compensator currents. The DSTATCOM injects harmonics/reactive currents into the PCC in such a way as to cancel the harmonics/reactive power component of the distorted load currents [10]-[14]. The primary function of the three-phase DSTATCOM maintains the balanced sinusoidal source currents with unity power factor.

A block diagram of the pseudo linear enhanced phased –locked loop based control algorithm for generation of reference source currents is shown in Fig.2. It is used for computation of fundamental active and reactive power components of reference source currents with unit vector of PCC voltages [15]-[23]. The PCC two phase line voltages measured and converted to three- phase voltages, which is used to estimate in-phase unit templates as well as amplitude of PCC voltages (V_t) as follows

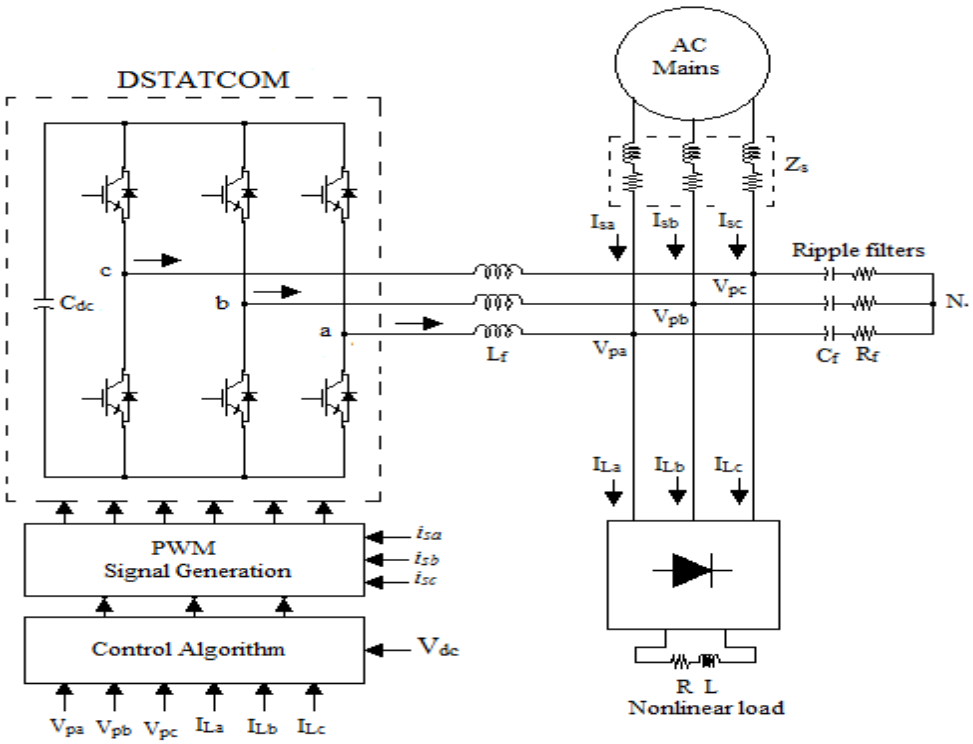


Fig. 1. Schematic diagram of the VSC-based DSTATCOM

$$V_t = \sqrt{\frac{2\left(v_{pa}^2 + v_{pb}^2 + v_{pc}^2\right)}{3}} \tag{1}$$

The unit templates (u_{ap}, u_{bp}, u_{cp}) in phase of PCC voltages are expressed as

$$u_{ap} = \frac{v_{pa}}{V_t}, \quad u_{bp} = \frac{v_{pb}}{V_t}, \quad u_{cp} = \frac{v_{pc}}{V_t} \tag{2}$$

The quadrature unit templates (u_{aq}, u_{bq}, u_{cq}) are estimated by the following set of equations

$$u_{aq} = \frac{\left(-u_{bp} + u_{cp}\right)}{\sqrt{3}}, \; u_{bq} = \frac{\left(3u_{ap} + u_{bp} - u_{cp}\right)}{2\sqrt{3}}, \; u_{cq} = \frac{\left(-3u_{ap} + u_{bp} - u_{cp}\right)}{2\sqrt{3}} \tag{3}$$

The unit template values are used to estimation of active and reactive components of source currents.

III. EXTRACTION OF AVERAGE FUNDAMENTAL ACTIVE AND REACTIVE POWER COMPONENTS OF SOURCE CURRENTS

In polluted load currents, the fundamental active power components, reactive power components, harmonics and dc components are the major components. The pseudo linear enhanced phased locked loop (PL-EPLL) is used to extract the phase 'a' load fundamental current I_{La} as shown in Fig.2. In the extraction process, phase 'a' fundamental load current is subtracted from the load current to estimate the current error signal. In the general PLL and EPLL's behavior depends on the input signal magnitude. This is a main drawback in cases where the input signal magnitude causes wide range of changes. Once planned for the value of input magnitude, the PLL and EPLL responses tend to unsteadiness when the magnitude becomes high while they become lethargic when the magnitude becomes small. The PL-EPLL is an improved approach of EPLL which is independent of the input signal magnitude The PL-EPLL is described by the subsequent set of equations [24].

$$\dot{I}_0 = k_1 e \sin\varphi_0,\ \dot{\Delta\omega}_0 = \frac{k_2 e}{I_0}\cos\varphi_0,\quad \dot{\varphi}_0 = \omega_n + \Delta\omega_O + \frac{k_3 e}{I_0}\cos\varphi_0 \qquad (4)$$

As stated in the succeeding theorem, performance of the PL-EPLL represented by set of Eq.4 does not depend on the signal magnitude. The PL-EPLL internal parameters k_1, k_2, and k_3 are used as respectively, to control steady state and transient performance.

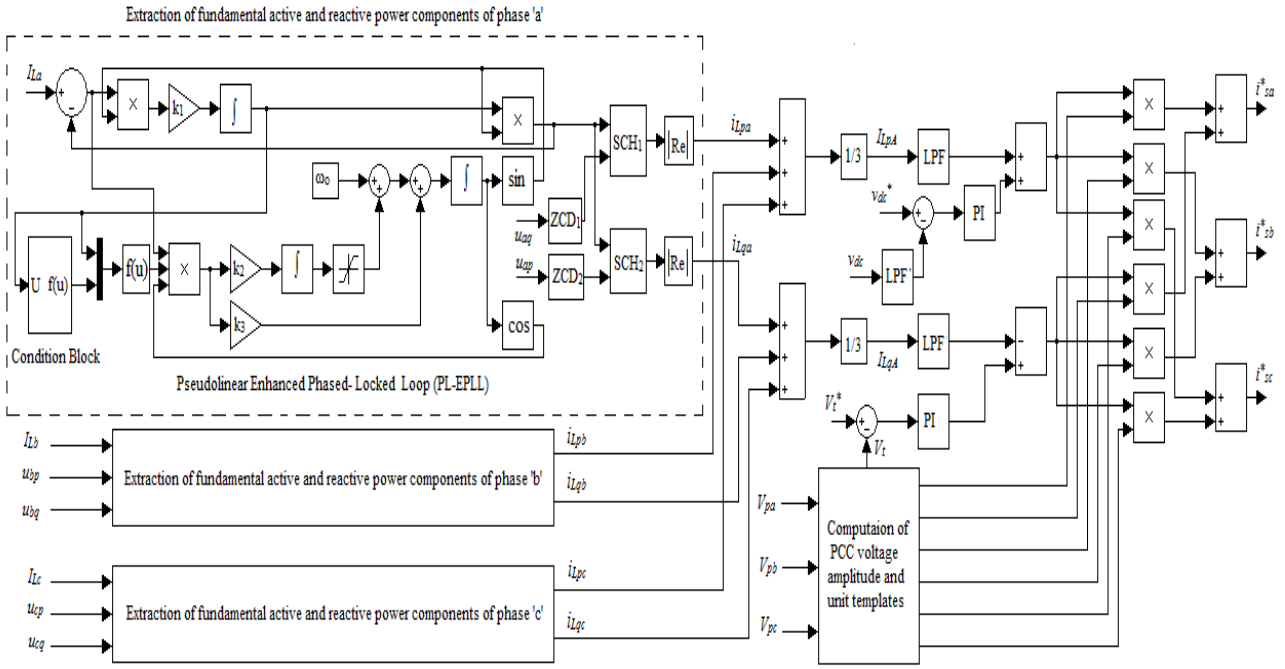


Fig. 2.Reference current generation using Pseudo linear enhanced phased locked loop (PL-EPLL) based control algorithm

Theorem: The input current signal of $i = I_i \sin\phi_i$, $\phi_i = \int_0^t \omega_i(\tau)d\tau + \delta$ of the pseudo linear enhanced phased locked loop described by the equations set 4. It has three internal parameters with two equilibrium solutions at the point $P_1 = (I_{01}, \omega_{01}, \phi_{01}) = (I_i, \omega_i, \phi_i)$ and point $P_2 = (I_{02}, \omega_{02}, \phi_{02}) = (-I_i, \omega_i, \phi_i + \pi)$. Both equilibrium points are asymptotically stable and the eigen values of the linearized system are equal to

$$\lambda_1 = \frac{k_1}{2},\quad \lambda_{2,3} = -\zeta\omega_r \pm j\omega_r\sqrt{1-\zeta^2},\quad \omega_r^2 = \frac{k_2}{2},\quad 2\zeta\omega_r = \frac{k_3}{2} \qquad (5)$$

This theorem represent that the transient response of the PL-EPLL does not depend on the input signal magnitude. In the PL-EPLL, the estimated amplitude can be negative so that a correction should be made to drive the actual estimated values. The corrections are made as follows

$$I_0^c = \text{sign}(I_0)I_0,\quad \varphi_0^c = \varphi_0 + \frac{1-sign(I_0)}{2}\pi,\quad S^c = sign(I_0)S \qquad (6)$$

In the above equations 'c' stands for corrected variable and sign (I_o) is the sign function that is equal to 1 when (I_o) is positive and equal to -1 when (I_o) is negative. The function 'f 'is defined as $f(I_o) = 1/I_o$ in the PL-EPLL, it can modified to

$$f(I_0) = \frac{sign(I_0)}{|I_0| + \varepsilon} \qquad (7)$$

Where ϵ is a small positive number. It can be set at *x*% of the nominal value of the input signal magnitude, such as x=1 or x=0.5. Thus $\epsilon=0.01xI_n$, where I_n is the nominal value of the input signal magnitude. The function '*f*' operates like a switch that disconnects the input signal when it is in abnormal conditions. A suggestion for '*f*'

$$f(I_0)=\begin{cases}\dfrac{sign(I_0)}{|I_0|+\varepsilon} & I_0^{\min}\le|I_0|\le I_0^{\max}\\ 0 & otherwise\end{cases} \tag{8}$$

Where I_o^{min} and I_o^{max} are the minimum and maximum admissible ranges of the input signal magnitude for specific applications. A zero crossing detector (ZCD_1) is used with quadrature unit template (u_{aq}) to produce trigger pulse. An output of the zero crossing detector is used with i_{Lpa} as the input of sample and hold circuit (SCH_1) to extract the amplitude of the active power component of load current phase 'a'. At the same time, other phases 'b' and 'c' load fundamental active power currents components i_{Lpb}, i_{Lpc} also extracted. A another unit of the zero crossing detectors (ZCD_2) is used with in phase unit template (u_{ap}) to operate the (SCH_2) with i_{Lqa} in order to extract the amplitude of the reactive power component of load current phase 'a'. Simultaneously other phases 'b' and 'c' load fundamental active power currents components i_{Lqb}, i_{Lqc} also extracted. The average magnitude of fundamental active power component of reference source currents is stated as

$$I_{LpA}=\frac{1}{3}\left(i_{Lpa}+i_{Lpb}+i_{Lpc}\right) \tag{9}$$

In the same method, the average magnitude of fundamental reactive power component of reference source currents is also calculated. Its expression is given as

$$I_{LqA}=\frac{1}{3}\left(i_{Lqa}+i_{Lqb}+i_{Lqc}\right) \tag{10}$$

IV. Amplitude of Active Power Loss of Reference Source Currents

The amplitude of active power loss component of reference source current is calculated as follows. Here the basic PI controller is used to measure active power loss component. The sensed dc bus voltage is send through a low pass filter to attenuate ripple components. A reference dc bus voltage (V^*_{dc}) and filtered dc bus voltage (V_{dc}) through low pass filter are compared and an error (V_{dce}) is given to the PI controller. The output of the dc bus PI controller is considered as active power loss component.

$$I_{dcp}(n)=I_{dcp}(n-1)+K_{dp}\left\{v_{dce}(n)-v_{dce}(n-1)\right\}+K_{di}v_{dce}(n) \tag{11}$$

Where K_{dp} and K_{di} are the proportional and integral gain constants of the dc bus PI controller.

V. Amplitude of Active Power Component of Reference Source Currents

As stated earlier, the amplitude of active power component of reference source current is estimated by addition of active power loss component of DSTATCOM and average amplitude of active power component. The PI controller parameters selection is also very important to obtain a perfect compensation. If any changes in the load it is directly affected dc link voltage of the DC bus in the compensator. The source current is computed by using the following equation

$$I_{spt}=I_{dcp}+I_{LpA} \tag{12}$$

VI. Amplitude of Reactive Power Component of Reference Source Currents

The reactive power components of reference source currents are computed from the output of PCC voltage. A voltage error (V_t) is the difference between the selected reference voltage and sensed amplitude of PCC voltage at the *n*th sampling instant as given to the PI controller. The output of the PI ac voltage controller is used for maintaining the PCC voltage at a constant value at *n*th sampling instant is expressed as [25]

$$I_{acq}(n)=I_{acq}(n-1)+K_{dp}\left\{v_{te}(n)-v_{te}(n-1)\right\}+K_{di}v_{te}(n) \tag{13}$$

Where K_{dp} and K_{di} are the proportional and integral gain constants of the ac bus PI controller. The amplitude of instantaneous value of reactive power components (I_{sqt}) of the reference source current is calculated as

$$I_{sqt}=I_{acp}+I_{LqA} \tag{14}$$

V. EXTRACTION OF REFERENCE SOURCE CURRENTS AND GENERATION OF PWM SIGNALS

Three-phase reference active and quadrature components of currents are computed using an amplitude of three-phase (a, b, and c) load active and quadrature components, in-phase PCC voltages active and reactive unit templates as

$$i_{sap} = I_{spt}u_{ap}, \quad i_{sbp} = I_{spt}u_{bp}, \quad i_{scp} = I_{spt}u_{cp} \tag{15}$$

$$i_{saq} = I_{sqt}u_{aq}, \quad i_{sbq} = I_{sqt}u_{bq}, \quad i_{scq} = I_{sqt}u_{cq} \tag{16}$$

Finally, the reference source currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) are computed by the summation of reference active and quadrature power components of currents as

$$i^*_{sa} = i_{sap} + i_{saq}\ , \ i^*_{sb} = i_{sbp} + i_{sbq}\ , \ i^*_{sc} = i_{scp} + i_{scq} \tag{17}$$

The reference source currents (i^*_{sa}, i^*_{sb}, i^*_{sc}) and sensed source currents (i_{sa}, i_{sb}, i_{sc}) are given to the error detector for respective phases and each phase current error is amplified using PI controller and their outputs are compared with a carrier signal of 10KHz to generate the PWM signals for VSC based DSTATCOM.

VI. SIMULATION RESULTS AND DISCUSSION

A simulation model of a PL-EPLL based DSTATCOM is developed by using Sim Power System tool boxes available in the MATLAB environment. The performance of the PL-EPLL control algorithm in the time domain for the DSTATCOM is simulated for PFC and ZVR modes of operation. The performance of the control algorithm is discussed under linear and nonlinear loads. Simulation parameters are shown in appendix.

A. Dynamic Performance of DSTATCOM in PFC mode

The performance of a VSC based DSTATCOM in PFC mode under linear load is shown in Fig.3. The wave form shows PCC phase voltage (V_s), load currents (I_L), source currents (I_S), compensator current (i_{Ca},i_{Cb},i_{Cc}) and voltage across the capacitor (V_{dc}) are shown during load variation (at t=0.5s to 0.7s). It shows the satisfactory performance of compensator for the function reactive power compensation and load balancing.

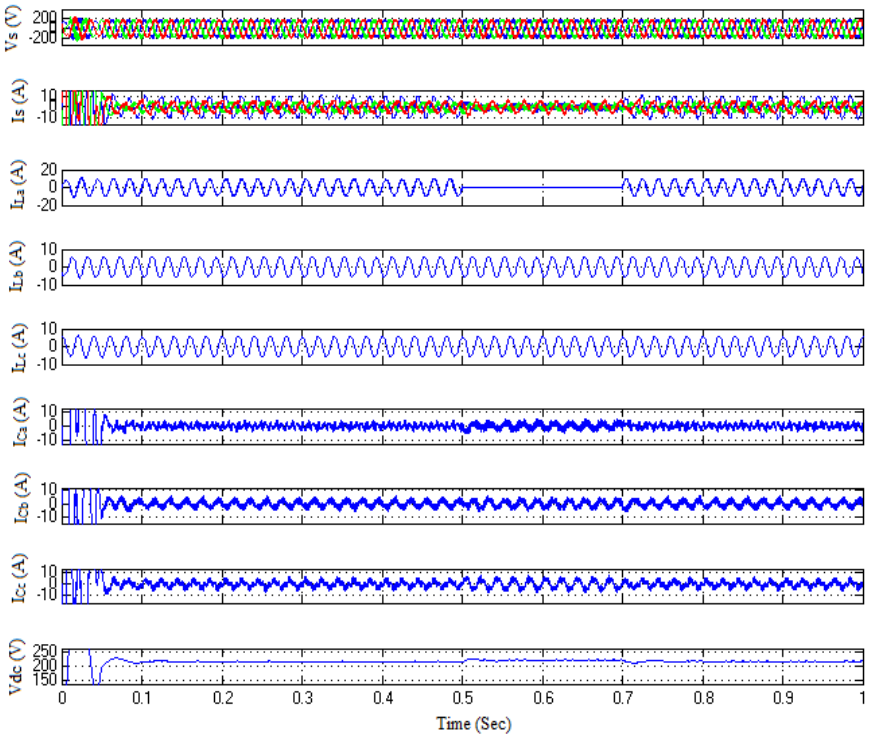


Fig. 3. Dynamic performance of DSTATCOM in PFC mode under linear load

Similarly, an uncontrolled rectifier as a nonlinear load is connected to the supply system. The dynamic performance of the wave form shows PCC phase voltage (V_s), load currents (I_L), source currents (I_S), compensator current (i_{Ca},i_{Cb},i_{Cc}) and voltage across the capacitor (V_{dc}) are shown during load variation (at t=0.5s to 0.6s) as shown in Fig.4. It shows the satisfactory performance of compensator for the function reactive power compensation and load balancing.

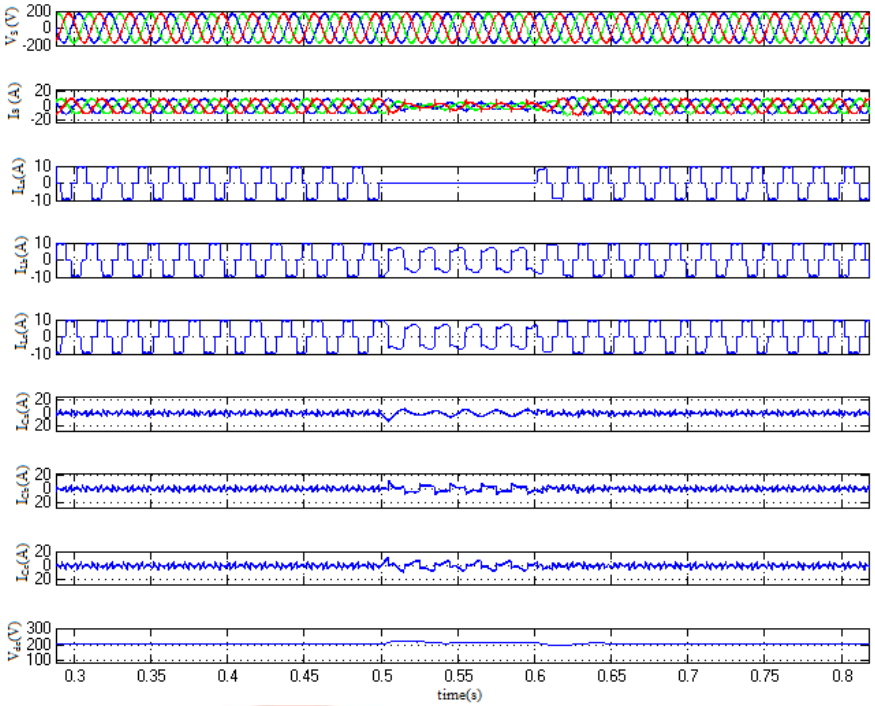


Fig. 4. Dynamic performance of DSTATCOM in PFC mode under varying non linear load

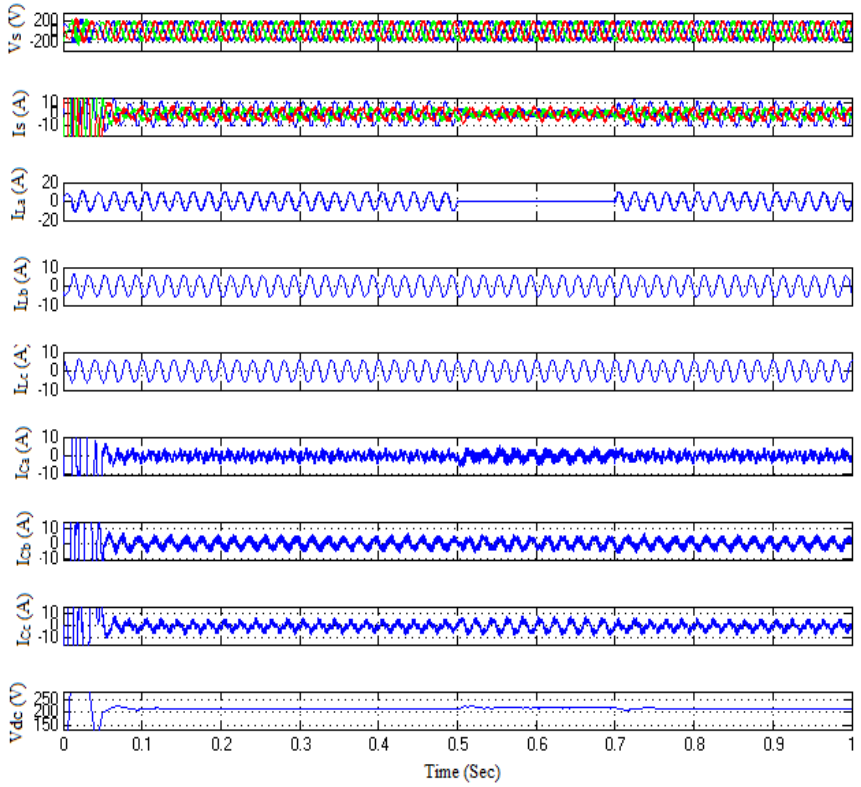


Fig. 5. Dynamic performance of DSTATCOM in ZVR mode under linear load

B. Dynamic Performance of DSTATCOM in ZVR mode

The dynamic performance of DSTATCOM in ZVR mode under linear load is shown in Fig.5. It shows different wave forms PCC phase voltage *(V_s)*, source currents *(I_S)*, load currents *(I_L)*, shunt compensator currents *(i_{Ca},i_{Cb},i_{Cc})* and voltage across the capacitor *(V_{dc})* during load disturbance (at t=0.5s to 0.7s). Similarly, an uncontrolled rectifier as a nonlinear load is connected to the supply system. The dynamic performance of the wave form shows PCC phase voltage *(V_s)*, load currents *(I_L)*, source currents *(I_S)*, compensator current *(i_{Ca},i_{Cb},i_{Cc})* and voltage across the capacitor *(V_{dc})* are shown during load variation (at t=0.5s to 0.6s) as shown in Fig.6. In Fig.7.(a-c), exactly shows THD % of the phase 'a' at PCC voltage, load current, source current, are 2.02%, 29.98% and 3.25% respectively. The performance of the DSTATCOM is found satisfactory for the functions of load balancing, power factor correction and harmonic elimination.

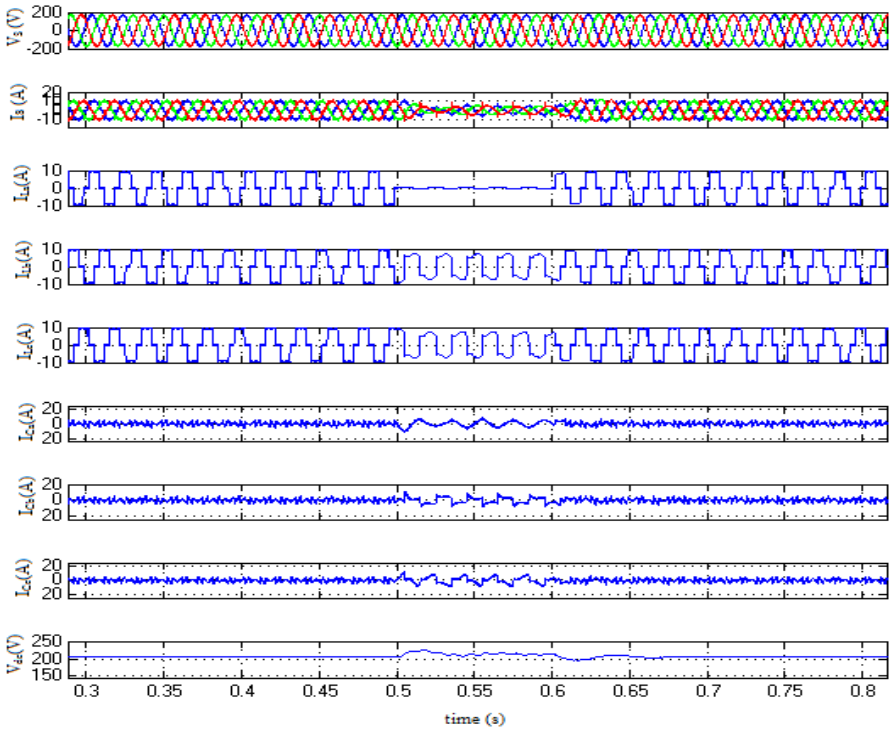
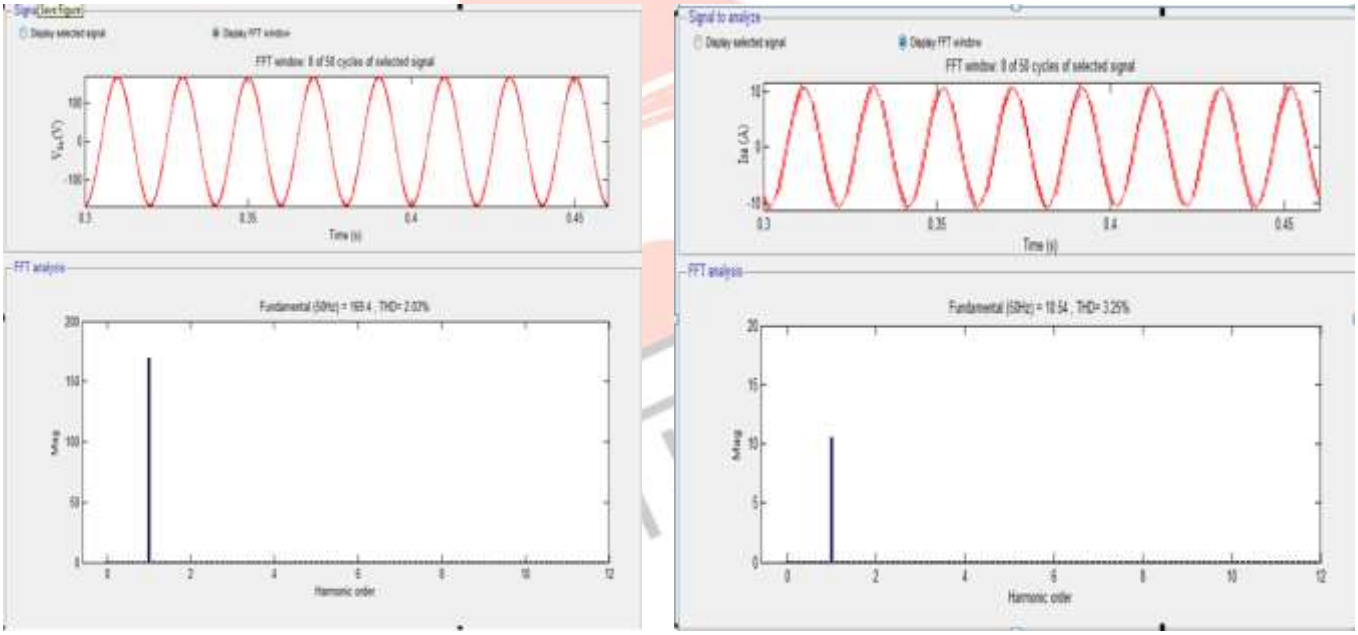
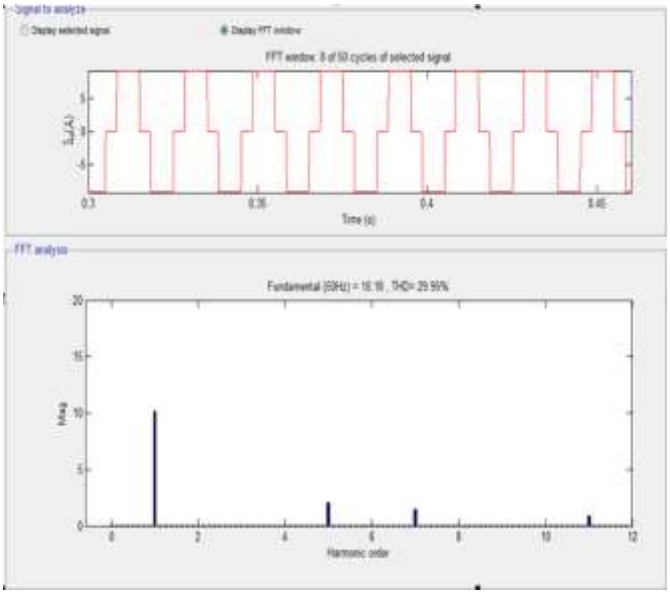


Fig. 6. Dynamic performance of DSTATCOM in ZVR mode under non linear load



(a) (b)



(c)

Fig. 7. (a-c). Waveforms, THD and harmonic spectrum at ZVR mode

The dynamic performance of DSTATCOM is discussed through simulation results at different operating mode PFC and ZVR mode under non linear load .The two modes of operation gives the clear function of DSTATCOM. During PFC mode of operation the PCC voltage regulator is not considered. The THD of the source voltage, load current and source current are controlled with in limit. The performance of the DSTATCOM is found satisfactory for the functions of load balancing, power factor correction and harmonic elimination.

Appendix

Ac mains: three-phase, 120V (L-L), 50Hz, Linear load: resistive load bank 69 V (phase), 35Ω and series combination of 14Ω and inductor 80mH load boxes; Non linear load: three phase full- bridge uncontrolled rectifier with R=17.5Ω and L=90mH, dc-bus capacitance: 1650μF; Gains of PI dc voltage regulator: Kp=0.65, Ki=0.1, Gains of PI dc voltage regulator: Kp=0.4, Ki=0.22, reference dc-bus voltage: 220V; interfacing inductor Lf=2.25mH; cutoff frequency of a low pass filter used in dc bus=10Hz

VI. CONCLUSION

In this paper, the PL-EPLL based control algorithm on a DSTATCOM has been implemented in three-phase three wire distribution system. Three-leg VSC has been used as DSTATCOM in this implementation. The control algorithm has been used for computation of reference source currents to generate the gating signals of IGBTs for the VSC based DSTATCOM. Different functions of DSTATCOM such as, harmonic elimination, reactive power compensation and load balancing have been demonstrated. The THD of the source current using the applied control algorithm is well below 5%, the harmonic limit imposed by IEEE-519 standard. From the simulation results, it is concluded that the PL-EPLL based control algorithm has been found satisfactory for compensation of linear and non linear loads.

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