Review Paper on the Noise Shaping Property of 4th order VCO based ADC by using Feedback Loop

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***Abstract* – This paper presents the review of different order voltage control oscillator analog to digital converter (VCO-ADC) and their SNR calculation. The 4th-order Continuous Time(CT) delta-sigma VCO-ADC has been explored on a 0.13 µm CMOS with a measured performance of 81.2/78.1dB Signal to noise ratio(SNR)/Signal to noise distortion ratio(SNDR) over a 20 MHz bandwidth while consuming 87 mW from a 1.5 V supply and is occupying an active area of 0.45 mm^2. The 4th order noise shaping which is achieved by putting the quantization error in the feedback loop eliminates the *Kv* non-linearity of the circuit. Noise shaping works by putting quantization error in the feedback loop Main purpose of noise shaping is to increase the SNR of the resultant signal.**

***Index Terms* - VCO-ADC, SNR, noise shaping, quantization error, *Kv* non-linearity.**

I. INTRODUCTION

With the continuous scaling of the CMOS technology according to Moore's law, digital integrated circuits benefit simultaneously from double the speed and half the area (cost) every two years. But the impact of Moore's law is different on analog integrated circuits, since their performances are fundamentally limited by the trade-off between speed, accuracy and power [4].

One of the most promising analog to digital converter (ADC) architectures now a days is the VCO based ADC. VCO-ADCs as first-order sigma-delta modulators have been described in [1], [2] and as second order sigma delta modulator in [3],[4], the difference in both the orders is mainly the noise shaping property of the signals. Ref.[3] uses a dual-modulus divider, the quantizer output need not be fed back to the input of the VCO. Therefore, the VCO input is influenced only by a band-limited input signal, and accurate voltage-to-phase integration is achieved. The circuit in [4] focuses mainly on the Spurious-Free Dynamic Range (SFDR) for the noise shaping of the signal. The [5] allows the evaluation of the peak SQNR and dynamic range of a VCO-ADC at the system level design stage. This analysis is necessary before any other circuit-related consideration such as distortion, thermal noise, or clock jitter. In recent years, several publications [6-9] have demonstrated that the ring VCO based time-domain delta-sigma ADC has many promising advantages compared with the conventional voltage-based ones, such as an order of magnitude reduction in chip area, a high DC gain and a reduced design complexity by replacing many circuit blocks such as the integrators, digital to analog converters (DAC), quantizer… [10] by only a ring VCO and some standard digital blocks [6]. Besides these advantages, there are also inevitable drawbacks. The primary one is the severe nonlinearity of the *Kv* (the voltage to frequency conversion coefficient of the VCO), which limits the linearity of the published designs to mostly between 30- 50dB [6][8][9].

A VCO has two traits that are especially attractive and relevant in the design of CT ΔΣ ADC's. First, the VCO behaves as a CT voltage-to-phase integrator. Second one is the digital nature of a ring-VCO's outputs. While the VCO output phase and frequency are continuously varying, the VCO output itself toggles between two discrete levels, *VDD* and GND, much like a CMOS digital gate. A serious drawback of this multi-phase approach, however, is that the counter becomes proportionately more complicated to design, and typically consumes greater power and area in order to meet timing and data throughput constraints. At the same time, both the single phase and multi-phase VCO-based ADC must contend with error incurred when the counter misses a VCO edge during reset.

A continuous time delta sigma (CT-ΔΣ) architecture proposed in [11] achieved second order noise shaping by preceding the multi-phase VCO quantizer with an op-amp based integrator, and using a multi-bit feedback DAC. The Discrete time(DT) ΔΣ architecture in [12] tried to bypass a multi-bit DAC implementation and the required dynamic element matching (DEM) overhead by using a frequency difference detector that pulse-width modulated a one-bit DAC.

However, this approach had additional complexities in the frequency difference detector design, and lost the inherent first-order noise-shaping provided by the VCO quantizer. A modified version of the ADC in [13] was actually implemented and provided measured results in [14]. Ref [14] shows that the third-order CT ΔΣ ADC achieved an extra order of noise shaping without a second op-amp integrator by creating a passive pole with a large on-chip capacitor. Figure. 1 shows the third order noise shaping of VCO-ADC.

The main problem that all the three orders VCO-ADC faced was the non-linearity, though it was reduced in the third order VCO-ADC but was not completely eliminated from the circuitry (as the order of the ADC increases, non-linearity decreases). The measured results presented in [14] demonstrated the benefits of using negative feedback with a high gain loop filter to

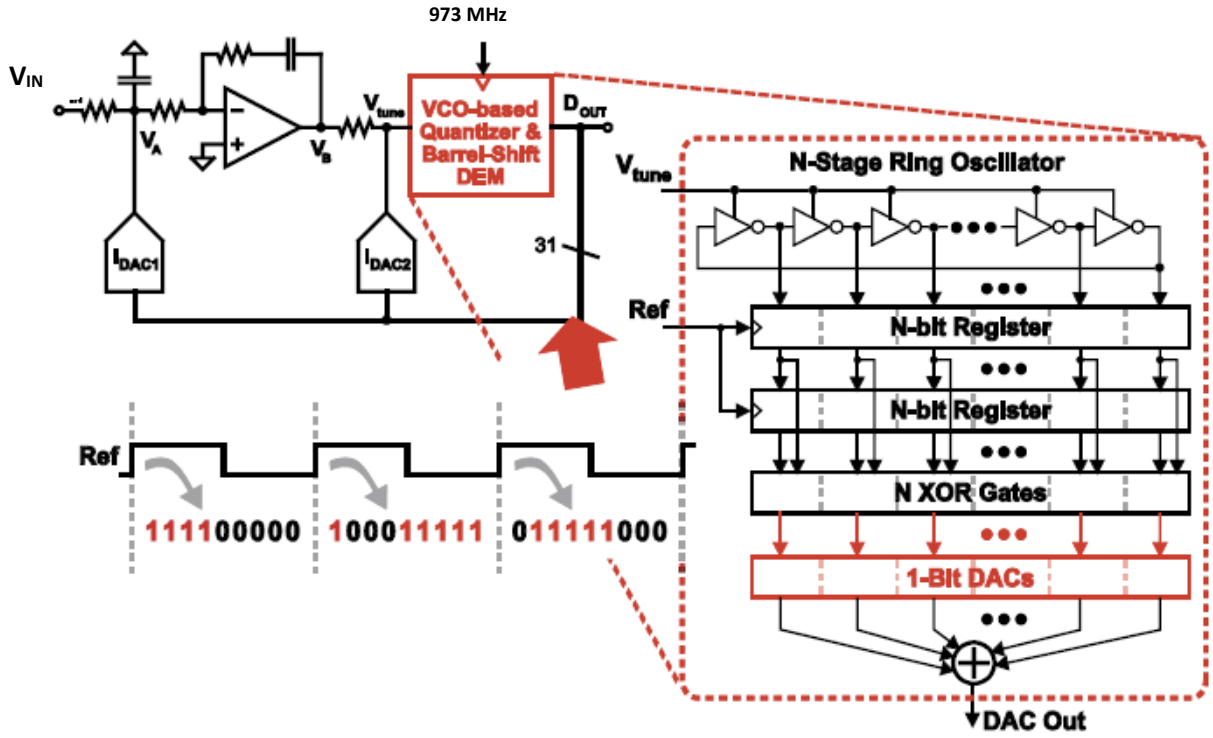

Figure 1 3rd order VCO-ADC with feedback and an additional passive and active integrator [14]

reduce the impact of VCO *Kv* non-linearity. The resolution of prior VCO based ADC's was primarily limited by distortion arising from the VCO *Kv* non-linearity. While negative feedback techniques did manage to suppress the distortion by more than an order of magnitude, non-linearity still prevented the ADC from achieving its full dynamic range.. To that end, the 4th order VCO based ADC architecture overcomes the SNDR limitation imposed by the VCO's non-linear *Kv* characteristics.

II. BACKGROUND

The previous section showed that nonlinearity poses a severe challenge toward achieving high converter SNDR for applications that embed the VCO based quantizer within a CT ADC structure. To overcome this obstacle, we are using phase rather than frequency as the key output variable of the quantizer. In practice, thermal noise, DAC mismatch, and other noise and error terms will add on top of the quantization noise floor and further degrade SNDR.

In order to achieve the performance target of around 80 dB SNDR, it is necessary to achieve higher order quantization noise shaping by extending the loop filter beyond first-order. The nonlinearity in the VCO's voltage-to-frequency (*Kv*) transfer characteristic seriously limits the resolution of VCO-based ADCs as shown in Fig. 2

The nonlinearity in the VCO's voltage-to-frequency (*Kv*) transfer characteristic seriously limits the resolution of VCO-based ADCs as its clear in Fig. 3. In all prior published work, the VCO output frequency is the desired output variable due to its proportional relationship with the input signal. Therefore, exercising the full DR of these converters requires the input signal to span the entire nonlinear *Kv* transfer characteristic, incurring harmonic distortion and limiting resolution to less than 8 Effective number of bits (ENOB) as in Fig. 2. While the circuit in Fig. 3 improves distortion performance by placing a high-gain filter before the VCO and employing negative feedback, *Kv* nonlinearity still limits resolution to less than 11 ENOB in a 20MHz bandwidth. The resolution of prior VCO based ADC's was primarily limited by distortion arising from the VCO *Kv* non-linearity. While negative feedback techniques helped to suppress the distortion by more than an order of magnitude, non-linearity still prevented the ADC from achieving its full dynamic range.

III. 4th order VCO-ADC

This VCO-ADC eliminates the impact of *Kv* nonlinearity by preserving the integral relationship of the VCO output phase to the input signal as shown in the Fig. 3. Certain non-idealities namely, non-linearity in the VCO's voltage-to-frequency translation have limited the resolution of the VCO based ADC to less than 8 effective number of bits (ENOB). Here, the VCO phase is sampled and quantized by registers, and compared to a reference phase via a phase detector. The output of the detector then drives a multibit DAC, which subtracts the previously quantized value from the input signal applied to the VCO. The resulting residue is then applied to the control node of the VCO, and integrated during the next cycle. The VCO voltage-to-phase quantizer improves the SNDR of the converter significantly.

4th-order CT ΔΣ Loop Filter

The simulation results from the previous section clearly showed the improved linearity can be obtained when using a VCO

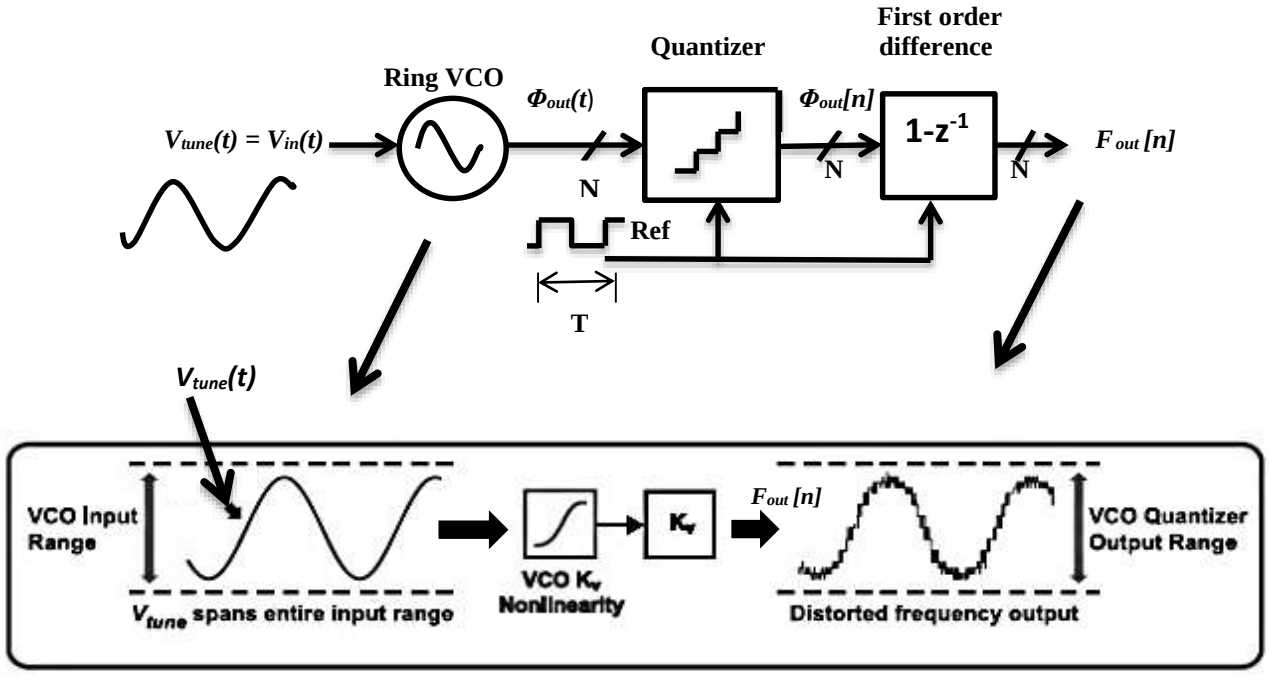

Figure 2 Prior voltage to frequency VCO based ADC architecture that suffered from distortion due to *Kv* non-linearity

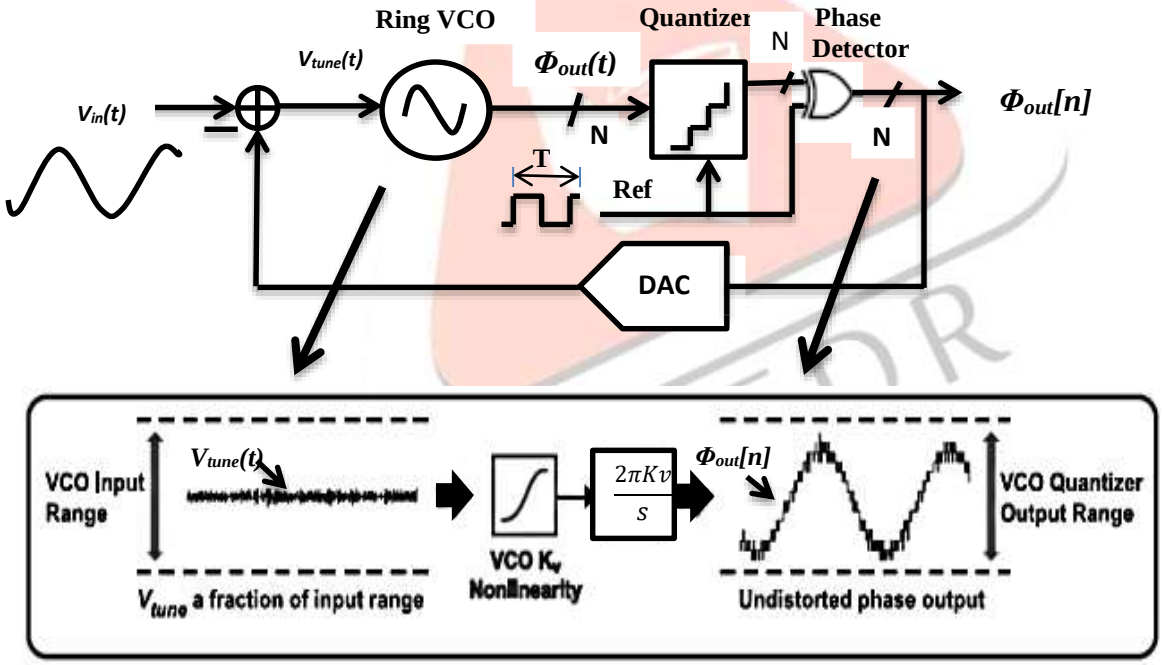

Figure 3 Proposed voltage to phase VCO based ADC that is immune to distortion caused by *Kv* non-linearity

voltage-to-phase quantizer. In reality, thermal noise, DAC mismatch, and other noise and error terms will add on top of the quantization noise floor, further degrading SNDR. To ensure high resolution, it is necessary to expand the loop filter and go beyond first-order noise shaping so that quantization noise can be further suppressed. A fourth-order loop filter was chosen is due to its high quantization noise shaping ability (SQNR > 95dB in 20 MHz BW). Traditionally, such a high order loop filter would be implemented using a cascade of integrators and feed-forward paths, with summation of all signals occurring at the input of the quantizer. This architecture also has the advantage of enabling easy compensation of feedback loop delay by using an additional feedback DAC. Current-steering non-return-to-zero(NRZ) and return-to-zero(RZ) DACs are implemented for their fast switching speeds. Unit-element mismatch errors in the main NRZ feedback DAC appear directly at the input of the converter and can seriously degrade SNDR. Errors from the minor-loop NRZ and RZ DACs are suppressed by the preceding loop filter gain, but can still limit performance when >11 ENOB resolution is desired. Therefore, DEM must be performed on all feedback DACs.

A block diagram of the 4th order loop filter with feed-forward and feedback stabilization is shown in Fig. 4.

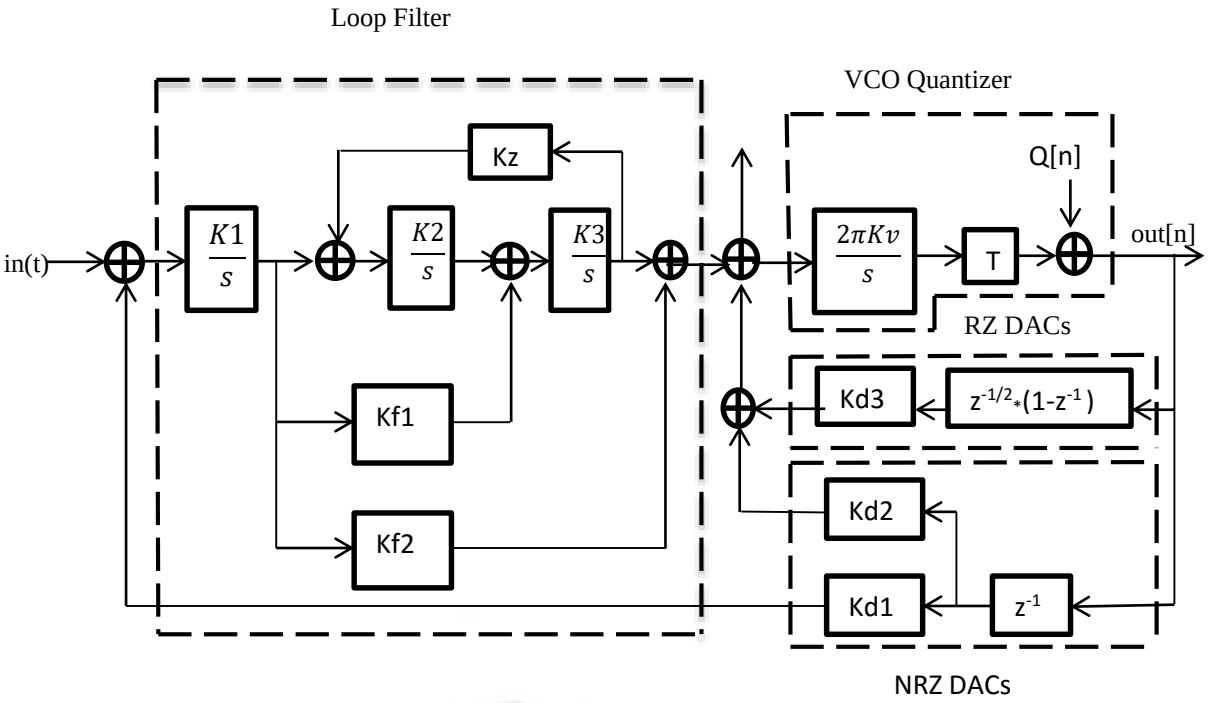

Figure 4 Loop filter block diagram with VCO Quantizer and feedback DACs indicated

Main and Minor-Loop NRZ Feedback DAC's

In principle, the main feedback DAC can be implemented by using either a NRZ or RZ structure. RZ structure is attractive than that of the NRZ structure due to its robustness to switching transient mismatch errors. RZ DAC was used within the minor loop feedback since any quantization noise folding arising from VCO K_v non- linearity will be suppressed by the open loop gain of the loop filter.

RZ feedback DAC

Mismatch in the main feedback DAC unit-elements appear directly at the input of DAC. Fortunately a data directed DEM algorithm have been developed to shape DAC unit-element mismatch errors, enabling high performance compared to prior scrambling algorithm that relied on random selection of DAC unit-elements.

NRZ DAC ISI

ISI occurs when unit-elements have mismatched output current transients during switching. A common solution to DAC ISI is to adopt a RZ DAC structure since all the DAC unit-elements will transit once every sample period. Unfortunately, RZ DAC is disadvantageous due to its heightened sensitivity to clock jitter. RZ DAC signal itself has effectively twice the bandwidth of its counter[art, requiring higher power DAC switch buffers, for these reasons NRZ DAC implementation was chosen.

IV. BEHAVIOR SIMULATIONS

Device Noise

In many state of the art data converter designs, device noise establishes the upper limit on achievable SNR. Consequently, the converter resolution ultimately becomes a question of how much power the designer is willing to sacrifice to reduce the device noise to a desired level. In CT ΔΣ ADC's, the device noise primarily originates from the main feedback DAC, the first integrator, and the input resistors.

Note: applying a full-scale input to a ΔΣ ADC can cause saturation in the integrators, resulting in quantization noise-folding.

VCO Unit Element Mismatch

Mismatches in the delay stages comprising the ring oscillator result in a net accumulated phase error at the end of each sampling period. Fortunately, these errors will be suppressed by the gain of the preceding loop filter, and should result in a small degradation of SNDR when referred to the input.

Main NRZ DAC Unit Element Mismatch

While mismatches in the second and third feedback DAC unit elements will be shaped by the high gain of the preceding loop filter, mismatches in the main feedback DAC unit elements appear directly at the input of the ADC.

Main NRZ DAC Inter-Symbol Interference (ISI)

In some sense, the term dynamic element matching (DEM) is a misnomer in that its purpose is to shape a static error, namely mismatches in the DC current values of the unit elements in a current-source DAC topology. However, such topologies do encounter a real dynamic error during switching transients, a phenomenon known as inter-symbol interference (ISI). ISI occurs when the unit elements have mismatched output current transients during switching.

Minor loop NRZ and RZ DAC unit-element mismatch and ISI

The minor loop DAC can be made smaller and the architecture can tolerate a higher degree of mismatch and ISI in their unit-elements. It is clear that, mismatches in minor-loop DAC are not as serious as those in the main NRZ feedback DAC, thanks to the loop filter gain.

Clock Jitter

The effect of clock jitter on the SNDR of CT ΔΣ ADC's has been well documented in the literature [18, 19, 20]. But, by specifically adopting a multibit NRZ DAC structure, the converter can be made less sensitive to clock jitter than the single-bit

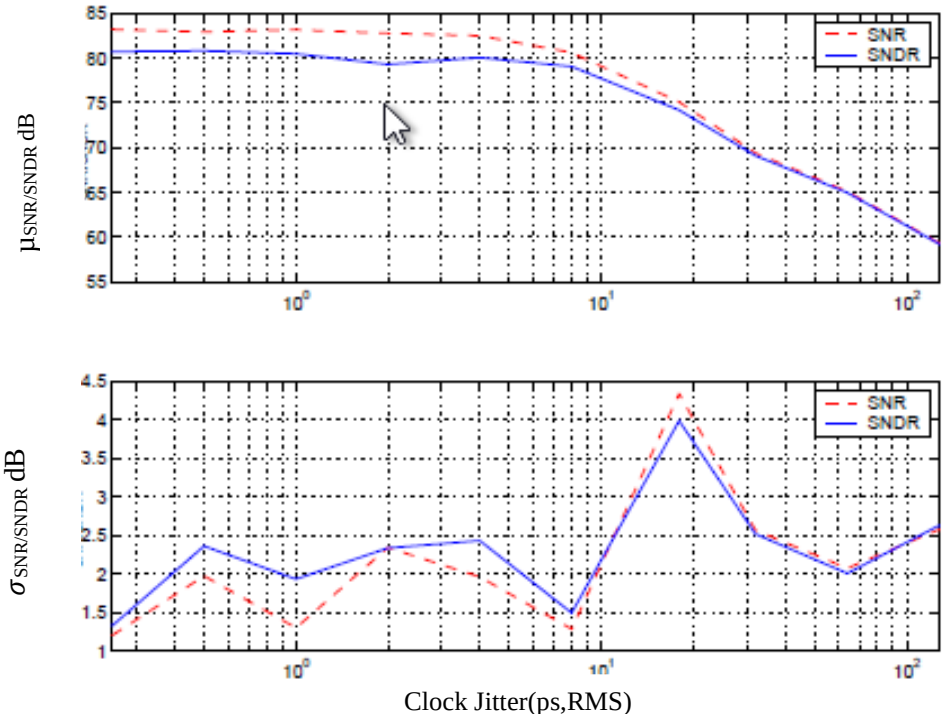

Figure 5 Average and standard deviation SNR and SNDR for variable amounts of clock jitter, as determined from Monte Carlo behavioral simulations [7]

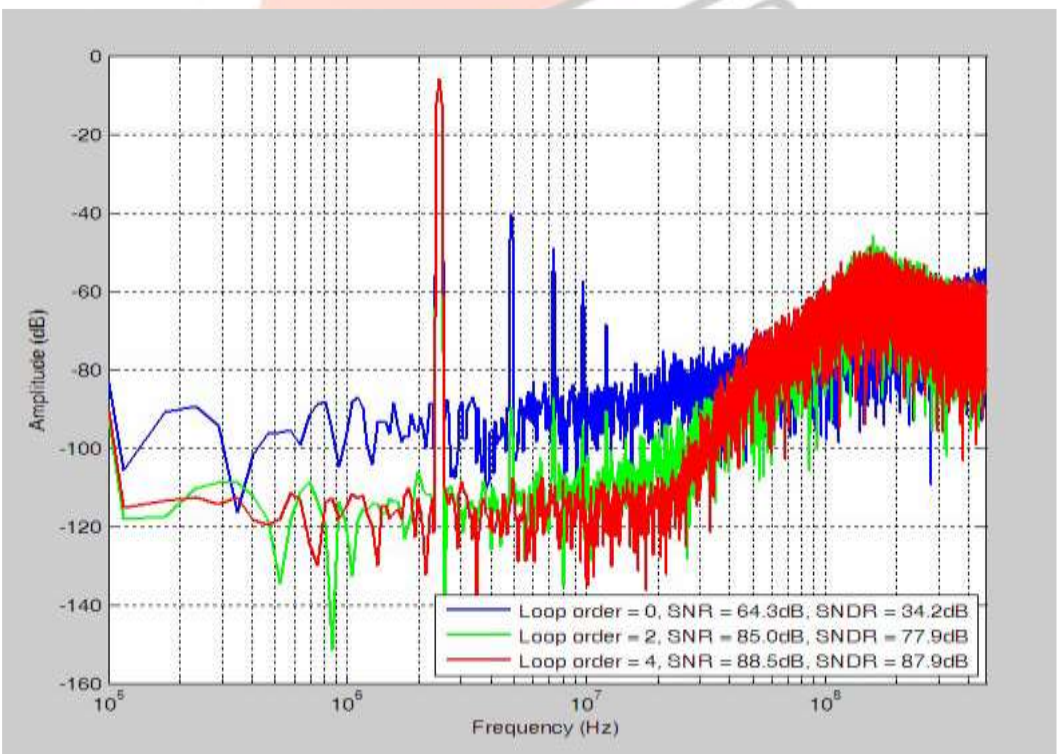

Figure 6 Graph of basic VCO-Based ADC simulations using Sue2 and CppSim View [17]

modulator. To verify the architecture's insensitivity to jitter, the behavioral model is modified to include variable amounts of clock jitter. Figure. 5 shows the average and standard deviation converter SNR and SNDR from Monte Carlo behavioral simulations, assuming a clock jitter as low as 250 fs,RMS up to more than 100 ps,RMS. As can be seen, the architecture can tolerate up to 4-5ps,RMS of jitter without significant degradation of converter resolution, thus validating the multibit NRZ DAC's robustness to clock jitter.

V. MEASURED RESULT

Table 1 Different VCO-ADC Measurements

VCO-ADC type	2nd order ADSM	2nd order ADC (ADSM+ VCO)	2nd order VCO-ADC with feedback loop		4th order VCO-ADC	
Technology	90 nm CMOS	90 nm CMOS	0.18 µm 1P5m digital CMOS		0.13 µm IBM CMOS	
Supply voltage	1 V	1 V	1.8 V		----	
Bandwidth	20MHz	20 MHz	1 MHz		20 MHz	
Sampling frequency	560MHz	640 MHz	800 MHz		900MHz	
SNR	68.4 dB	46.2 dB	60 dB		81.2 dB	
SNDR	67.3 dB	46 dB	39 dB		78.1 dB	
Power	3.1 mW	6.3 mW	Core part	34 mW	Analog Power	69 mW
			VCO	32 mW	Digital Power	18 mW
			VCO buffer	84 mW		
Active area	0.01 mm^2	0.026 mm^2	0.5 mm^2		0.45 mm^2	

Its clear from the table that the SNR and SNDR of 4th order VCO-ADC is better than the other order VCO-ADC which results in the better noise shaping of the output signal as now the signal is not effected by the *Kv* non-linearity. Figure. 6 shows the graph of basic VCO-Based ADC simulations using Sue2 and CppSim View [17].

VI. CONCLUSION

Previous chapters showed that the op-amps consumed the majority of the analog power (> 70%), which was necessary to achieve wide unity-gain bandwidths. Some improvements have been made to the op-amp topology that would enable potentially lower noise and wider unity-gain bandwidths. The 80 dB SNR and 78 dB SNDR of 4th order VCO-ADC work shows that VCO based ADC's can be leveraged in high performance applications, and that the non-linearity of the VCO *Kv* curve is not a limiting factor in achieving such performance. The proposed voltage-to-phase VCO-based ADC nearly eliminated the distortion that had riddled prior voltage-to-frequency VCO-based ADC's, enabling ideal SNR limited resolution.

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