Modified128 bit CSLA For Effective Area and Speed

Shaik Bademia Babu, Sada.Ravindar
,M.Tech,VLSI, Assistant professor
Nimra Inst Of Sci and tech   college, jupudi, Ibrahimpatnam,Vijayawada,AP state,India

_____

Abstract - **In the design of Integrated circuits, area occupancy plays a vital role because of increasing necessity of portable systems. Carry Select Adder (CSLA) is a fast adder used in data processing Processors for performing fast arithmetic functions. From the structure of the CSLA, the scope is to reduce the area of CSLA based on the efficient gate-level modification. In this paper 128 bits Regular Linear CSLA, Modified Linear CSLA, Regular Square-root CSLA (SQRT CSLA) and Modified SQRT CSLA architectures have been developed and compared. However, the Regular CSLA is still area-consuming due to the dual Ripple Carry Adder (RCA) structure. For reducing area, the CSLA can be implemented by using a single RCA and an add-one circuit instead of using dual RCA. Comparing the Regular Linear CSLA with Regular SQRT CSLA, the Regular SQRT CSLA has reduced area as well as comparing the Modified Linear CSLA with Modified SQRT CSLA BEC; the Modified SQRT CSLA BEC has reduced area. The results and analysis show that the Modified Linear CSLA and Modified SQRT CSLA BEC provide better outcomes than the Regular Linear CSLA and Regular SQRT CSLA respectively. This project was aimed for implementing high performance optimized FPGA architecture.Modelsim 10.0c is used for simulating the CSLA and synthesized using Xilinx PlanAhead13.4.Then the implementation is done in Virtex5 FPGA Kit.**

Key words - **Enhanced speed, Reduced Area, SQRT, BEC, Virtex5 FPGA.**

_____

I. INTRODUCTION

Highly -increasing requirement for mobile and several electronic devices want the use of VLSI circuits which are highly power efficient. The most primitive arithmetic operation in processors is addition and the adder is the most highly used arithmetic component of the processor. Carry Select Adder (CSA) is one of the fastest adders and the structure of the CSA shows that there is a possibility for increasing its efficiency by reducing the power dissipation and area in the CSA. This research paper presents power and delay analysis of various adders and proposed a 32-bit CSA that is implemented using variable size of the combination of adders, thus the proposed carry select Adder (CSA) which has minimum Delay, and less power consumption hence improving the efficiency and speed of the Carry Select Adder. In recent years, the increasing demand for high-speed and low power arithmetic units in floating point co-processors, image processing units and DSP chips has resulted in the development of high-speed adders, as addition is an obligatory and mandatory function in these units. A compact and a high-performance adder play an important role in most of the hardware circuits. Adders are used in microprocessor system based application for arithmetic addition and for computation in large electronics circuit. Less efficient and low power adders would lead to an increase in the total power dissipation in the circuit.

II. EXISTING SYSTEM

Ripple carry adder

Carry-ripple adder (CRA) consists of cascaded "N" single-bit full-adders. Output carry of previous full adder becomes the carry input for the next full adder. Carry propagation delay exists between any two full adders in sequence For an N-bit full-adder as shown in Fig. 1, the critical path is equal to N-bit carry propagation path in the cascaded full-adders. As the value of N increases, the corresponding delay of carry-ripple adder will increase in a linear way. CRA has the slowest speed amongst all adders because of the large carry propagation delay but occupies the least area
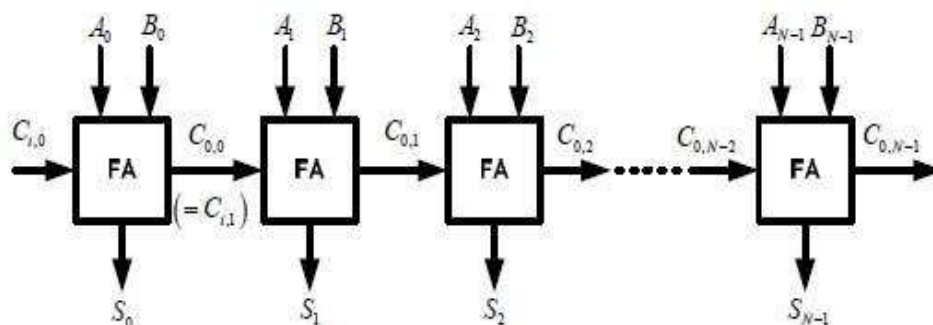

Fig1.   N- bit CRA using N set single bit full adders

Conventional Carry Select Adder

Each CRA pair in CSA can compute in parallel the value of sum before the previous stage carry comes. This reduces the critical path of an N bit adder. Delay in CSA is much lesser than CRA because the critical path in case of conventional adder is N-bit

_____

carry propagation path and done sum generating stage while in case of CSA, the critical path is (N/L)-bit carry propagation path and L stage multiplexer with one sum generating stage in the N- bit CSA, where L is number of stages in CSA. Since L is much less than N and multiplexer delay is less than the delay in full adder, hence the delay in the CSA is much less than that in the CRA but there exists duplication of hardware in every stage which leads to an increase in the amount of power consumption and cost.
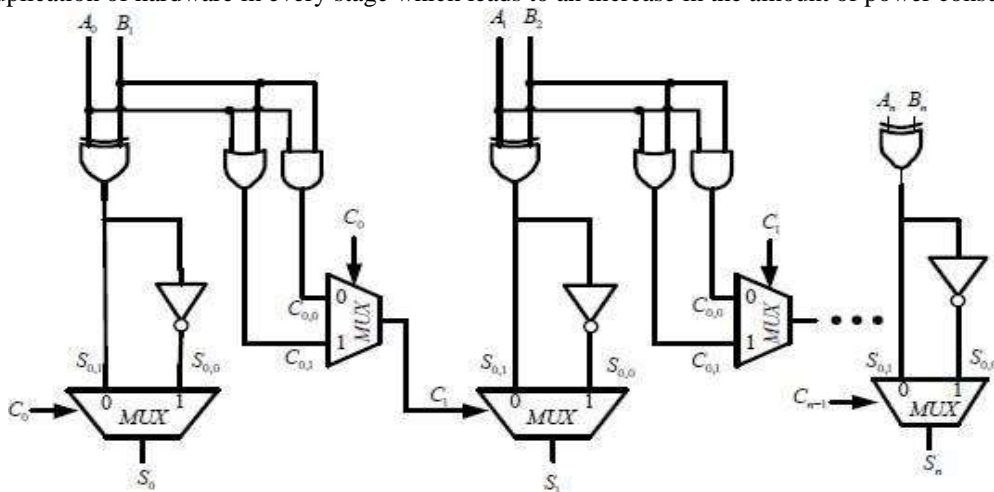

Fig2. Block diagram of conventional CSA

PROPOSED SYSTEM
Improved Carry Select Adder
The truth table shown in Fig. 3 of a single-bit full-adder indicates that output sum (S0) is Ex-OR of inputs A and B when carry initial is logic "0" while output S0 is Ex-NOR of inputs A and B when carry initial is logic "1" as illustrate as two red circles in Truth table. The improved CSA can be implemented by using this technique of sharing the common Boolean logic term in summation generation as shown in figure 3.1.7. Hence we need to use Ex-OR gate and INV gate to generate the output sum signal pair. Sum output either the Ex-OR or the Ex-NOR could be selected using the multiplexer with select line as previous carry signal
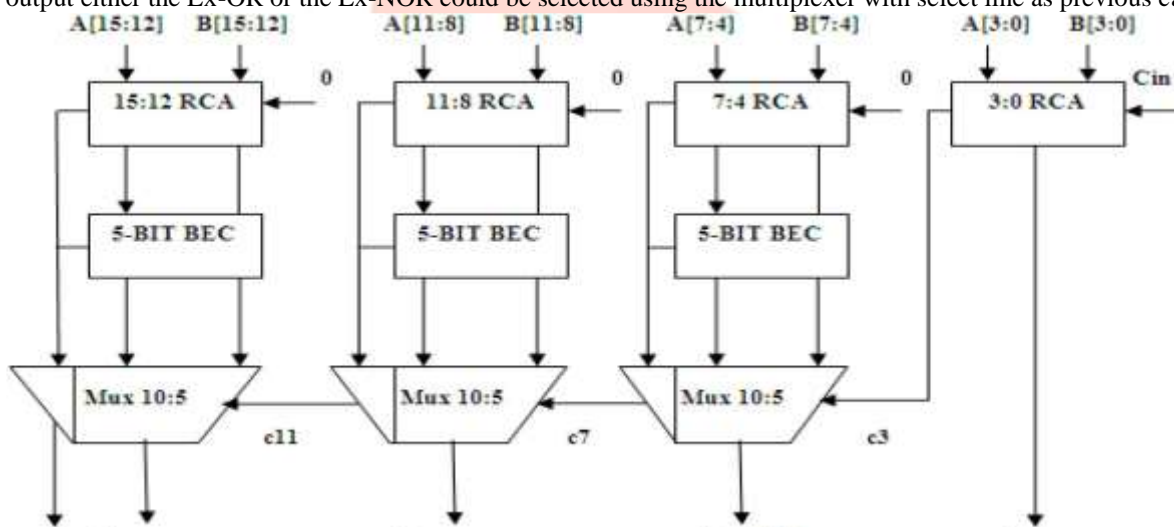

Fig3. Improved carry save adder with truth table for 1bit.

The truth table also reveals that output carry (C0) is AND of A, B inputs when initial carry is logic "0" while C0 is OR of A, B when initial carry is logic "1". Same previous carry as select line to second multiplexer is used to select the carry output of the first stage which would act as select line of the multiplexers in the second stage. As both sum generation and carry generation is carried out in parallel therefore there exist some competitiveness in speed also the power consumption reduces as duplication of the hardware doesn't exist in improved CSA as in case of the conventional.

Binary To Excess-I Converter (BEC)
As stated above the main idea of this work is to use BEC instead of the RCA with cin =1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-b BEC are shown in Fig 4.1.a.and Table 4.1.c, respectively. Fig4.1.a.illustrates how the basic function of the CSLA is obtained by using the 4-bit BEC together with the mux. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~ NOT, &AND, ^XOR)
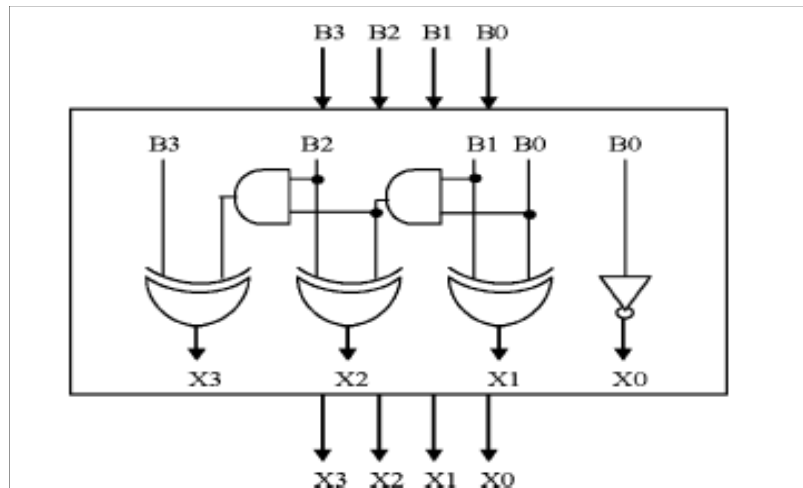
Fig4. Adder circuit

Adder blocks	Delay	Area
XOR	3	5
2:1 MUX	3	4
Half Adder	3	6
Full Adder	6	13

Table1. Delay and Area of the carry select adder

Methodology of Modified 16-Bit Linear CSLA And SQRT CSLA

The structure of the proposed 16-bit Linear and SQRTCSLA using BEC for RCA with carry in = 1 to optimize thearea is shown in Fig. 4.3. The 16-bit modified Linear CSLA has 4 groups of same size RCA and BEC. Each group contains one RCA, one BEC and MUX . . Inthe modified Linear CSLA, the group3 has one 4-bit RCA which has 3 FA and 1 HA for carry in = O. Instead of another 4-bit RCA with carry in = 1 a 5-bit BEC is used which adds one tothe output from 4-bit RCA. The selection input of 10:5 mux is c7. If the c7=0, the mux select RCA output otherwise it select BEC output. The output of group3 are Sum [11 :8] and carryout, cll. Then the area count of group3 is determined as follows:

Gate count = 89 (FA + HA + MUX + BEC)
FA =39 (3*13)
HA = 6 (1 * 6)
MUX = 20 (5 * 4)
NOT = 1,
AND = 3 (3 * 1)
XOR = 20 (4 * 5)
BEC (5-BIT) = NOT + AND + XOR = 24

GROUP	AREA ACCOUNT
Group 1	52
Group 2	89
Group 3	89
Group 4	89

Table2.No of logic gates

III. RESULT ANALYSIS

In this system we use the BEC to reduce the RCA circuits Here based on the carry input the MUX will be select corresponding input In this design we give the MUX inputs are RCA output and BEC output Compare to regular design the area of the design is less conventional CSA, and conventional CRA. Analysis shows that it results in 48 to 52 percent Are has reduced and the power dissipation and 40% less PDP when implementation is done using modified SQRT BEC. The no of LUTS used in the circuit implementation is 437 out of available 1920 and the utilization factor is 22%, no of fully used LUT – FF pairs are 74 which is less usable factor, the no of bonded IOBS used 386 out of 66 and the utilization factor is 584% so this implementation considering the RTL is occupied less area and size is also reduced. That increased the system speed and efficiency and also less power requirement in the 128 bit carry select adder. The below result is from the RTL schematic view of Xilinx implementation
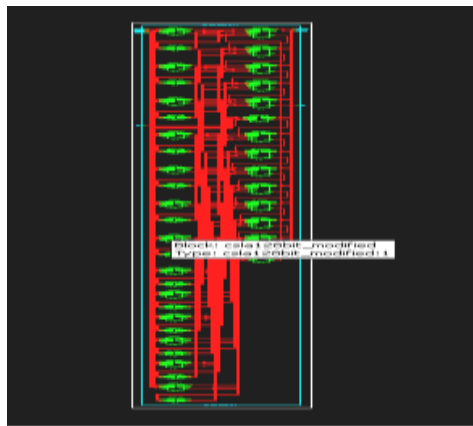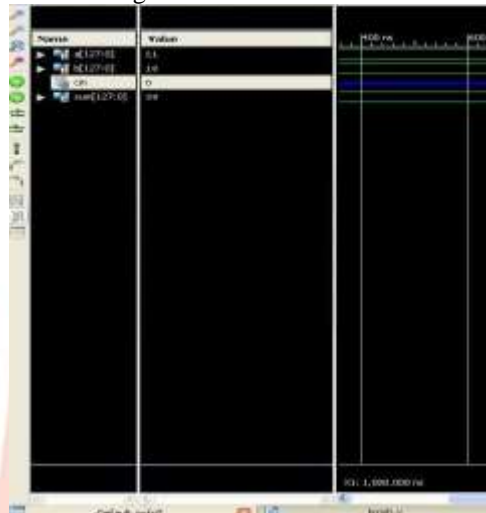
Fig 5.RTL schematic view

Fig6. Simulation result

IV. DESIGN SUMMARY

In this system we use the BEC to reduce the RCA circuits Here based on the carry input the MUX will be select corresponding input In this design we give the MUX inputs are RCA output and BEC output Compare to regular design the area of the design is less conventional CSA, and conventional CRA. Analysis shows that it results in 48 to 52 percent Are has reduced and the power dissipation and 40% less PDP when implementation is done using modified SQRT BEC. The no of LUTS used in the circuit implementation is 437 out of available 1920 and the utilization factor is 22%, no of fully used LUT – FF pairs are 74 which is less usable factor, the no of bonded IOBS used 386 out of 66 and the utilization factor is 584% so this implementation considering the RTL is occupied less area and size is also reduced. That increased the system speed and efficiency and also less power requirement in the 128 bit carry select adder. The below result is from the RTL schematic view of Xilinx implementation

Table 3. Design summary

Bit Size	Types	Area count of Linear CSLA	Area count of SQRT BEC CSLA
32-bit	Regular	871	868
	Modified	675	679
64-bit	Regular	1792	1736
	Modified	1387	1348
128- bit	Regular	3679	3472
	Modified	2811	2657

REFERENCES

[1] High enhancement Area Efficient Carry Select Adder(978-1-4673-4922-2113/$31.00 ©20 13 IEEE)

[2] Low Power and Area-Efficient Carry Select Adde K.Saranya

[3] -chyn Wey, Cheng Chen Ho, Yi-Sheng Lin ,and Chien- Chang Peng "An Area Efficient Carry Select Adder design by sharing the Boolean Logic term"vol-II,IMECS 2012,March 14- 16 2012,Hong Kong.

[4] O.Bedrij,"Carry Select Adder",IRE trans on Electronic Computers Vol EC-II,pp 340-346.1962.

[5] JM Rabaey,"Digital Integrated Circuits",IEEE trans on VLSI SYSTEMS 2003.

[4] Shen Fu Hsiao,Member,IEEE,Mingyu Tsai, and Chia ShengWen "Circuits and Systems-II";Express Briefs ,Vol 57,No1 January 2010.

[5] B. Ramkumar and Hrish M kittur, "Low-Power and Area Efficient Carry Select Adder" in IEEE Transaction on Very Large Scale Integration (VLSI) Systems, Vol.20, No.2, February 2012.

[6] Padma Devi, Ashima Girdhar, Balwinder Singh, "Improved Carry Select Adder with Reduced Area and Low Power

Consumption"in International Journal of Computer Applications, Vol.3, No.4, June 2010.

[7] B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," Eur. J. Sci. Res., vol. 42, no. 1, pp.53–58, 2010.

[8] Geetanjali Sharma, Uma Nirmal, Yogesh Mishra, "Comparative on Advances in Information Communication Technology and VLSI Design, Coimbatore, India, August 2010.

[9] Geetanjali Sharma, Uma Nirmal, Yogesh Mishra, "Synthesis of Hybrid PTL/CMOS Logic for Low Area/Power Applications" in proceeding of International Conference on System Dynamics and Control, India, August 2010.

[10] Shen-Fu Hsiao Ming-Yu Tsai, and Chia-Sheng Wen,"Low Area/Power Synthesis using Hybrid Pass Transistor/CMOS Logic Cells in Standard Cell-based Design Environment," IEEE Trans. Circuits and Systems vol. 57, NO.1, Jan 2010.

[11] G. R. Cho and T. Chen, "Synthesis of Single/Dual-Rail Mixed PTL/Static Logic for Low-Power Applications," IEEE Trans. Computer-Aided Design Integration Circuits Syst., vol.23, no

About the authors

SHAIK BADEMIA BABU1 pursuing M. Tech, in VLSISD at Nimra institute of science and technology, Jupudi,Vijayawada,Andhra Pradesh, India. He received B. Tech Degree in Electronics And Communication engineering from at Nimra institute of science and technology, Jupudi,Vijayawada,Andhra Pradesh, India. His areas of interest's lies in communication systems and processors.

SADA RAVINDAR2 is an Assistant Professor of Electronics and Communication Engineering at at Nimra institute of science and technology, Jupudi,Vijayawada,Andhra Pradesh, India. He received His M. Tech from gudlavalleru engineering college, JNTUK, and B.Tech from st.anna's Engineering college , JNTUK. His area of interests lies in Digital signal and Image processing.