A Review of Design of Efficient ALU's

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***Abstract* - Most of the recent scientific operations take DSP operations into consideration. Arithmetic and logical unit is the main part of a digital processor. The fastness of a processor is controlled mainly by the multiplication unit,as arithmetic and logic units are engaged for diverse areas ,places at which handling some of signals become necessary. Multipliers play extremely vital role in ALU design. Although some different algorithms of multiplication are in utilization, the implementation of multiplication units build on Vedic mathematics have not get much recognition. It includes the incomplete products headed by additive evaluation, in a one step. The design and implementation lessens the complication of the prototype of multiplier. After a extensive study it can be said that UrdhvaTriyambakam multiplication algorithm is the one of the best algorithm as incomplete products can be produced in the parallel manner. The mathematicsof vedas is put forth by 'Swami Bharati Krishna Tirtha'in 1965 as an incarnation list of 16 formulae and 13 sub formulae which contains a list of mental calculations. Also Vedic mathematics process show low handling time therefore the practice would be useful to initiate a leading process for speedy multiplication units and processing units. The Vedic mathematic based Urdhva-Tiryakbhyam multiplier is estimated 10 times quick in performance than the conventional multiplier architecture.**

***Keywords* - FPGA, ALU, DSP Unit**

I. INTRODUCTION

The respective deprecation of detention period and power expenditure is turned into one of the crucial problem regarding implementation of the top level completion of processing units. Arithmetic and Logical Unit is a fundamental part of every CPU design. It attain arithmetical, Logical and Unary operations on integers kept in accumulator unit, register array, operand register and values fed from outer memory. In recent decades, number of designs have been presented for effective power handling capability and decent performance. The implementation of an adder in parallel manner in ALU has become a vital role, as the propagation of respective (CP) is responsible for the delay in addition. With the help of vedic mathematics a number of operations can be performed in easy steps. The multiplier is the most delay causing unit, therefore the output of multiplier affects the whole ALU unit. Further, it normally covers the most of area. Therefore, as a summary it can be said that optimization of the area and delay of the multiplier unitin ALU is a vital design issue. Vedic Mathematics. The Urdhva Tiryakbhayam algorithm is considered as the powerful technique for improving the speed of the computations involved.

II. RELATED WORK

Brief detailed literature review is as follows-

In[1]In this paper ,the multiplication unit of alu is designed using a process of calculation based on set of 16 sutras ie(Vedic Mathematics). Based on this technique the structure of 2bit, 4bit and 8 bit multipliers based on vedic approach redisplayed and is encoded in a VHSIC Hardware Description language (VHDL) and synthesized with the aid of EDA tool, XilinxISE12.2i. Finally, an evaluation of differences is made across the results placed by Vedic design with traditional multipliers**.**

In[2]The prototype and purpose of the various tasks carried out by a reconfigurable ALU are described in [2]. A oneprecision presentation representing the location of decimal point by exponent of radix, addition and subtraction of 32 bit is taken. It can be helpful in parallel processing approach and computation intensive applications. The design is for 32 bit input sytem can be utilised in multimedia applications. As frequency decreases, the power consumption also decreases without taking IO standard into consideration .

In [3] The synchronous crucial algorithmis utilised, where both the transmitter and receiptant utilise a sole principle of encoding as well as decoding is AES. The declared structure is improved as compared to the Look-up table way , as arena filled by Look-up table technique is much farther along the extent of a Xilinx Spartan 3E series of FPGA. In status of timing approach, a contrast in time with LUT way is surplus, taking its major space habitation. When taking the status of logic gates, this technique occupies 46 XOR gates only.

In [4] Area Gated Diffusion Input Technique is a latest option for reduction in power dissipationand propagation hold up. There are three inputs in a GDI cell - G (NMOS and PMOS common gate input), P (PMOS, input to the source/drain) and N (NMOS, input to the source/drain).A major part of both NMOS and PMOS are joined to N and P respectively. The design utilise the idea of GDI (Gated diffusion input) approach in the implementation of ALU and its sub areas as Multiplexers and Full adders. Less dynamic power usage as power supply to ground connections is minimum in GDI design technique.

In [5]The Floating point integers are commonly written as((1)S)(F)(2E),where F shows a digit in fraction value, where E shows a digitin the exponent value. In widespread, mantissa value is assigned by addition of 1 as MSB. In case where the exponent value

is big enough that it cannot be handled by exponent field then an overflow flag becomes high . In the situation where the negative exponent is big enough to fit the exponent field, then an overflow flag is shown. IEEE-754 standard started a new method known as NaN (Not a Number) ,for the functionsthat are not valid that are condition when zero is divided with zero, subtraction of infinite number from infinite one.*Karatsuba* algorithm used progressively for the need in such applications is explained.An impressive multiplication algorithm, which helps in accurate usage of input output pins and with reduced delay should be utilised for proper design of floating point processors. In binary system,floating point integers are defined in two ways namely, single and double precision. These formats are characterized by exponent, mantissa and sign fields. On the basis of device usage and output evaluation, Vedic multiplier advanced over*Karatsuba* multiplier both for single and double precision formats. Even though Booth multiplier adapt minimum resources, it is also low in speed.

In [6]There is a new approach used for energy optimization that is low voltage complementary metal oxide semiconductor technique.LVCMOS12, LVCMOS15, LVCMOS18 and LVCMOS25 are various options of LVCMOS relying on their supply voltage of output driver.The output evaluation shows a energy optimization as using LVCMOS12 and LVCMOS15 instead of LVCMOS 25 is 68.34% and 52.51%. All the values are calculated in Verilog language withbehavioral simulation and ISim in Xilinx 13.4 ISE and all code can be synthesized on virtex-6 FPGA. Further it also states that in term of power expenditureLVCMOS is one of the best IO standard and Virtex-6 is the well power planned FPGA.

In [7]The Co-existence of CMOS and SET (Single Electron Transistor) is the latest trend in the era of advanced semiconductor industry. In the paper we are given with the robust execution of ALU (Arithmetic Logic Unit) with the help of hybrid SET-CMOS ,also utilising hybrid SET-CMOS based logic gates that are reversible in nature. The simulation of results of given both cases is made witha estimate of similarities and dissimilarities made between them by using variousapproaches**.** In this paper ALU design of 4 bit hybrid SET-CMOS based ALU and 4 bit hybrid SET-CMOS Reversible logic gate .It can be concluded that hybrid SET-CMOS based Reversible logic is better in operation in contrast to conventional CMOS design and realizes the target of low power expenditure.

In [8] The paper presents a well planned and operational designing the asynchronous ALU with reduction of delay for the execution of instructions on FPGA.With the help of 4 way handshaking protocol we can decrease the delay and get large pliability and execution of the arithmetical and logical unit.The design methodology utilized is asynchronous. The work proposes the ALU, that attempts to reduce the fundamental drawbacks of the synchronous design of ALU, viz. clock skew ,power expenditure and detention by utilising the asynchronous ALU but the major limitations is large LUT consumption.

In [9] When computation for large number of bits in ALU is required, there is a need of cascading the adder circuit. These Cascaded adders however lead to Carry Propagation Delay (CPD) thereby affecting the speed of operation. 8 Bit, 16 Bit, 32 Bit and 64 Bit ALU is proposed using modified SQRT CSLA and also implemented ALU using modified SQRT CSLA by CLA. For realizing higher bit ALU using regular/modified SQRT CSLA, cascade methodology can be used. The ALU design and implementation using modified SQRT CSLA shown for low power and area-efficient applications. By introducing CLA in ALU better performance is obtained in terms of speed.

In [10] the one to one correspondence is the actual key required for reversible circuits that should count input and output pins equal. In other words every state of input should be consumed for particular output that is output logic will be shared by only one input logics present. A number of AND gates as well as adder units have been used to design a conventional multiplier, which also produces a remarkable delay. A time worthy approach for the resultant by using reduced count of resources is by using vedic algorithm, thereby effective delay decrement while gradual enhancing the rate of execution of output. The proposed implementation overcome power as well as delay hardcore bring forth by Selective Reversal as well as rapid algorithm of Vedic Method.

In [11] to design the two bit multiplication unit i.e. multipliers are proposed to obtain the result of two n-bit binary integers and then execute it on a Nexys 3, Spartan 6 FPGA kit is the principal purpose. Binary multiplication units of 32x32 have been evaluated with traditional multipliers depending on their result obtained at the execution after the final design. A list of evaluation is made based on 32-Bit Vedic mathematics based multiplier unit and a Conventional Binary Multiplier. It has been seen that the number1I0s required for 32-bit Vedic mathematic based multiplier unit and other binary multipliers are 128 out of 232, therefore out of which the requirement becomes 55% for both of the multipliers.

III. CONCLUSION

An efficient operational unit could be designed with the help of simulation tool and the functional units with optimized count of slices, count of flip-flops and input LUTs. The maximum frequency can be obtained from the analysis of timing view. Power count of the system should be proportional to the respective frequency. Time delay can be optimized using Vedic mathematics technique in implementation of multipliers as the speed of ALU depends prominently on the speed of multiplier. Further in the future work the speed of ALU can be increased by using various fast and efficient multipliers available in the literature.

IV. REFERENCES

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