Efficient Design of Area Delay Power Carry Select Adder

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Abstract **- Adders are one of the most important components in the digital logic used in every Integrated Circuit. To speed up the binary operations in an IC, high performance adders should be used. The requirements of an adder consists of low power consumption, small chip area and extremely fast. Carry Select Adder (CSLA) and Carry Look Ahead Adder (CLA) belongs to the class of high performance adders. The conventional Ripple Carry Adder (RCA) based CSLA and Binary to Excess 1 (BEC) based CSLA involves higher delay. In this paper, we proposed a delay and power efficient CLA based CSLA to overcome the disadvantages with conventional CSLA's.**

Keywords **- Carry Select Adder, Carry Look Ahead Adder, Ripple Carry Adder etc.**

I. INTRODUCTION

In digital electronics, Adders plays a prominent role in every operation involved and used in multiple blocks of architecture. The adders are used in ALU's as well as to calculate address. Adders have wide applications in DSP architectures and other complex architectures. These complex architectures will take a certain amount of delay to perform the operations. In present day technology design of low power and delay efficient architectures are needed. To solve this problem, if we design the adder with lowpower and delay efficient then automatically the architectures consisting of adders will have high performance.

II. RELATED WORKS

The choice of selecting the adder will determine the whole system performance. There are so many adders like Ripple Carry Adder (RCA), Carry Select Adder (CSLA), and Carry Look Ahead Adder (CLA) etc. While designing high performance addition based architectures, we must choose fast adder architectures to optimize logic level. CSLA and CLA belong to the class of high performance adders. The Ripple Carry Adder is not chosen for high performance, even though it looks simple but slower and has high Carry Propagation Delay (CPD). Suppose if n bits are applied to RCA, it will have a delay of 2n units. The reason for not choosing BEC, even it involves less logic resources than conventional CSLA, is it has marginally higher delay. In this paper, we are using a CSLA proposed in [1] which is different from conventional CSLA. The conventional CSLA have two RCA's and a Sum and Carry selection unit. The proposed CSLA [1] consists of half sum generation unit, CG0, CG1, Carry Select unit, final sum generation unit.

III. EXISTING SYSTEM

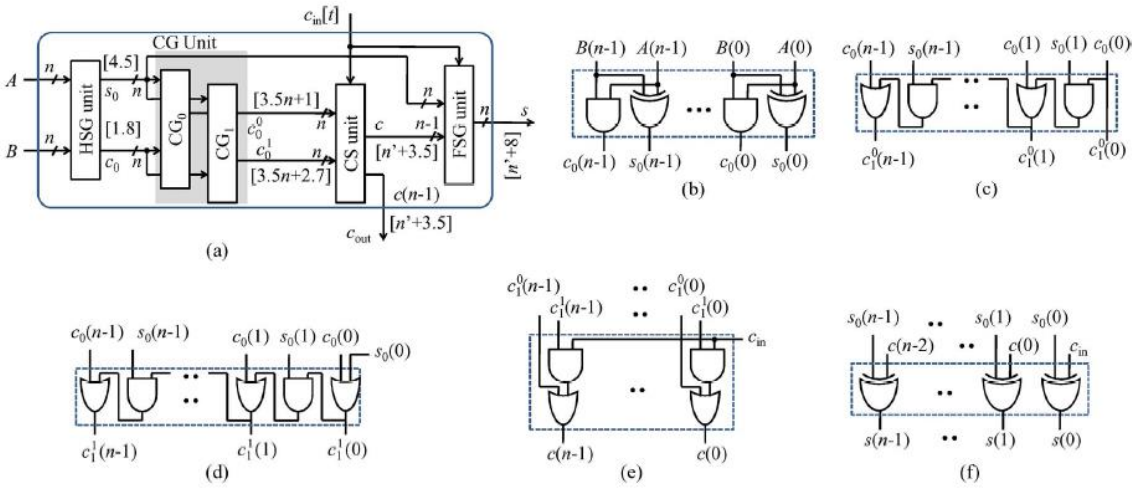

Fig.1.

(a) Proposed CS adder design, where n is the input operand bit-width, and [∗] represents delay (in the unit of inverter delay), n = max(t, 3.5n + 2.7).
(b) Gate-level design of the HSG.
(c) Gate-level optimized design of (CG0) for input-carry = 0.

(d) Gate-level optimized design of (CG1) for input-carry = 1.
(e) Gate-level design of the CS unit. (f) Gate-level design of the final-sum generation (FSG) unit.

The above figure 1 shows the proposed CSLA and its gate level design of different units. It operates on n bit input data and generate Sum and Carry out. CG0 and CG1 computes output by receiving outputs sum and carry from the HSG unit. The CS unit acts as a 2x1 mux selecting the outputs of CG0 and CG1 depending on input carry Cin. If Cin is 0, output of CG0 is selected and for Cin 1 CG1 output is selected. The FSG unit generates the final sum and carry out.

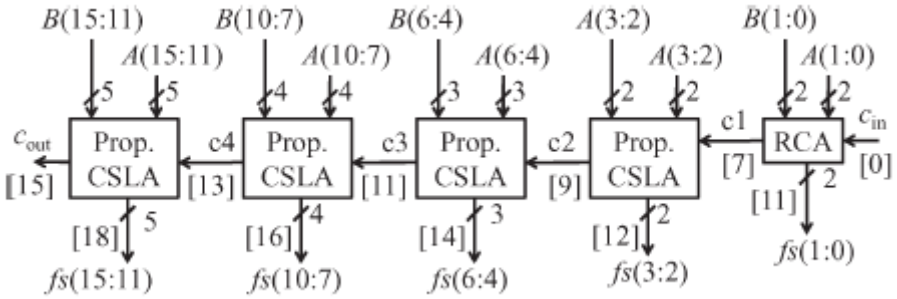

Fig.2 Existing 16 bit SQRT CSLA

IV. PROPOSED TECHNIQUE

As in the existing SQRT CSLA, RCA is used which in turn increases the delay, reducing the speed of operations performed by the adder. In this paper, we are proposing a SQRT CSLA by replacing RCA with Kogge – Stone Adder.
Kogge – Stone Adder is one of the forms of CLA. In industrial based applications, the Kogge – Stone adder is well known design of high performance adder and is known as possible fastest adder design.

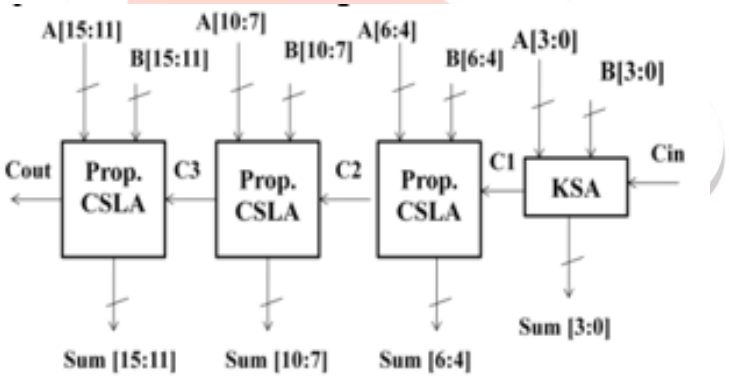

Fig.3 Proposed 16 bit SQRT CSLA

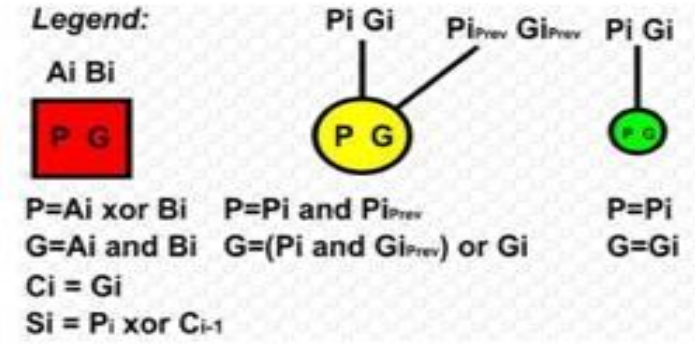

Fig.4 (a)

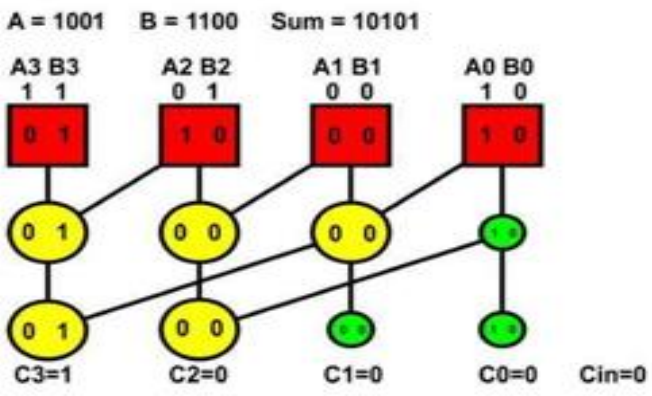

Fig. 4 (b) 4 bit Kogge Stone Adder

V. RESULTS

The proposed architecture is simulated and synthesized in Cadence NC launch simulator and Cadence RTL Compiler respectively, using 90 nm technology. The results of gate level simulation and architecture after synthesis are shown in below Fig. 5 and 6 respectively.

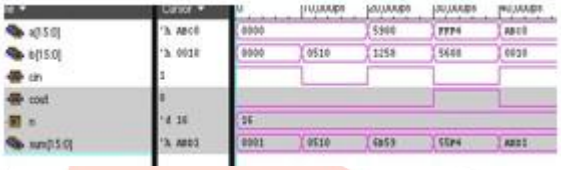

Fig. 5 Gate Level Simulation

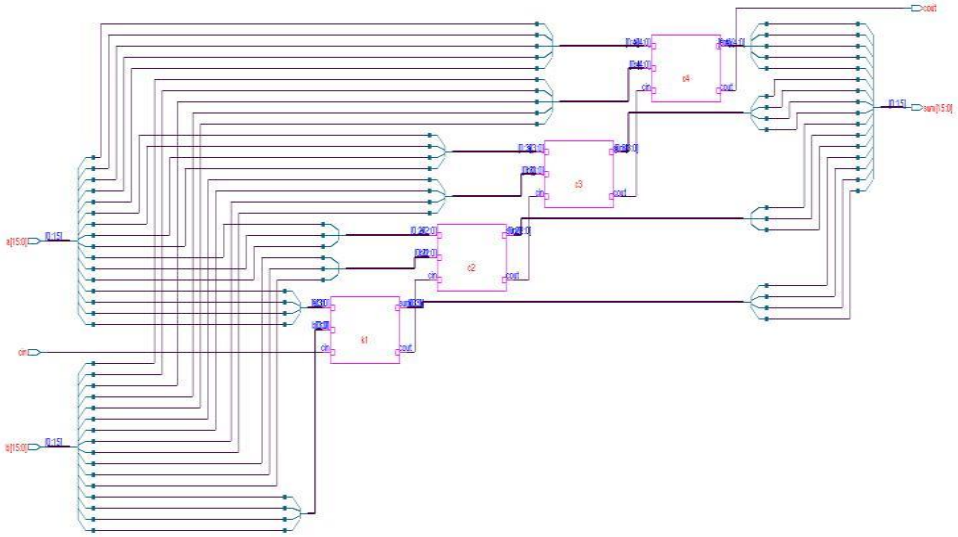

Fig. 6 Synthesis Architecture

VI. POWER, AREA ANALYSIS

The existing SQRT CSLA is implemented in Synopsys Armenia Educational Department (SAED) 90 nm CMOS library whereas the proposed SQRT CSLA is implemented in TSMC 90 nm library.

TABEL I COMPARISION OF SYNTHESIS RESULTS

Design	Width (n)	Delay (ns)	Area (μm^2)	Power (μw)
Existing SQRT CSLA	16	5.55	1813.45	19.665
	32	6.59	3735.36	38.188
Proposed SQRT CSLA	16	2.4	355	12|132
	32	3.0	818	30.531

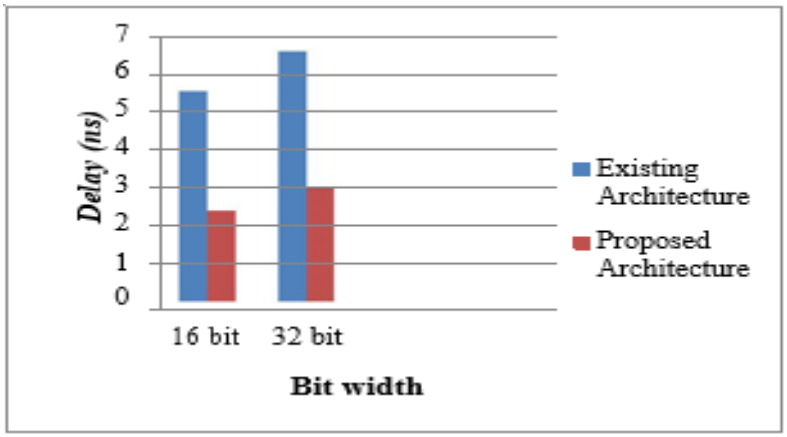

Fig. 7 Comparison of Delay

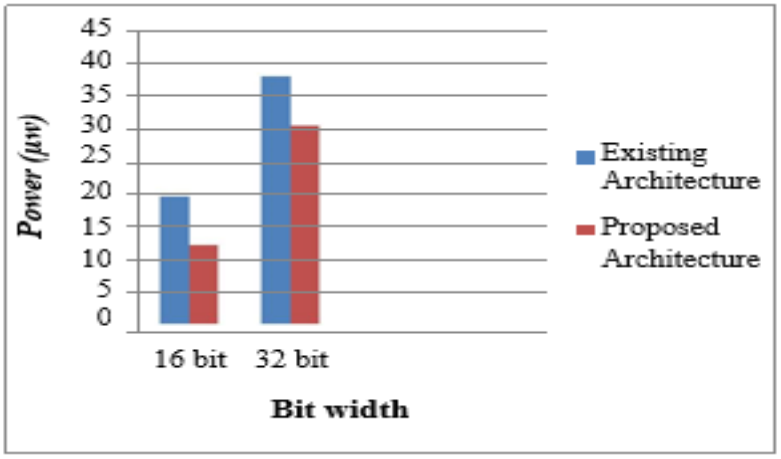

Fig. 8 Comparison of power

VII. CONCLUSION

In this paper, we presented the effects of RCA's and BEC based CSLA. We proposed a new architecture for CSLA on Kogge – Stone based approach. This KS adder makes the CSLA to overcome the disadvantages of previous adders and to achieve high performance and increases the speed of operations performed.

VIII. REFERENCES

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