Online Testable Reversible Circuits using reversible gate

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***Abstract* - Reversible logic is very promising due to its low power consumption. As the advancement of nanometer technology transient fault occur during the operation of circuit. Traditional technique such as Triple modular redundancy (TMR) consumes large area and power. So overall power dissipation of the chip increases. Reversible logic gaining interest due to low power consumption. This paper proposes the Automatic conversion of any reversible circuit to online testable circuit that can detect online any single bit error. In this paper conversion of decoder circuit and multiplexer is proposed. The proposed structure has been designed and simulated on XILINX 12.2 tool in Verilog language.**

***Index Terms* - reversible logic and gates, garbage, multiplexer, online testing and digital circuits.**

I. INTRODUCTION

Reversible logic [1] is a very prospective approach of logic synthesis for power reduction in future computing technologies. Reversible circuits are constructed using reversible gates. The recent computers erase a bit of information every time they perform a logical operation. Such logical operations are generally known as "irreversible logic". It imposes many design constraints. Zero energy dissipation would be possible only if the network consists of reversible gates. **L**ANDAUER [2] states that irreversible logic operations dissipates $kT\ln 2$ J of heat energy for every bit of information loss, where k is Boltzmann's constant and T is the absolute temperature at which the operation is done. Zhirnov *et al*. [3] predict that this heat dissipation would become impossible to remove by 2020 if Moore's Law continues to be in effect by doubling the circuit density in every 18 months. Bennett [4] shows that from thermodynamic point of view, $kT\ln 2$ heat dissipation would not occur if a computation is done in reversible manner. This theoretical thermodynamic limit can be achieved only if the circuit is both logically and physically reversible. Thus, reversible logic may be a favorable logic by dissipating less heat than the thermodynamic limit of kTln2 for the emerging computing technologies. Thus designing practically reversible circuit has become very important. On the other hand semiconductor device density on chip continues to increase to follow Moore's law and due to this million of transistor on very small die area. Operating voltage and dimension of the device decreases with the increase of device density. With the nanometer technology the device operates by storing very less charge. So these devices highly susceptible to striking of highly charged particle in the external environment in which they are operating. This paper presents the technique for construction of reversible circuit and online error detection. Paper consists of different section.Every reversible circuit can be converted into online testable circuit by the proposed technique discussed in the paper. Section II represents automatic conversion of reversible decoder circuit to online testable circuit. Section III represents Online testable multiplexer and section IV represent simulation result for above reversible circuits. Section V concludes the paper.

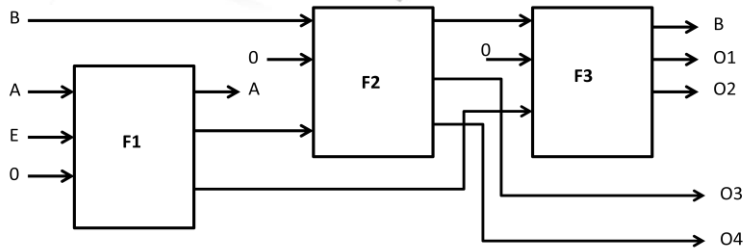


Fig 1. Two-to-four reversible decoder using Fredkin gate

II. AUTOMATIC CONVERSION OF REVERSIBLE DECODER CIRCUIT TO ONLINE TESTABLE CIRCUIT

Any reversible circuit can be automatically converted into online testable circuit describe in [5] that can detect any single bit error in the circuit when the circuit is in operation. If there is any error in the circuit online error can be detected. In this paper reversible decoder is converted. The following steps describe automatic conversion of reversible decoder as shown in fig.1 to online testable decoder.

1) Firstly each 3×3 fredkin gate in decoder circuit replaced by 4×4 DRG DRa(F) shown in Fig 2.
2) Construct TRC by connecting each DRa (F) to deduced identity gate DRG(X). DRG(X) is shown in Fig 3.TRC shown in fig 4.Set the Parity input bit Pia=Pib.
3) Online testable version of reversible decoder in Fig 1 shown in Fig 5 where every fredkin gate is replaced by TRC. F1, F2,

F3 replaced by TRC1, TRC2, TRC3 respectively. Parity input bits of TRC1, TRC2, TRC3 set to equal i.e. Pia1=Pib1, Pia2=Pib2, Pia3=Pib3.

4) At last parity output bits of the TRCs are connected to TC. If anyone output of the reversible gate is faulty then output T of the TC is set to 1.

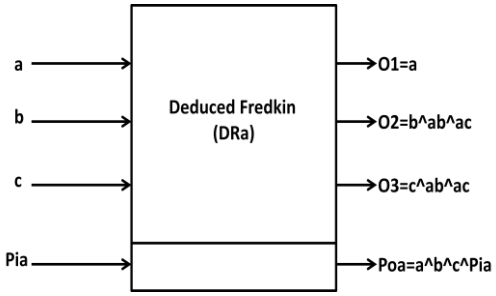


Fig 2.Deduced Fredkin gate DRa

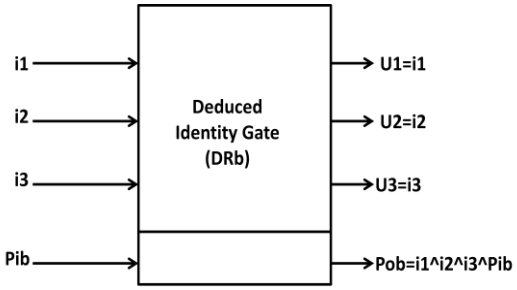


Fig 3.Deduced identity gate DRb

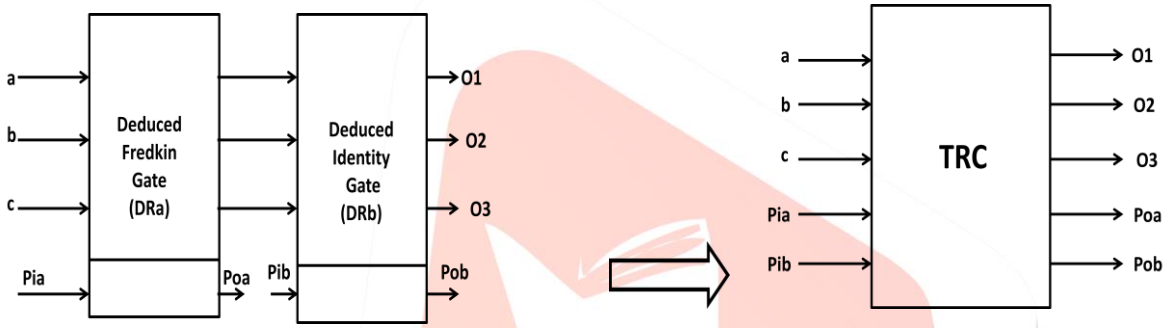
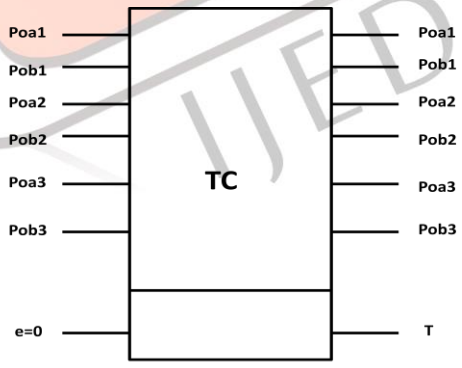


Fig 4. Cascading DRa and DRb to form TRC



Where T=[((POa1 ^ Pob1) ^(Poa2 ^ Pob2) ^ (Poa3 ^ Pob3)) ^ e]

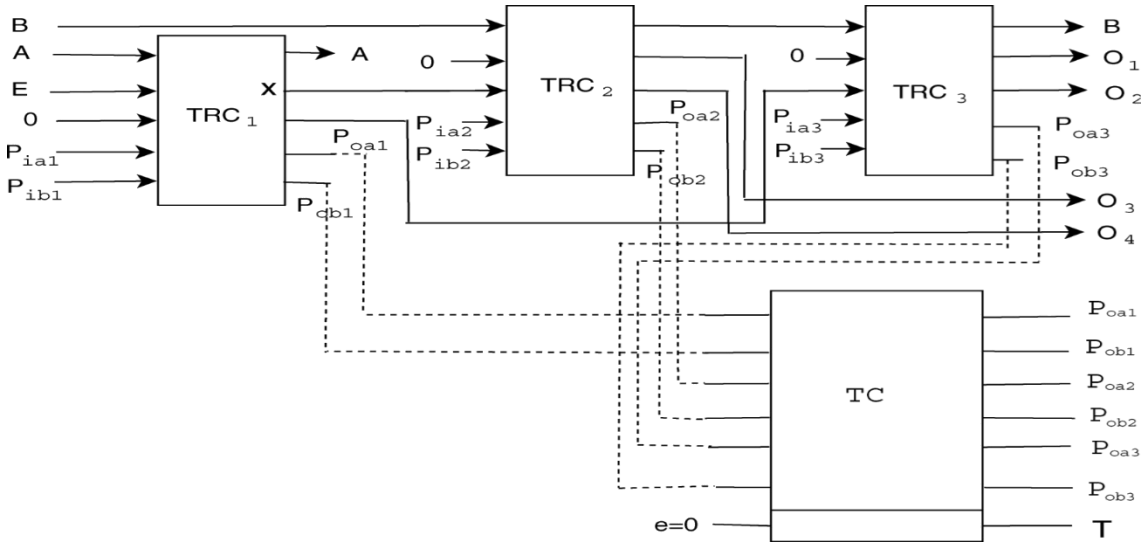


Fig 5. Online Testable reversible decoder circuit

III. ONLINE TESTABLE REVERSIBLE 4:1 MULTIPLEXER

By the use of proposed technique online testable multiplexer is designed. Algorithm is similar to as for reversible online decoder.

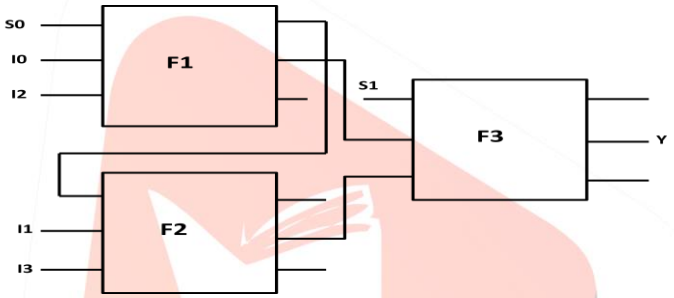


Fig 6. Reversible 4:1 multiplexer using Fredkin gate

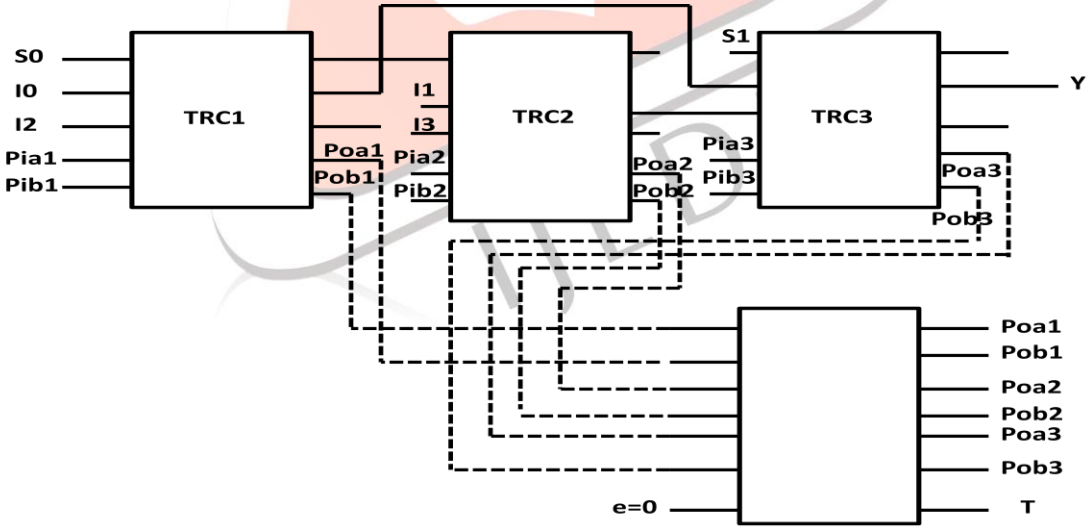
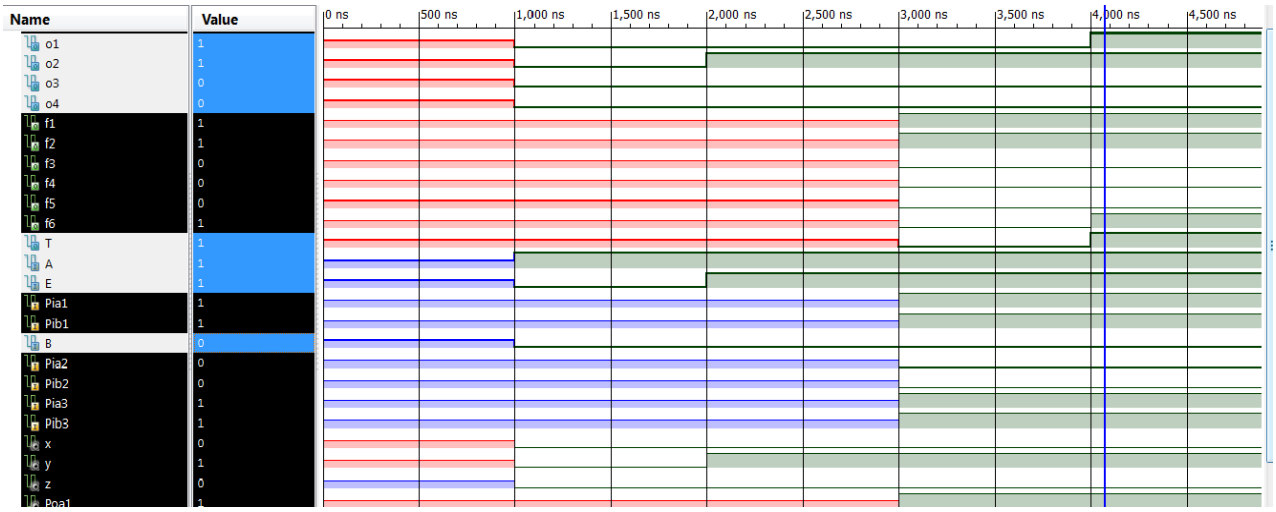
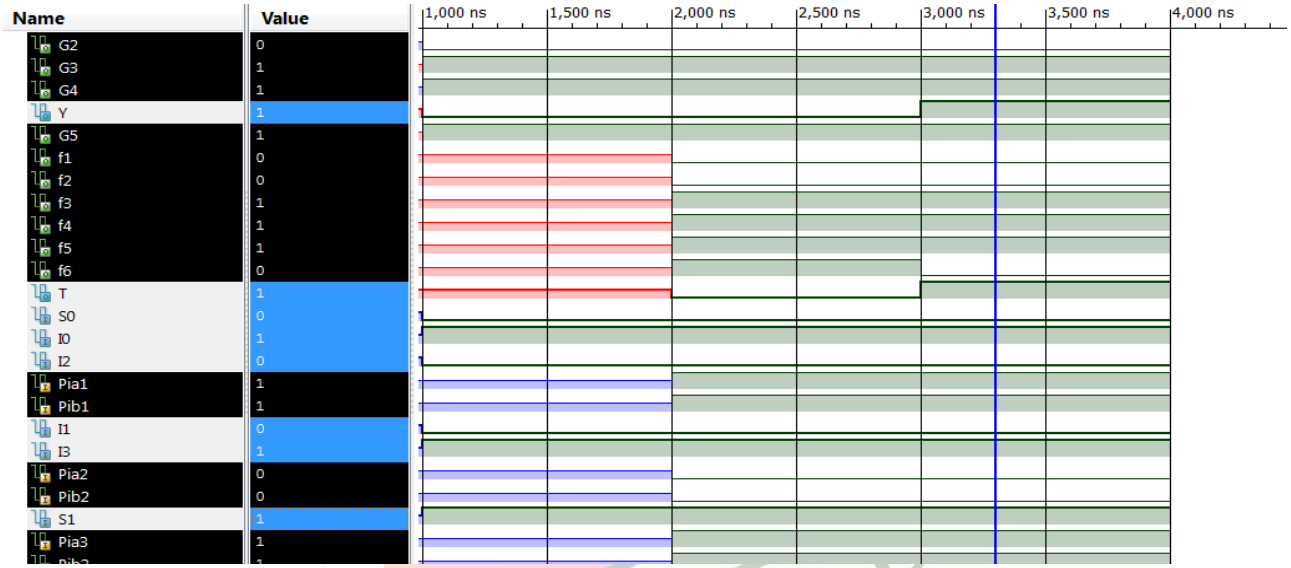


Fig 7. Online Testable reversible multiplexer circuit

IV. SIMULATION RESULT



Simulation result for online testable reversible decoder circuit



Simulation result for online testable reversible 4:1 mux circuit

V. CONCLUSION

This paper proposes reversible decoder and multiplexer and also proposes online testable version of these two circuit. The resultant testable circuit can detect online any single bit error in the logic blocks. These circuits are constructed using Xilinx 12.2 and simulated on Isim simulator. These circuits give less delay and less garbage value when compared to R1 based reversible circuit [6].Using this technique any reversible circuit can be converted to its online testable version .

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