Implementation of Area Efficient Encoder for 4-Bit Flash ADC

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***Abstract* - Analog–to-digital converter is an important device has a huge application in today's digitized world. Flash converter is high speed converter among all other ADCs. This paper concerns the design of Flash type of Analog to Digital Converter (ADC) which is more likely to be used for high quality audio and video signals. Different architectures of encoder are designed to build 4 bit Flash ADC The performance of proposed architecture is compared with other available architectures like multiplexer based direct conversion method, Wallace tree encoder, intermediate gray code based encoder using basic gates and using 2:1 multiplexers. From the study it is obtained that the proposed architecture consumes lesser area. The proposed architecture uses minimum number of multiplexers for the conversion. Design of these circuit use gpdk 180nm technology in cadence tool and simulated using SPECTRE.**

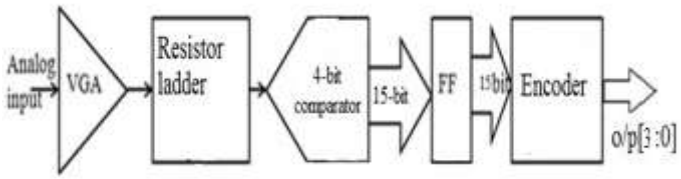
***Index Terms* – Flash ADC, Encoder.**

I. INTRODUCTION

With the merit of the digital circuit that gives strong motivation to make the digital world, the main aspect in nature is that real world signals are analog signals. This naturally occurring signal is made to digital for accuracy and better quality. In this modern era of electronics portable devices and high end instruments are becoming more and more sophisticated and perform a variety of tasks with high precision. The trend toward increased integration of analog and digital signals need data converters such as ADC, DAC is embedded in large digital IC's. There are various architectures in ADC and selected depending on the application. One such relatively easy architecture which is used for converting continuous time varying signal to digital signal is Flash ADC. Flash ADCs are mainly used in high speed applications and are known for its high power consumption. In Flash ADC itself there are various blocks such as resistor ladder, Comparator array, Thermometer code to Binary code encoder etc. Even though the comparator array and resistor ladder consumes the major part of ADC power, the encoder part also plays some significant role of ADC. The applications of flash ADC include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives.

II. FLASH ADC

For high speed applications, flash ADC is often used. Flash ADC is very fast and used for low resolution application due to its parallel architecture. It is best and less complex up to 8 bits. But when the number of bits increased complexity increases since the number of comparator needed is large. The main significance of flash ADC is that they are used within pipeline and sigma delta converters. The flash ADC consists of three main components resistor string, comparator bank, encoder logic. For N bit ADC, 2^N resistors and 2^N-1 comparators and 2^N-1 to N bit encoder is needed. The block diagram for typical flash ADC architecture is shown below.



The on-chip micro Computer first calibrates the ADC upon ADC start-up, and then continuously compensates the non-linearity in VGA. The ADC consists of a frontend Variable Gain Amplifier (G) which provides fine control of gain and maintains the analog input signal in full-scale voltage range of ADC. The comparator array is fed by a resister ladder network with 400m V of full-scale voltage.

The output of comparator array is 15 bit thermometer code. To prevent Metastability-related error propagation, the thermometer code goes through a sequence of flip-flops before arriving at the encoder inputs. Together with the comparator and the D Flip-Flop guarantees Metastability error rate betterment. A multiplexer logic then converts the Metastability-hardened thermometer code into binary. Finally, the output is retimed to a single clock phase.

Variable Gain Amplifier (VGA)

The variable gain amplifier (VGA) is designed to keep the input amplitude of the analog-to-digital converter (ADC) in range. The designer keeps the linearity of the variable gain amplifier (VGA) high. The Variable gain amplifier (VGA) should also have low noise figure, so that the performance of the analog-to-digital converter (ADC) should not be degraded. Variable gain amplifier (VGA) conditions the signal received from the channel to utilize full dynamic range of the analog-to-digital converter (ADC).

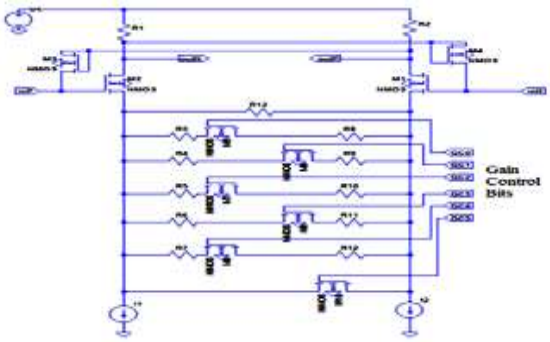


Figure. Variable gain amplifier

The variable gain amplifier (VGA) is utilized in many applications for decades, which includes radar, ultrasound and wireless communication. The purpose of the variable gain amplifier (VGA) is to improve the dynamic performance. Broadly speaking, the variable gain amplifier (VGA) is used in two different situations. The first is to match the input signal level to full scale input level of a device like an analog-to-digital converter (ADC) or a FM-discriminator. The second in which the fixed input voltage is scaled to compensate variable losses like transmission line voltage level adjustment. The variable gain amplifier (VGA) is a signal conditioning circuit with adjustable gain. Depending upon the nature of the gain control signal, the variable gain amplifier (VGA) is divided into two categories. Analog variable gain amplifier (AVGA) and Digital variable gain amplifier (DVGA).

Dynamic Comparator

The comparator array consists of 15 active comparators and a resistor ladder. To achieve a power-efficient design, the dynamic comparators in this ADC operate without any pre-amplifiers. To save power in the clock tree, each comparator uses a local clock buffer that can be disabled during individual comparator power down.Figure4.3 shows the design of the comparator, which is based on a dynamic-sense amplifier latch incorporating several modifications. The comparator compares the sampled input signal with the reference generated by the resistor ladder. This operation (i.e. comparing) is performed by pair M1–M2. This input device configuration accommodates the large signal range at the edges of the ladder. The output of a comparator is HIGH if the input voltage is larger than the reference voltage at the input of the comparator, otherwise the output is inverted clock since the comparator is working in dual input and single output mode the inverted clock region will be cancelled and considered as LOW.

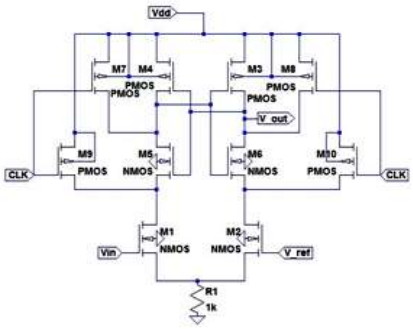


Figure: Dynamic comparator

Metastability Hardening by D Flip-Flop

A metastable event is defined as the time period when the output of a logic device is neither at logic high nor at logic low but rather in an indeterminate level. Metastability may occur when using a FIFO to synchronize two digital signals operating at different frequencies. This type of application is a familiar one to many design engineers. Triggering a metastable event is common in single-stage (single flip-flop) synchronized FIFOs that are used to synchronize different clock signals. With this method, the asynchronous input might change states too close to the clock transition, violating the flip-flop's setup and hold times. This causes an increase in resolve time (tr) which then results in an overall increase in propagation delay (t_{pd}). Once a metastable event is triggered, the probability of the output recovering to a high or low level increases exponentially with the increased resolve time.

Completely preventing Metastability is not possible, to be able to limit the possibility metastable behavior to a significant degree. Some of the ways to do this include using only one clock, using faster flip-flops, decreases the asynchronous input frequency, and use synchronization hardware. When more than one clock is used, the time window in which that the input is vulnerable to Metastability occurs more often. Using faster flip-flops decreases the setup and hold times of the flip-flop, which in turn decreases the time window that the flip-flop is vulnerable to Metastability. When the input frequency is decreased, the chances of the input changing during the setup and hold time also decreases.

ENCODER Block

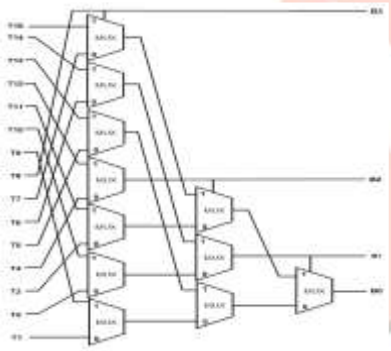
The thermometer code requires very huge memory since it takes more number of bits (2^N -1) to represent digital equivalent of a sample. It will become very complex to process this code in further levels. Hence it is very crucial to convert thermometer code into some other code that represents the equivalent data with optimized number of bits (N) like binary code. There are two types of encoders for conversion, known as

1. Direct conversion of thermo-meter-code to binary code
2. Indirect conversion of thermo-meter-code to binary code

In first method, by the help of the truth table we made the equations of direct conversion of thermo-meter code to binary code. The advantage of this method is, the parameters like power dissipation, current dissipation, propagation delay etc. will be minimum. In second method thermometer code will be converted into some intermediate code and then into binary code. Due to this extra intermediate stage the parameters like power dissipation, current dissipation, propagation delay etc. will be increased. Most common and widely used one is direct conversion of thermometer to binary code using 2:1 multiplexers. In this method the thermometer code is converted to binary using only 2:1 multiplexers. This circuit is known for its high speed and low power consumption. The number of multiplexers required in this circuit is more.

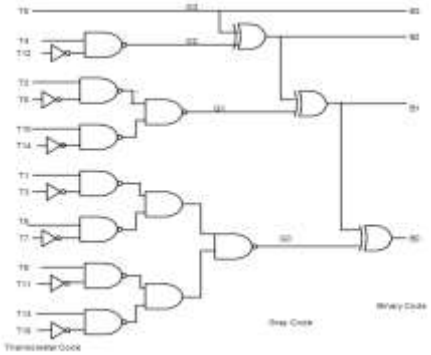
Multiplexer based direct conversion architecture

In this architecture the thermometer code is directly converted to the binary code using 2:1 multiplexers based on the truth table. This architecture is one of the most common architecture used in ADC design because of its low power consumption and high speed. For a 4 bit encoder it requires 11 2:1 multiplexers.



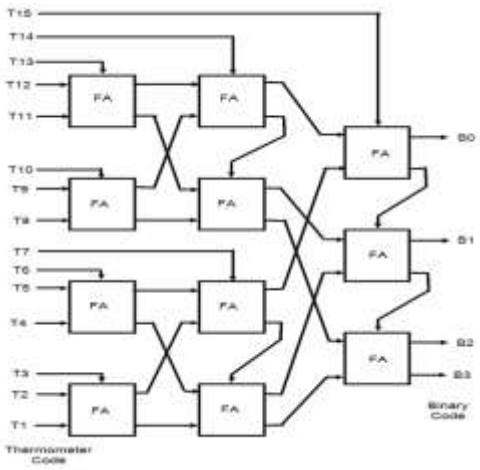
Intermediate gray code based Encoder using basic gates

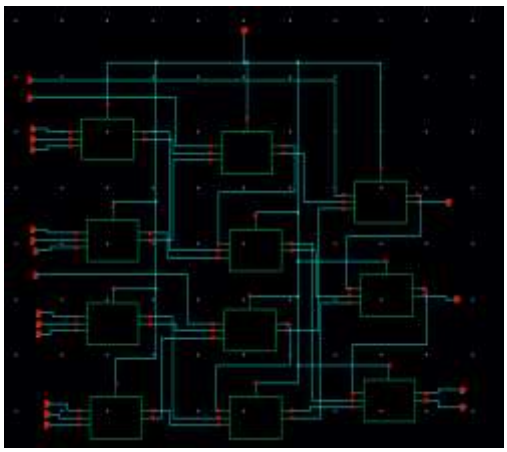
This architecture the thermometer code is directly converted to its corresponding gray code and then the gray code is converted to binary. This technique is very highly power efficient in nature. Other than power efficiency, converting the thermometer code to gray code will help in reducing the bubble errors. The conversion of gray code to binary code is done using the basic logic gates (AND, OR and INVERTER).



Wallace Tree Encoder

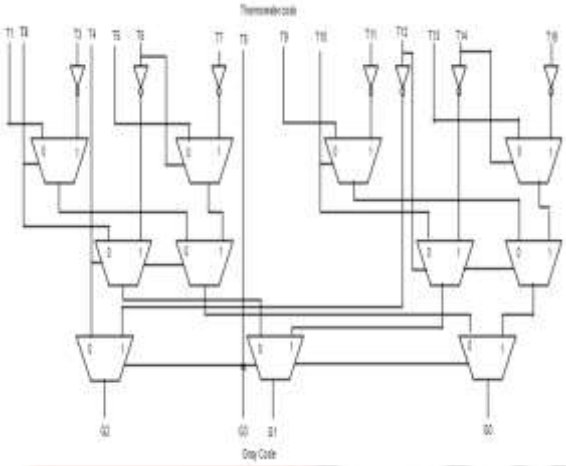
The basic building block of Wallace tree structure is full adder. For a 4 bit ADC it requires 11 full adder circuits and are connected as shown in figure. A full adder circuit itself contains many transistors which in turn makes the complete encoder bigger and area consuming. So this circuit consumes more average power and maximum delay also becomes more. The number transistors used in this circuit is more compared to other encoder architectures.





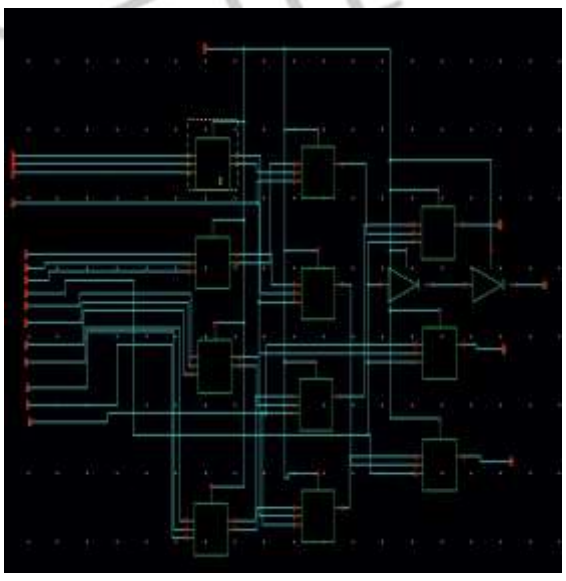
Gray code based encoder using 2:1 Multiplexer

The circuit is implemented using basic gates and here it is using 2:1 Multiplexers. Here we have to use additional inverters at the input port to get the gray code. These extra inverters spoil the advantage of this architecture in terms of power consumption and area. Moreover it requires 11 multiplexers for the realization of 4 bit architecture.



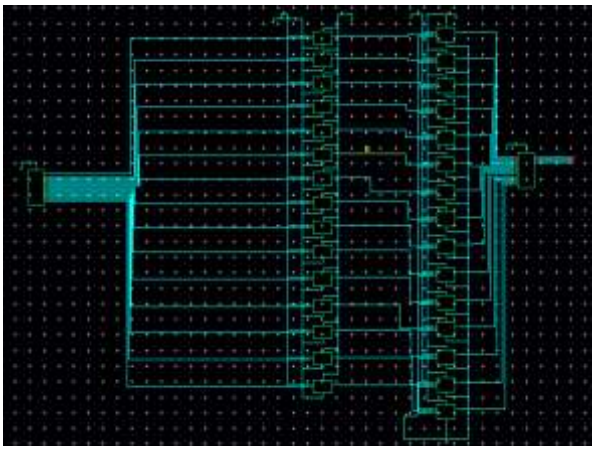
Heterogeneous Encoder

Heterogeneous encoder can be implement from the any of existing encoders like Wallace tree encoder or Fat tree encoder. Heterogeneous encoder consists of full adder and multiplexer circuit as shown. In this selection signal is used form MUX, which is critical.



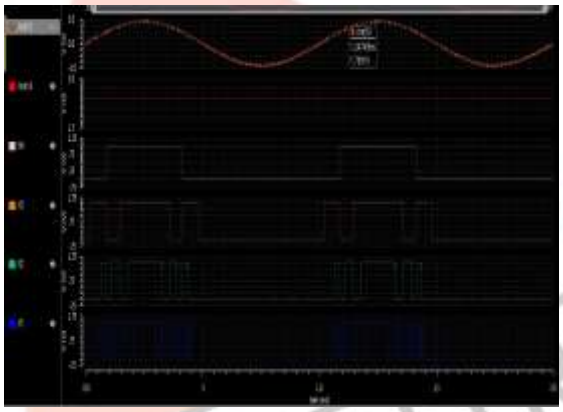
This can tolerant the bubble error and remaining signal can be used as inputs. Wallace encoder is also free from bubble error but it is complex in circuit. Hence, the proposed heterogeneous encoder is easy to design and also it consumes less power.

Implementation of Flash ADC using Heterogeneous Encoder



III. SIMULATION RESULTS:

The ADC is designed and implemented in standard gpdk180nm using CMOS technology. The proposed encoder design is used in ADC design in order to decrease the area of flash ADC. The Wallace Tree Encoder requires 8.280mw (Power), 54.45 nsec (Delay), 242 Transistors and Heterogeneous Encoder requires 8.335mW (Power), 25.39nsec (Delay), 130Tansistors and the results shows that the Heterogeneous Encoder is area efficient compared previous architectures.



REFERENCES

[1]. D.Lee, J.Yoo, K.Choi and J. Ghaznavi, "Fat-tree encoder design for ultrahigh speed flash analog to digital converters" I proc. IEEE Midwest Symp. Circuits Syst, pp 233-236, Aug 2002.

[2].Chung-Hsun Huang, Jinn-Shyan Wang, "High-performance and power-efficient CMOS comparators", IEEE Journal of Solid-State Circuits, vol. 38, no. 2, pp. 254 – 262, Feb. 2003.

[3]. Vinayashree Hiremath, Saiyu Ren "An Ultra High Speed Encoder for 5GSPS Flash ADC ", IEEE Conference on Instrumentation and Measurement Technology, pp 136-141, May 2010.

[4]. S. Sheikhaei, S. Mirabbasi, A. Ivanov, "An Encoder for a 5GS/s 4bit flash A/D converter in 0.18um CMOS", Canadian Conference on Electrical and Computer Engineering, pp 698-701, May 2005.

[5]. Nikoozadeh, A., Murmann, B., "An Analysis of Latch Comparator Offset Due to Load Capacitor Mismatch", IEEE Transactions on Circuits and Systems II, Vol. 53 , no. 12, Dec. 2006.