Improved SNR Integrator Design with Feedback Compensation for ∑Δ Modulator

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***Abstract* - This paper represents a method to improve the SNR and linearity of an integrator by feedback compensation technique. The discussed design reduces signal swing while keeping advantages of both feed-forward as well as feedback topology without changing the signal transfer function. SNR and linearity are related to the output of an integrator. Reduced SNR and non-linearity resulted because of the integrator's output swing that is due to change in input. Proposed integrator design significantly increases the SNR. This integrator is designed using 180nm CMOS technology.**

***Index Terms* - Sigma-Delta modulator, feed-forward compensation, feedback compensation, operational amplifier.**

I. INTRODUCTION

Sigma Delta converter have received much attention in recent years in VLSI industry, due to technological advancement. A general figure of sigma-delta (Σ-Δ) modulator is shown in fig.1. The sigma-delta (Σ-Δ) ADC is the converter used in recent voice-band, audio, and high-resolution precision industrial measurement applications. Due to implicit anti-aliasing filter, Continuous time sigma-delta (Σ-Δ) modulators are the best solution for digital front ends, and 90% of die is implemented in digital circuitry which enhances the vision of CMOS technology. In present scenario of CMOS processes the highly digital architecture is suited, thereby allowing easy addition of digital functionality without significantly increasing the cost.

As CMOS technology advances, size of the transistor reduces and the speed increases which enables higher-speed communications and more complex systems. These benefits come at the cost of decreasing intrinsic device gain, increased transistor leakage currents, non-linearity and other mismatches due to process variations [1]. All of these drawbacks influence the design of these analog-to-digital converters (ADCs) in nanometer scale CMOS processes.

Sigma-delta modulator has a quantizer having a control loop around, hence it requires more compensation for stability which can be provided either by feedback (FB) topology or feed-forward (FF) topology or a combination of both topologies [2]. If feed-forward topology is implemented then it offers advantages in linearity and power but also offers large peaking in signal transfer function. If feedback topology is implemented then also non-idealities of integrator in not suppressed. The mixed topologies implemented in [2] and [3] could not solve the issue at the output of the integrator or could not remove the peaking in the signal transfer function.

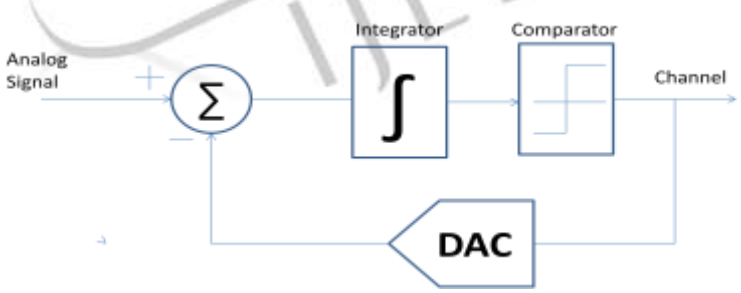

Fig. 1 Basic Sigma-Delta Modulator

Another technique uses feedback path as well feed-forward path in which a high pass filter is added in the feedback path and a low pass filter added in the feed-forward path [4], this method provides a good signal transfer function roll-off, but active elements are also required for implementation. In this paper we present a technique which alters the feedback topology by decreasing the signal swing at the output of integrator analogous to feed-forward topology.

Section II discusses the 2^{nd} order sigma-delta modulator and Section III discusses implementation of improved integrator with Σ-Δ modulator while simulated results are presented in Section IV and conclusions are discussed in Section V.

II. 2ND ORDER SIGMA-DELTA MODULATOR

The transfer characteristics of both feed-forward and feedback topology has to be analyzed in order to see the advantages of feed-forward in feedback topology. Feed-forward topology and feedback topology is shown in figure 2(a) and 2(b) respectively. We have chosen 2nd order Σ-Δ modulator as it is the basic design for the method.

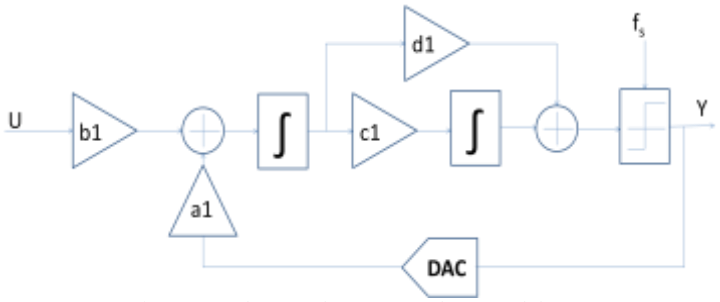

Fig. 2(a) Feed Forward compensated Σ-Δ modulator

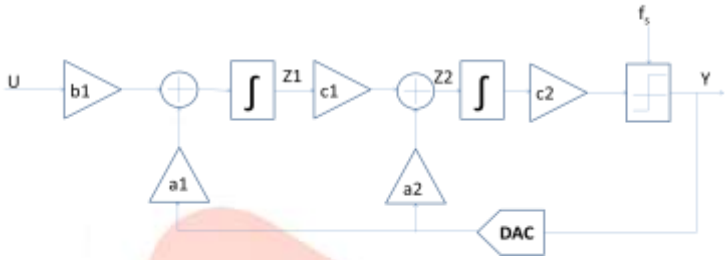

Fig. 2(b) Feedback compensated Σ-Δ modulator

The ideal integrator gain at DC is infinite that means to obtain a finite level of output, input should be zero. With decrease in the integrator's gain the input signal may increases with the increasing frequency. From figure 2(a) the 1st integrator output is connected directly to the next integrator of 2nd order sigma-delta modulator which yields in the suppression of signal at lower frequencies. The feedback compensated modulator (figure2 (b)) provides the suppression of signal at node Z_2 but has signal swing at node Z_1, it originates because of summation following the 1st integrator.

The signal transfer function has low pass characteristics similar to the transfer function of 1st integrator. Our aim is to achieve high pass characteristics at the output of 2nd integrator.

III. PROPOSED 2ND ORDER Σ-Δ MODULATOR

The proposed circuit is shown in figure (3). In this Σ-Δ modulator we have B_1 and B_2 as additional blocks. The purpose of these blocks is to affect the swing at the node Z_1, the transfer function of these blocks are realized in s-domain by analog circuitry. Realization of these blocks is done such that it does not affect the signal transfer function and noise transfer function. Transfer function of B_1 and B_2 are related as:

$$B_2(s) = 1 - \frac{B_1(s) c_1 f_s}{s} \quad (1)$$

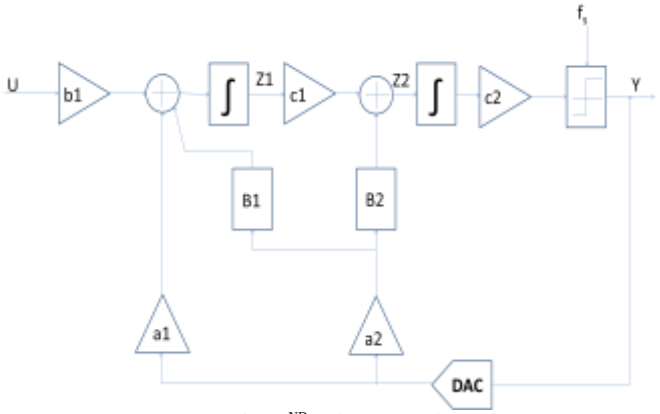

Fig. 3(a) Modified 2ND order Σ-Δ modulator [5]

The standard implementation of block B_1 and B_2 is such that $B_1 = 0$ and $B_2 = 1$. Feed-forward architecture characteristics can be achieved through modified 2nd order sigma-delta modulator by $B_{1\ act}$ as differentiator and B_2 is zero. We have implemented through capacitive feedback. The Capacitive feedback is shown in figure 3(b).

In the capacitive feedback implementation block $B_1 = s/c_{1\ acts}$ as a differentiator while block $B_2 = 0$, that yields a replica of feed-forward compensation that is discussed in Section II. This implementation bypasses the 1st integrator with capacitor discussed for the last integrators in feed-forward compensated modulators in [5]. This design results in total cancellation at DC which yields in the signal cancellation for lower frequency at the output of 1st integrator. Simple design and exceptional impedance matching make this methodology advantageous. This methodology reduces the effect of non-linearity at the output of 1st integrator to a greater extent by increasing the overall signal to noise ration of the integrator.

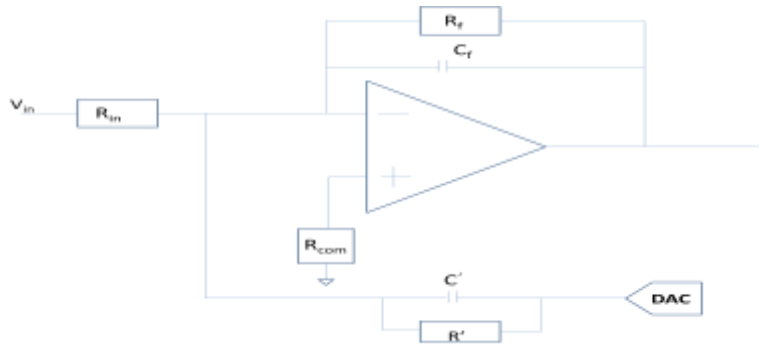

Fig. 3(b) Proposed 2ND order Σ-Δ modulator with Capacitive Feedback

The values of the components in dual feedback structure of proposed integrator design are given in Table. I.

TABLE I: VALUES OF COMPONENTS

Component Name	Value
R_f	350 KΩ
C_f	10 nF
R_{in}	35 KΩ
R_{comp}	10 MΩ
R'	84.75 KΩ
C'	10 µF

IV. SIMULATION RESULTS

The 1st integrator is also implemented at transistor level with the capacitive feedback method in the Cadence Virtuoso. The amplifier used for the integrator is a 2 stage operational amplifier having a unity-gain bandwidth of 27.5MHz and power dissipation of 252uW. The gain of the integrator is 65dB with a phase margin greater than 60°. In this simulation we compare non-modified sigma-delta modulator with the proposed structure. The linearity mainly depends upon the output of the first integrator, so both of the 1st integrators output is compared i.e. integrator of the conventional sigma-delta modulator and integrator of the proposed sigma-delta modulator. Using the FFT data SNR is calculated excluding first five harmonics as they dominate, thus leaving only noise terms. On comparing the SNR results of conventional and, it was observed that SNR significantly improves from 35dB to 77dB.

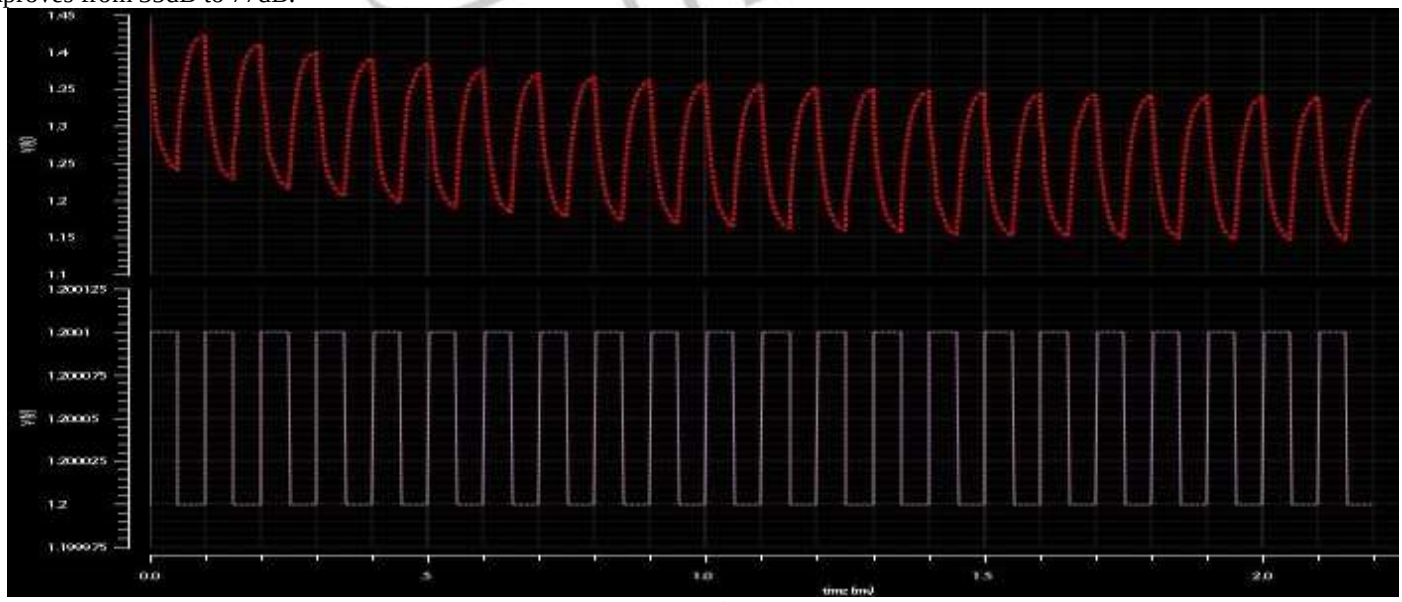

Fig. 4 Transient response of regular integrator.

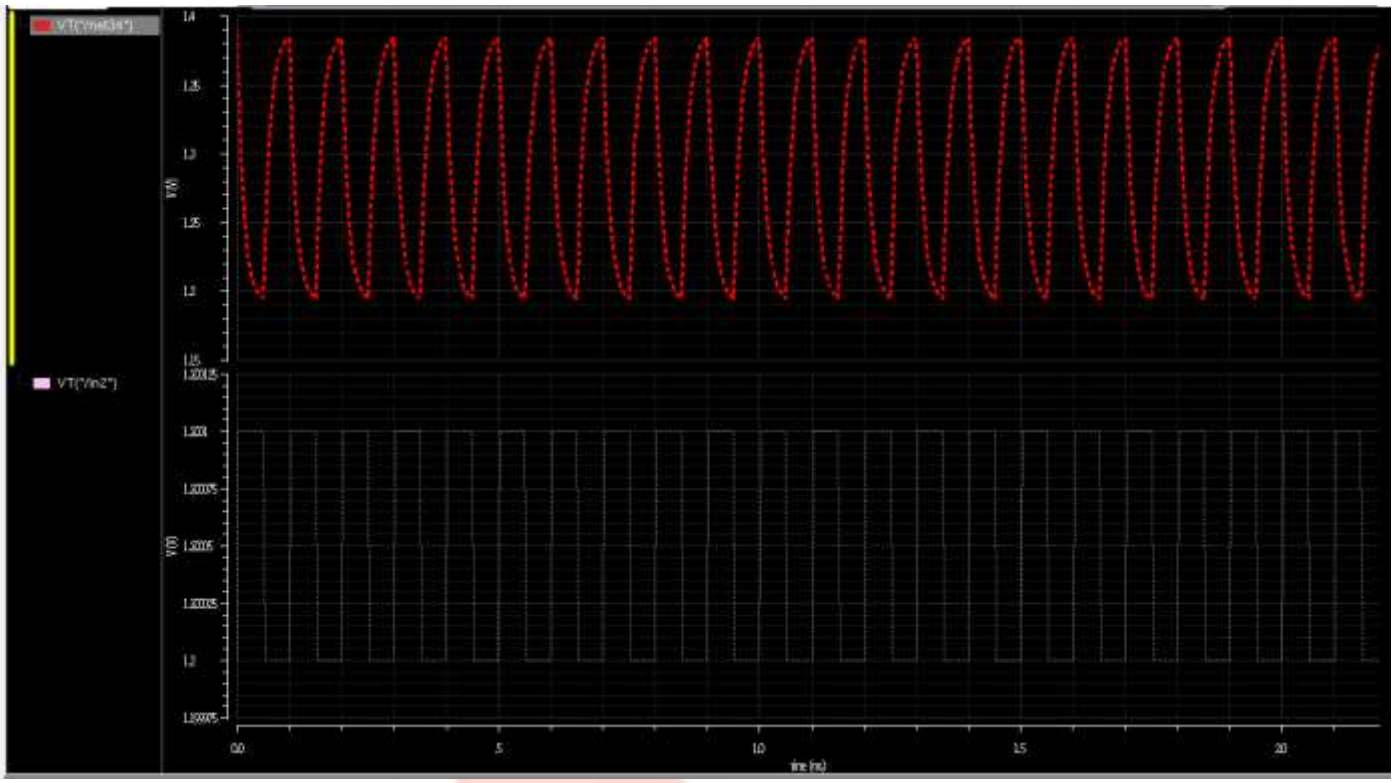

Fig. 5 Transient response of proposed integrator with improved linearity

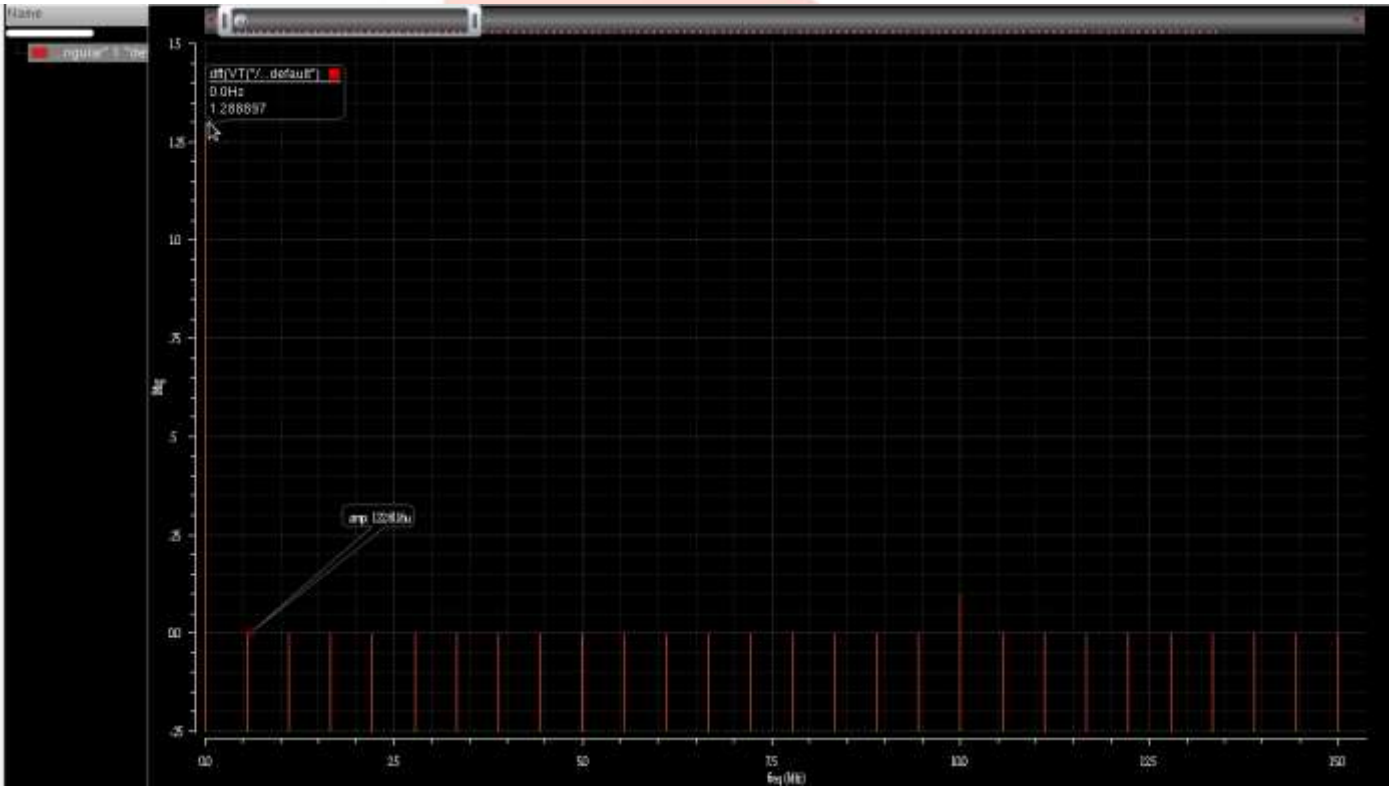

Fig. 6 FFT of proposed integrator

v. CONCLUSION

The modified method for the feedback compensated sigma-delta modulators with capacitive feedback technique is presented. A result of Simulation proves that this methodology is very favorable for possible application. Using this technique signal to noise ratio (SNR) is increased and non-linearity reduced to a significant extent.

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