A 97dB, 21µW uncompensated CMOS Operational Amplifier Design for Biomedical Applications

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***Abstract* - In this paper the challenge of enhancing the gain and reducing the power requirement of amplifiers, preferably used in biomedical applications is addressed by demonstrating that composite cascode stages, operating in subthreshold/weak inversion regions provide a method of designing a ultra high gain (97dB) and low-power (21µW) op amp with 1.5V power supply. The op amp is designed without compensation capacitor. Additional advantages of this op amp design include low input noise and small chip area. Thus this design is applicable in biomedical applications where low power, low noise amplifiers, efficient in amplifying bio-signals in mHz-KHz range are required. The op amp is designed using 180nm CMOS technology and simulations that demonstrate results are given.**

***Index Terms* - high gain, low power, low input noise, subthreshold, weak inversion, composite cascode.**

I. INTRODUCTION

Biomedical electronics is fast becoming a significant part of the healthcare engineering. Biomedical devices are extensively used in diagnosis of life threatening diseases and other conditions, or in cure and prevention of such diseases. They are widely used in cardiac pacemakers for cardiac arrhythmia, in rental implants for blindness or in cochlear implants for deafness. Considerable research is going on in brain-machine interfaces for paralysis, stroke and blindness [1]. All biomedical devices consist of a high gain amplifier circuitry inbuilt on the chip which is capable of amplifying weak physiological signals, so that they can be suitably amplified to higher levels before further processing. This circuitry has to be designed for minimal power consumption to adhere with stringent power constraint.

Recent research on low power biomedical amplifiers has generated significant attention toward gain stages that provide ultra-high gain with low current draw. This work presents op amp design which utilizes the subthreshold/ weak inversion operation of composite cascode stages to achieve high voltage gain [2],[3] low power [3], low noise, low chip area, and low bandwidth. Low bandwidth is often considered a limitation but here, it eliminates the need of a compensation capacitor to achieve stable operation in the presence of feedback [2]. Required chip area, also get reduced by this uncompensated op amp design.

Section II and Section III discusses contemporary low power biomedical amplifier architectures and architectures using composite cascode stages operating in subthreshold/ weak inversion region while Section IV presents proposed work. Simulation results and conclusions are discussed in Section V and Section VI.

II. CONTEMPORARY LOW POWER BIOMEDICAL AMPLIFIER ARCHITECTURES

Several architectures have been implemented to achieve high gain (> 90dB) and low power (< 1mW) amplifying systems using gain boosting stages or bulk driven MOS structures, for biomedical applications.

In amplifying systems using short channel devices, system gain reduces due to short channel effects but by employing gain boosting stages these effects can be negated and sufficiently high gain systems can be implemented even using short channel devices. In [4], active cascode configuration is used as an effective method for boosting the gain available from conventional MOSFET cascode structure. In this configuration, as shown in Fig. 1, differential amplifier provide negative feedback to MOSFET M_2, thus keeping the voltage on the gate of M_2 at V_{ref}. This increases the output impedance of M_2 resulting in higher gain. However operational amplifiers implemented using gain boosting technique face severe limitations in terms of instability, power consumption and chip area. The differential amplifier driving the gate of MOSFET M_2 needs to have higher f_{-3dB} frequency than the overall bandwidth of designed operational amplifier. If not the gain reduces which in turn results in increased instability. Each gain boosting stage employed requires biasing differential amplifier and reference voltage source, which continuously draw currents from the supply resulting in increased power consumption and they also require valuable chip area.

Another popular method of implementing high gain amplifying systems is using bulk driven MOS structures. In these structures signal is applied at the bulk and DC bias voltage, V_{bias} is applied at the gate [5]. A cascode stage using this configuration is shown in Fig.2. This method provides high gains at low power consumption due to lower headroom requirements. As current through the bias voltage source into gate of MOSFET reduces power consumption also get reduced. But the transconductance of bulk driven structures is much smaller compared to transconductance of gate driven structures. Thus bulk driven structures provide lowered gain and bandwidth than gate driven structures. Bulk driven devices also require additional fabrication steps, as a well has to be formed around the device to insulate other devices in remaining bulk from possible leakages.

The best features of both gain boosting technique and bulk driven technique can be combined in amplifying systems implemented using composite cascode stages.

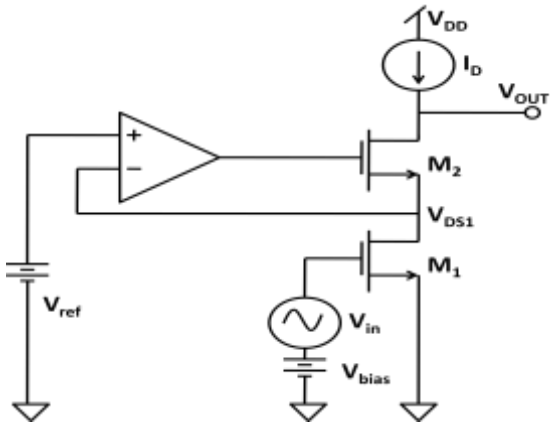


Fig. 1 Active cascode configuration used in conventional cascode structure for gain boosting [4]

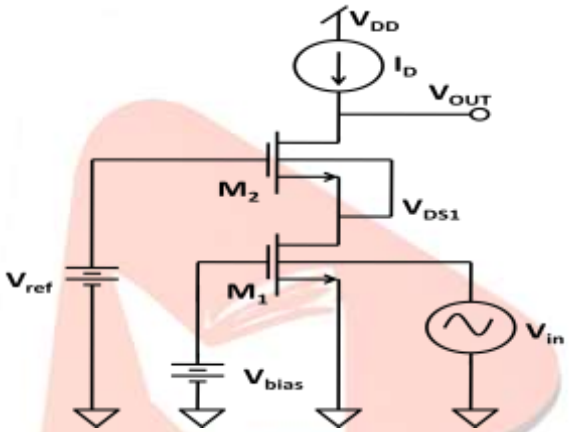


Fig. 2 Bulk driven cascode configuration for increased gain [5]

III. BIOMEDICAL AMPLIFIER USING COMPOSITE CASCODE STAGES

In cascode configuration implemented using MOSFET, the source of the upper device is connected with the drain of the lower device and both the devices are independently biased. While in composite cascode configuration the gates of both the devices are tied together, thus requiring one less biasing voltage sources. Moreover it is been shown by Comer et al. [6], that high gain amplifiers can be implemented by operating composite cascode configuration in weak or moderate inversion region.

Typical MOS amplifier operate in active (Saturation) region, but even within active region devices can be biased to strong inversion region, moderate inversion region or weak inversion region. In weak and moderate inversion the number of free carriers in the channel is small leading to a small drift current but diffusion current is significant, and the MOSFET act more like a BJT [3],[7]. Device operating in these regions are considered to be in subthreshold region of operation. Inversion coefficient (I_{coeff}) of a device indicates the inversion level of a MOS device. Typically a device having $I_{coeff} < 0.01$ is considered to be in subthreshold/ weak inversion region. I_{coeff} is defined as [7]:

$$I_{coeff} = \frac{I_D}{I_0 \frac{W}{L}} \tag{1}$$

where, I_D is drain current through MOS device, W is width of the device, L is length of the channel and I_0 is the technology current, which is the intrinsic current flowing through the device, having both W/L ratio and I_{coeff} equal to unity. I_0 typically depends upon the fabrication process and is given as:

$$I_0 = 2\mu n C_{ox} U_T^2 \tag{2}$$

where, μ is the mobility of charge carriers in MOS device, n is substrate factor extracted from experimental data, C_{ox} is capacitance per unit area of oxide layer and U_T is thermal voltage (26mV at 300 K). In subthreshold/ weak inversion region the drain current, I_D is experimentally approximated as [3]:

$$I_D = \frac{W}{L} I_0 e^{\frac{qV_{GS}}{nKU_T}} \quad (3)$$

where, V_{GS} is slightly less than V_T (about 10mV-20mV below V_T). Subthreshold operation of small channel devices provides high gain, lower power dissipation, low threshold voltages and smaller input noise densities but at the cost of lower operating bandwidths. Since for operating devices in subthreshold region their size has to increase which in turn increases gate to bulk capacitance, thus lowering the intrinsic bandwidth. However both thermal noise density and flicker noise density decreases with lower inversion coefficient.

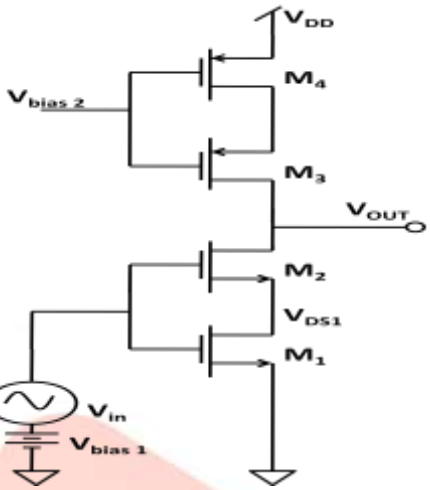


Fig. 3 Composite cascode configuration with composite cascode load

Above figure shows a single ended, composite casode configuration with composite cascode load. Device M_1 is sized such that it operates in strong inversion region while W/L ratio of M_2 is chosen for it to operate in subthreshold/ weak inversion region. Small subthreshold drain current flowing through M_2 provides large output resistance, when we look into the drain of M_2. This combined with composite cascode load, formed using M_3 and M_4, which also generates large output resistance, translates into very high voltage gains. Two single ended, composite cascode stages can be combined to realize a high voltage gain input differential stage having, low drain current and low bandwidth. Fig. 4 shows one such differential stage. However, in this low bandwidth is beneficial in providing dominant pole compensation in op amp. Here tail current source I_D supplies current (typically in nA range) to both the branches and to have maximum gain devices across from each other horizontally are matched.

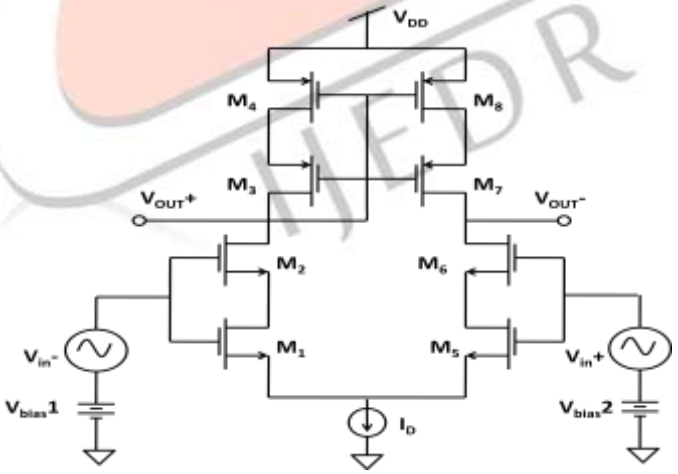
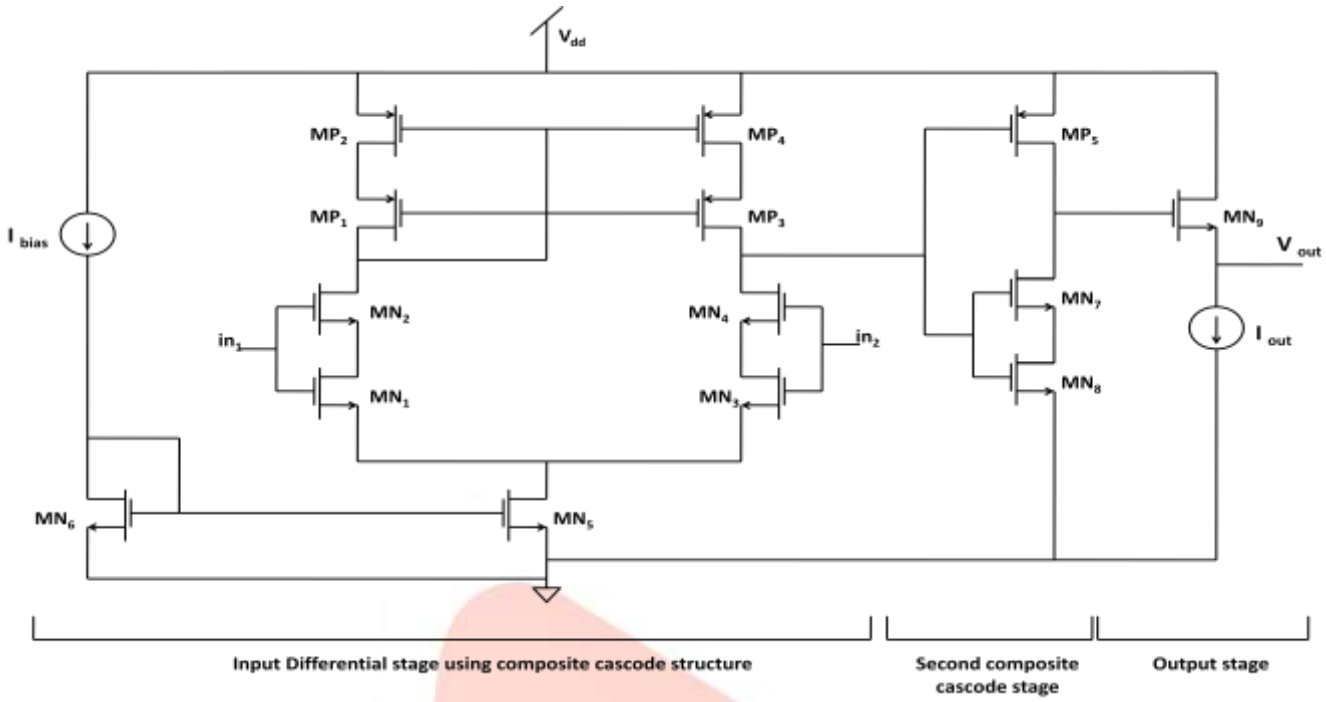


Fig. 4 Differential stage using composite casode configuration

IV. PROPOSED WORK

The proposed operational amplifier has three stages. First is the input differential stage using composite cascode configuration with composite cascode load to provide high voltage gain. Second is also a gain stage but its main objective is to provide considerable operating bandwidth for biomedical applications. This stage provides a fine balance between two design objectives, one to have low bandwidth for eliminating the need to have additional compensation capacitor between the output of first and second stage and another to have enough operating bandwidth for intended applications. Third stage is the output stage, which is simply a voltage buffer stage.

The schematic of the proposed operational amplifier is shown in Fig. 5. The amplifier is designed to operate at a voltage supply of 1.5V with no compensation capacitor required. The drain current through each arm of input differential stage is kept at 100nA by current source I_{bias} to achieve minimum possible power dissipation.



Transistors MN_1 and MN_2 are sized according to equation (1) for inversion coefficient 12 and 0.005 respectively, keeping I_D equal to 100nA, for them to respectively operate in strong and weak inversion region. Value of inversion coefficient is critical for designing as size of transistors increase proportionally with increase in inversion coefficient. Sizing of transistors MP_1 and MP_2 is done such that they provide a voltage drop of $V_{dd}/2$ across them. This is done to ensure maximum output resistance. Transistors, horizontally opposite in differential stage are matched to reduce offsets, so MN_1 and MN_2 are matched to MN_3 and MN_4, while MP_1 and MP_2 are matched to MP_3 and MP_4. Transistor MN_5 is biased to form tail current source and is sized such that 200nA current flow through it. MN_5 along with MN_6 forms a current mirror; hence they are matched to each other.

In second stage W/L ratio of transistor MP_5 is selected such that maximum possible current flow through it, to enhance operating bandwidth while keeping the size of transistor MN_7 and MN_8 small because increasing current through MP_5 increases drain current of MN_7 and MN_8, which in turn increases their size. As MN_7 and MN_8 form composite cascode pair increase in their W/L ratios, increases inversion coefficient which makes it difficult to operate them in strong and weak inversion region respectively. Thus a fine balance between transistor sizing's in second stage has to be maintained. In proposed amplifier drain current through MP_5 was kept at 4µA and output current source of 10µA is used. Aspect ratios of all transistors in proposed operational amplifier design are given in Table I.

TABLE I. ASPECT RATIOS OF PROPOSED OPERATIONAL AMPLIFIER.

INPUT DIFFERENTIAL PAIR		
Transistor	**W**	**L**
MN 1, MN 3	0.2µ	0.18µ
MN 2, MN 4	17µ	0.18µ
MP 1, MP 3	27µ	0.18µ
MP 2, MP 4	0.2µ	0.18µ
MN 5, MN 6	3.5µ	0.18µ
SECOND GAIN STAGE		
MP 5	0.3µ	0.18µ
MN 7	31µ	0.18µ
MN 8	5µ	0.18µ
OUTPUT STAGE		
MN 9	10µ	0.18µ

V. SIMULATION RESULTS

Operation of proposed operational amplifier was simulated in CADENCE Virtuoso 6.1.4 using gdpk 180nm library with 1.5V power supply at temperature variation of -5° to 50°. The magnitude and phase response obtained from AC analysis of the amplifier are shown in Fig.6 and Fig.7

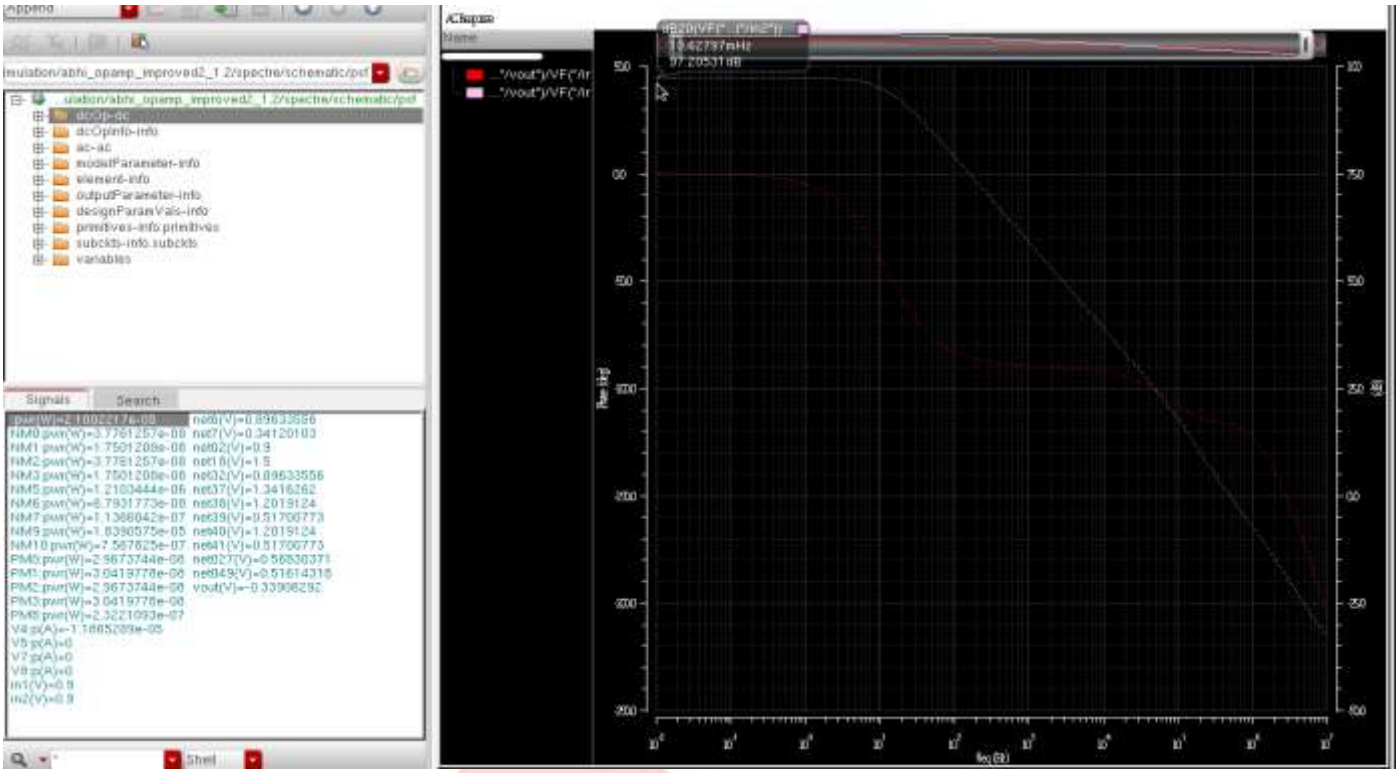


Fig. 6 Magnitude of proposed operational amplifier

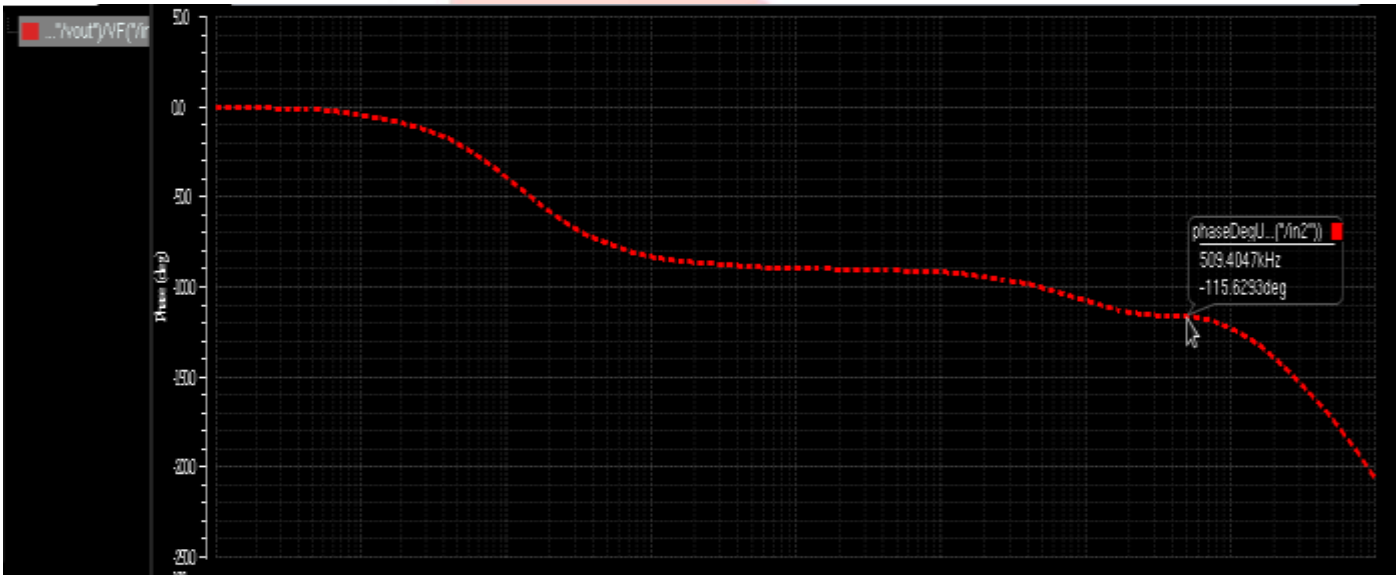


Fig. 7 Phase of proposed operational amplifier

The overall open loop voltage gain is 72,500 V/V (97.2 dB) at power dissipation of 21µW. The phase margin is 64^0 (180-116) which provides stability and unity gain bandwidth is 510 kHz. -3dB corner frequency is found to be 15Hz. Input referred noise density at 1KHz is found to be 0.2nV/sqrt(Hz). The required chip area for this amplifier design is significantly reduced removing the need of a compensation capacitor. Table II summarizes important results of the designed operational amplifier.

TABLE II. SUMMARY OF IMPORTANT RESULTS

Open loop gain, dB	97.2
-3dB corner frequency, Hz	15
Phase margin, degree	64º
Power dissipation, µW	21
Unity gain bandwidth, KHz	510
Input referred noise density @ 1KHz (nV/sqrt(Hz))	0.2

VI. CONCLUTION

This work shows the practicality of designing a high gain, low power uncompensated operational amplifier using composite cascode structures operating in subthreshold/ weak inversion region. The design is best suited for low power, low frequency biomedical application requiring high voltage gains.

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