Designing of low power barrel shifter using reversible logic

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Abstract **-** In the current development the concept of reversibility is finding its attention day by day. As in the reversibility no information can ever be lost. Reversible logic have received great attention for the reason that is consumes low power which is the basic requirement in vlsi designing. The important basic used logic gates are Feynman Gate, Modified Fredkin gate, toffoli gate, and peres gate etc. Reversible technology has find its important in barrel shifter also. This paper presents the basic reversible logic gates which are being used in designing barrel shifter and how the improvement is being done in the barrel shifter technology.This paper presents the proposed design of the improved bidirectional barrel shifter.

INTRODUCTION

Reversible logic is a emerging technology in which the input and the output can be uniquely retrieved from each other. In order to fulfill this there exist one to one mapping linking input and output. As per R.landauer demonstration in an irreversible circuit losing a bit causes dissipation of about KTln2 joules of energy where k=1.3806488×10^{-23} $m^2kg\,s^2k^6$ (joules $kelvin^{-1}$) is Boltzmann constant and T is absolute temperature at which operation is being performed. So in order to recover the efficiency with which we erase information we use reversible logic as they dissipate a little heat. Reversible logic have many applications in the emerging technologies such as quantum computing ,digital signal processing and optical computing etc. The vital use of reversible logic is in quantum computing. Quantum computers are network of reversible logic gates where each gate perform a unitary operation on one ,two or more state quantum system called qubits. Multiple-valued logic (MVL) can be used to reduce the width of quantum circuit. In Multiple Valued Logic the ternary quantum reversible logic are being widely used. As binary logic can exit only in two states: 0> and 1> so we started using ternary logic as it can exit in superposition of the two states.

REVERSIBLE GATES

A Reversible Gate is an n-input, n-output (denoted by n * n) reversible circuit having one-to-one mapping in order to link the input and output. In the reversible logic inputs can be retrieved from output. Several dummy output signals are needed to be produced in order to maintain the reversibility property of reversible logic gates and to equal the number of input to that of output. These signals are commonly recognized as Garbage Outputs. In this there is no chance of losing the information as the data can be recovered by computing backward.

TERNARY QUANTUM GATES

Ternary quantum gates qutrit states are |0> |1> |2> .Ternary shift gates are 1*1 mapped gates that operate on single qutrit state. Six quantum ternary reversible gates were realized in [10] where the addition (+) and multiplication (.) are over modulo three or galois field 3 (GF3).

Muthukrishnan-Stroud gates

Muthukrishnan and Stroud projected a family of ion-trap realizable 2-qudit primitive ternary gates [8], which apply one of the below unitary transforms, except buffer, on the second qudit (the controlled qudit) provided that the first qudit (the controlling qudit) is at the highest value.

Gate Name	Gate Symbol	Logic State		
		0	1	2
Buffer	$x \rightarrow x$	0	1	2
Single–Shift	$x \rightarrow +1 \rightarrow x+1$	1	2	0
Dual–Shift	$x \rightarrow +2 \rightarrow x+2$	2	0	1
Self–Shift	$x \rightarrow 12 \rightarrow 2x$	0	2	1
Self–Single–Shift	$x \rightarrow 01 \rightarrow 2x+1$	1	0	2
Self–Dual_Shift	$x \rightarrow 02 \rightarrow 2x+2$	2	1	0

Figure1: various shift gate

The diagram of an M-S gate for ternary logic is shown in Figure 2. Here, input B is the controlled input and input A is the controlling input. The output P is equal to the input A.Output Q is the Z-transform (Z ∈ {+1, +2, 12, 01, 21) of the input B if A = 2, otherwise Q = B.

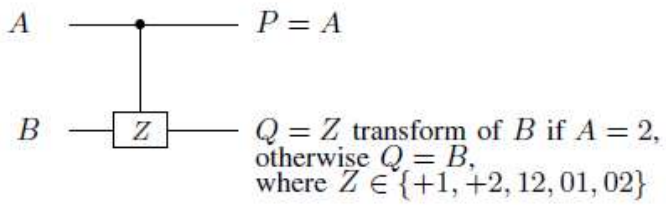

Figure2:Design of MS gate

Realization of ternary gates using MS gate

Ternary Feynman Gate

Ternary Feynman gate is 2-input and 2-output reversible logic having A and B inputs being mapped to (P=A, Q=A+B) where A is controlling input and B is controlled output. The input A can only be applied to the output P and Q if and only if input B is kept constant at 0.The advantage of this is that it helps in avoiding the fan out which is the necessity of the reversible logic. The Feynman gate can be realized using two MS gates and 2 shift logics so its quantum cost is 4.The implementation of ternary Feynman gate is as shown

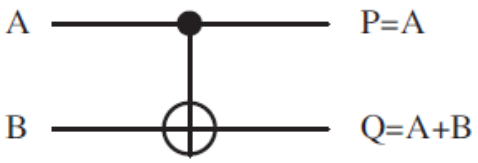

Figure3:Ternary Feynman gate

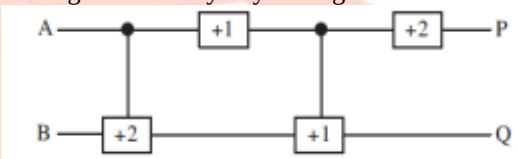

Figure4:MS realization of ternary Feynman gate

Modified Fredkin Gate

Toffoli and Fredkin introduced Fredkin gate for binary reversible logic which is one of the basic gates in quantum computing and reversible. Modified Fredkin gate (MFG) which is multi-valued reversible logic. was introduced by Picton.MFG gate is 4*4 reversible gate, having input being A mapped directly to P,input B mapped to Q and C mapped to R if A<B else R=D, S=D if A<B else S=C) P, Q, R, S are the respective output. The MGF gates can swap the input C and D if the value of A>=B else they remains unchanged. The Modified Fredkin Gate can be implemented by using 21 shift gates and 20 M-S thus the overall number of quantum gates is 41.

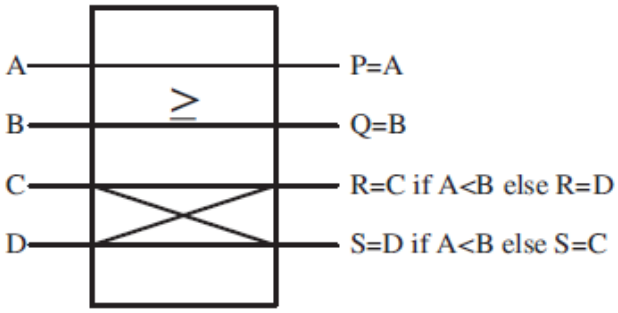

Figure5:Modified Fredkin Gate

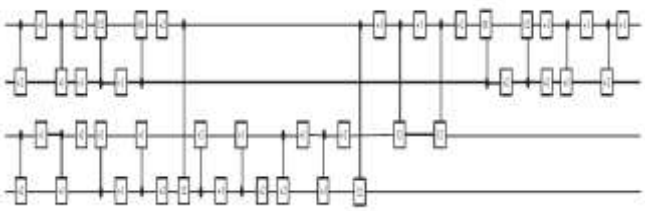

Figure 6:M-S realization of Modified Fredkin Gate

Ternary Peres Gate

Peres gate is considered as significant concept in entire reversible computing and the ternary quantum version .This gate is also imperative for ternary quantum logic synthesis. Ternary Peres Gate (TPG) is 3*3 reversible gate, having inputs (A,B,C) being mapped to (P = A, Q = A+B, R = AB+C), where P, Q, R are the respective outputs. The Ternary Peres Gate can be implemented using six shift gates and seven M-S gates thus the total number of quantum gates is 13.

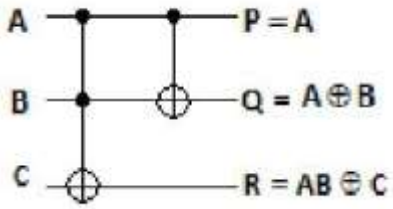

Figure7:Ternary Peres Gate

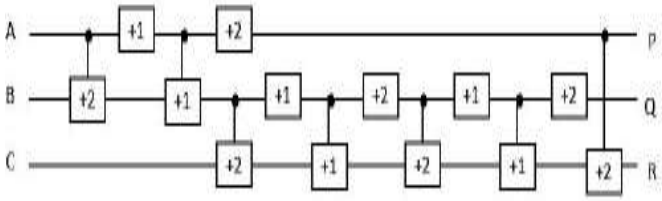

Figure8:MS realization of Ternary Peres Gate

BARREL SHIFTER

A Barrel shifter is combinational logic circuit with n inputs, n outputs and k select lines that controls the bit shift operation. Unidirectional barrel shifter allow the data to be shifted only to left (or right), but bidirectional barrel shifter can allow data to be shifted or rotated in both the directions. A barrel shifter having n inputs and k select lines is called (n, k) barrel shifter.

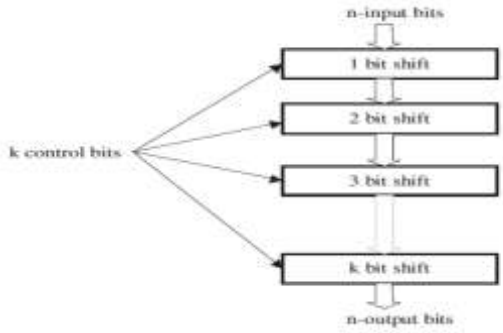

Figure9:logarithmic barrel shifter

Different design alternatives for barrel shifters that perform the following operations: shift right logical, rotate right, shift right arithmetic, shift left arithmetic ,shift left logical, and rotate left are Mux-based data-reversal barrel shifters, mask-based data-reversal barrel shifters , mask-based two's complement barrel shifters, and mask-based one's complement barrel shifters. On the basis of delay and area many design barrel shifters are being compared for various operand sizes and have reached the conclusion that data-reversal barrel shifters have less area than two's complement or one's complement barrel shifters and that mask-based data-reversal barrel shifters have less delay than the other designs. Mask-based data-reversal barrel shifters are especially attractive when overflow and zero detection is also required, as the detection is performed in parallel with the rotate or shift operation. One more substitute design of barrel shifter is logarithmic barrel shifter. A logarithmic (m, K) barrel shifter has m-bit

input data and K select lines that control bit shift operations. The logarithmic barrel shifter has $k = \log_2 n$ stages so that i=0, 1, …, (K–1).In every stage if di control signal equals one then 2i times shift will occur in input data, or else the input data will not alter. The irreversible logarithmic shifter is being realized using 2×1 multiplexers.

LITERATURE REVIEW

In 2007 Asif I. Khan, Nadia Nusrat, Samira M. Khan and Mozammel H.A. Khan [9] realized the ternary Toffoli gate and modified Fredkin gate. Realization of the quantum circuits is done using generalized ternary gates and Feynman gates and then are being replaced with their equivalent realization using Muthukrishnan-Stroud gates. The ternary quantum gates realized by them are more efficient and have less quantum cost.

In 2010 Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan [3] propose a proficient architecture and design of a reversible ternary barrel shifter. The ternary barrel shifter is being realized using the Modified Fredkin gates (MFG) and the ternary Feynman gates. In this they used the multiple valued reversible logic in order to design the (4:2) ternary barrel shifter which was being attempted first time in literature. In order to calculate the quantum cost they have used the MS-gate and shift gate which is being used in implementation of reversible barrel shifter.In this quantum cost , ancilla bits and garbage output is being calculated.

In 2012 Nayereh Hosseini Nia [2] proposed optimized (4, 2) Reversible bidirectional logical barrel shifter, optimized (8, 3) Reversible right barrel shifter & GRS-bit generation and optimized (8, 3) Reversible normalization logical left barrel shifter for floating point arthimetic for the first time in literature. The proposed optimized binary shifters are designed using Feynman gates, Fredkin gates and Peres Gates. Some parameters such as the amount of garbage outputs, the number of constant inputs, size of the circuit and quantum cost are being calculated.

In 2015 Nusrat Jahan Lisa and Hafiz Md. Hasan Babu [1] Proposed the two new designs of ternary barrel shifter the first design is ternary unidirectional barrel shifter and the second design is ternary bidirectional barrel shifter. They even proposed the ternary peres gate which is being used in the implementation of the proposed design the new technique to calculate the gate complexity is also being proposed. And the comparison of garbage output, ancilla bit and quantum cost is also being done . The compared results proved that the proposed work is more efficient than the existing work.

EXISTING WORK

The existing design of ternary unidirectional and bidirectional barrel shifter can perform right or left shift. They are implemented using ternary Modified Fredkin gates (MFG) ,ternary Feynman gates (TFG) and proposed ternary Peres gates (TPG).A 4-bit ternary unidirectional barrel shifter has two stages (ki, i = 0, 1). A bidirectional logarithmic logical shifter is a non-rotating barrel shifter which can shift input data to right or left. It has a control signal (K) for signifying the direction of the shift. If K signal is set to one then the logical shifter will work as a logical left shifter otherwise it will work as a logical right shifter.

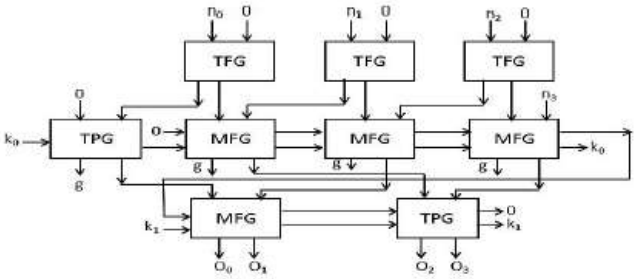

Figure10:Existing ternary unidirectional barrel shifter

The 4-bit bidirectional barrel shifter which is shown has two stages (ki, i = 0, 1) and it is implemented by ternary Modified Fredkin gates (MFG) ,ternary Feynman gates (TFG) and proposed ternary Peres gates (TPG). The ternary Feynman gate is used to avoid the fan-out. The ternary MFG and TPG are implemented as 2*1 multiplexer and AND gates. It has k1,k0 as select inputsand n3,n2,n1,n0 as data inputs .

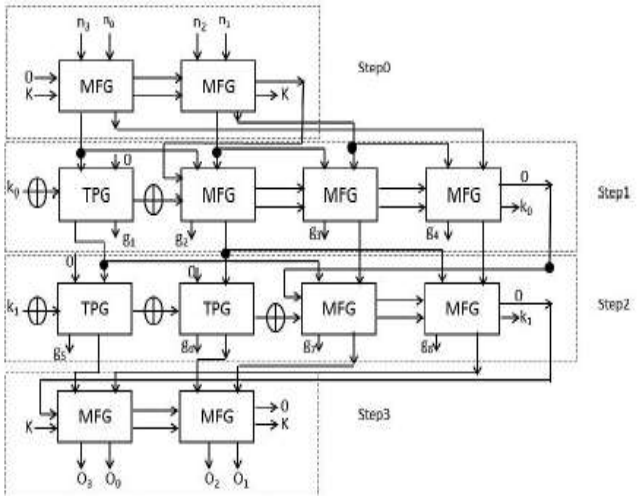

Figure11:Existing ternary Bidirectional barrel shifter

PROPOSED WORK

The ternary unidirectional barrel shifter was being designed using ternary Feynman gates (TFG), ternary Modified Fredkin gates (MFG) and proposed ternary Peres gates (TPG). In the proposed ternary barrel shifter the ternary peres gate at the input is being replaced by modified peres gate which performs the same function but its MS gate complexity is less by replacing the agte at the input the overall gate complexity can be reduced.

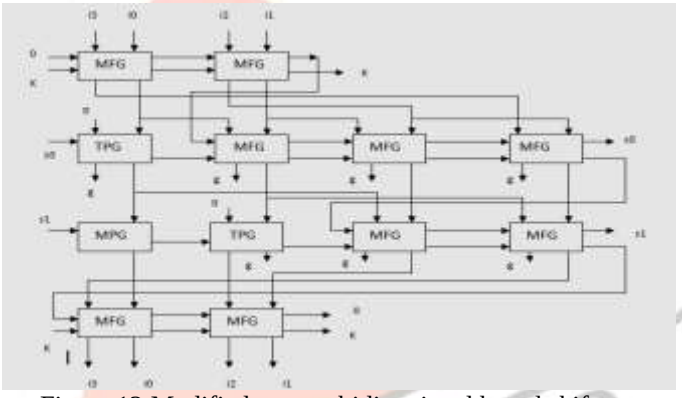

Figure 12:Modified ternary bidirectional barrel shifter

CONCLUSION

We have presented an approach to realize the unidirectional barrel shifter which consumes less power and the less no.of gates in its implementation. This work can form an important move in CMOS technology. It has the application in the various fields like quantum computing ,nanotechnology ,DSP technology and in designing of low power CMOS circuit.

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