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Performance analysis of Carbon Nanotube Field Effect Transistor with Dual material Gate

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Abstract – **In current years, the development towards device miniaturization is done to increase the performance and to reduce inconsistency and power consumption of the circuit. It causes to the introduction of three-dimensional device channel structures for example cylindrical device structure. Short channel effects are diminished by these structures. Scaling of device has been done in nanometer range. Improvement of switching in nanoelectronics, Carbon Nano Tube (CNT) could be used in nanoscaled MOSFET (Metal Oxide Semiconductor FET). In this paper depth study of performance of DMG-CNTFET is done. These performance characteristics are compared with conventional CNTFET(C-CNTFET). Firstly we have discussed the carbon nanotube structure. Then Conventional CNTFET and Double metal gate CNTFET output and transfer characteristics are plotted. Simulation is done at 20 nanometer channel length. Performance parameters of DMG-CNTFET are extracted using Atlas 2-D by Silvaco Inc. It is a numerical device simulator.**

Index Terms – **C-CNTFET (conventional carbon nanotube field effect transistor), DMG-CNTFET (Dual material gate CNTFET)** ***,*** **Atlas TCAD simulator.**

I. INTRODUCTION

Silicon based invention has been encountered exceptional growth in the most recent couple of eras. To accomplish high execution, scaling of MOSFET is going on and it is drawing nearer towards its limiting size. Consequently, the semiconductor manufacturing is seeing for various materials what's more, device to integrate with the present silicon based inorganic innovation and over the long duration, potentially supplant it. The CNTFET is the one which is most encouraging choice because it has prime electrical properties [1]. CNT field-effect transistors (CNFETs) have been realized based on semiconducting SWCNTs and intensively investigated. So far, two types of CNT transistor operation have been obtained. In conventional MOSFET-like CNFETs carrier injection is allowed from the metal contacts to the conduction band/valence band of the carbon nanotube without a considerable Schottky barrier. However, in Schottky barrier type CNFETs device, the Schottky barriers are present at metal contact. CNTs offer high ballistic transport, carrier velocity and inherent quasi-one-dimensional (1-D) nm scale structure [2]. Because of their quasi-ballistic properties they are particularly attractive for high-speed applications due to their quasi and high Fermi velocity. That's why CNTFETs pull in much consideration since their first demonstration. The CNTFETs are very-slim body devices which don't experience the ill effects of extreme mobility degradation which are commonly observed for Si-MOSFETs with nm measurements. Carbon nanotube transistors downsized to 10 nanometers or considerably shorter have drawn in a lot of interest. When length of the channel decreases on account of the extended charge sharing from source and drain short channel effects arise [3]. It has been already described that these effects can be reduced in MOSFETs by using a layer known as inversion layer. Inversion layer is used as a very thin extended drain/source in the sub 50 nanometer regime [4]–[7]. DMG-FET (Dual material gate FET) is the structure, that introduces ''gate material engineering'' in the place of ''doping engineering'' to improve SCEs and carrier efficiency both. To increase device performance and to reduce circuit power consumption three-dimensional channel device structures are introduced such as double gate, cylindrical gate structures. These channel geometries improve electrostatic control of the gate over the channel of the device, which reduce short channel effects (SCEs)[8]. To combine the benefits of CNTFET and DMG structures both, we propose another structure, DMG-CNTFET, just like that of a C-CNTFET using the different case that this is a cylinder shaped gate comprising of two distinctive metals having various WF(work function) . These metals with two different work functions converge into cylindrical shaped gate by reaching horizontally. In addition to this, here the at the first gate higher work function metal is selected near source and, at second gate lower work function metal is selected near drain.

Hence, in this research paper, the Double Metal Gate-CNTFET is recreated which utilizes 2D quantum simulation. These simulations are finished by the self-reliable arrangement of 2-Dimensional Poisson's Schrodinger equations, in the NEGF (non-equilibrium Green's function) formalism [9]. After this step necessary characteristics of DMG-CNTFET such as transfer and output characteristics are obtained. Our outcomes show that the suggested Double Metal Gate-CNTFET shows altogether lessened SCEs, therefore for superior CMOS circuit applications proposed structure is observed more trustworthy device configuration contrasted with the conventional CNTFET(C-CNTFET). Their characteristics are observed by silvaco atlas simulations.

This paper is divided into six sections; Section I is containing the introduction. Then after introduction in Section II carbon nanotube structure is discussed. After this, device structure with all the parameters is explained in Section III. Then simulation set up is given in IV. Result and discussion are given in the section V. At last conclusions are mentioned in section VI.

II. CARBON NANOTUBE (CNT)

CNTs are the graphene sheets rolled up into cylindrical forms. They are hollow cylinders having sp^2 bonded carbon with standard diameter of nanometer range. All atoms of the CNTs are arranged on the surface, mobility of the carrier is extremely high. The sp2 bonded carbon lattice remains exceptionally constant in biological environments. Depending upon the rolling up of the grapheme sheet CNT can exhibit semiconducting as well as metallic behavior. Firstly carbon nanotube was discovered by Ijima in NEC lab. The semiconducting nature of CNT is used to fabricate the CNTFET devices. CNT is used to fabricate CNTFET because of its very high conductivity. The CNTs have different energy band gap for different geometrical structures such as semiconductor or metal energy band. If we compare CNTFETs with bulk silicon FETs it is observed that CNTFETs can obtain a higher driving current, faster operating speed and significant reduction in power consumption because CNTs have exceptionally high mobility, and near ballistic transport [10]. Basic single wall CNT structure is presented in fig 1.

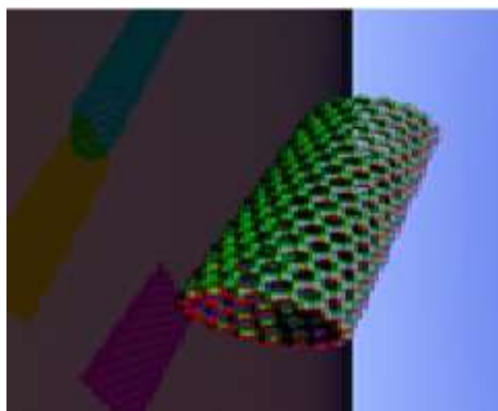

Fig 1 A Single wall CNT

III. DEVICE STRUCTURE

A schematic viewpoint of the recommended DMG-CNTFET is shown in figure 1. As it can be seen in the figure, the structure which is proposed in this paper is an improvement of a C-CNTFET, which is simulated in previous work. In this DMG-CNTFET structure, a (10, 0) CNT is taken that results in 1 eV band gap. Diameter of CNT is 0.8 nm, moreover this CNT is inserted in round and hollow HfO2 gate insulator. Thickness of insulator is 2 nm and its dielectric constant is 16. Channel is made of an undoped CNT with length 20nm, and n-doping is done at source and drain regions and these regions have 20 nm length. Doping at the source and drain region is taken 1.0 nm^{-1}. The cylindrical gate of the FET is of 20nm length. It comprises of two horizontally connecting metals having difference in work functions and lengths of these two metal gate is equal which is 10nm. The difference in work function of gate metals is taken because the threshold voltage near source should be more positive than near the drain. Therefore here work function $\Phi_1 > \Phi_2$ must be selected. In this paper Φ_1=4.7 eV Φ_2=4.4eV.

In this paper each parameters at DMG-CNTFET and conventional CNTFET are same except the gate is made of dual material having different work function in case of DMG-CNTFET. In conventional CNTFET gate material is single with work function 4.4eV.

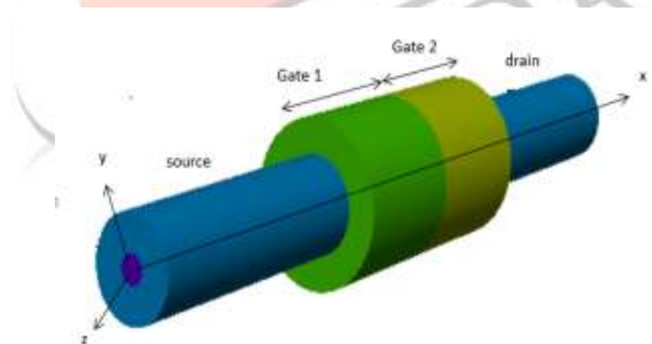

Fig. 2 DMG-CNTFET schematic structure

IV. SIMULATION SET-UP

The structure of DMG-CNTFET starts with a long intrinsic CNT. Then this intrinsic CNT channel is surrounded by hfo2 oxide layer. Then all around dual metal gate covers the oxide layer over a specific channel region. Then the source and drain electrodes are incorporated at the two sides of the CNT layer respectively. The DMG-CNTFET schematic diagram is illustrated in Fig. 2.

In this structure the gate is comprises of two metals having different work function. The first metal have work function of 4.7 eV and the second metal have the work function of 4.4 eV. Whereas in conventional CNTFET single metal is taken, which have work function of 4.4 eV.

In cylindrical coordinates the Poisson equation is basically a 2-D problem in z-direction (along the tube) and in the r- direction (radial direction) because the charge density and potential do not vary around the nanotube in the coaxially gate CNT transistor. Therefore self consistent electrostatic using 2-D finite difference method is obtained here. The potential profile follows the Poisson's equation which is given below.

$$\nabla^2 U_j(r,z) = \frac{q}{\varepsilon}\rho(r,z_j) \tag{1}$$

Where $U_j(r, z)$ denotes the electrostatic potential, ρ (r, z_j) denotes the net charge density distribution, ε is the dielectric constant. The net charge distribution ρ (r,z_j) is given by

$$\rho\ (r = r_{CNT}, z_j) = p(z_j) - n(z_j) + N_D^+ - N_A^-$$

$$\rho\ (r \neq r_{CNT}, z) = 0 \tag{2}$$

where N_A^- and N_D^+ denote the ionized acceptor and donor concentrations. r_{CNT} is CNT radius. Here it is to be assumed that dopants and charge (induced) are uniformly distributed all over the channel. One can calculate concentrations of electron and hole by using Schrodinger equation with boundary conditions open by means of the Non-equilibrium Green's formalism (NEGF).

Therefore the carrier concentrations are given by the following formula.

$$n(z) = \Sigma_b \int_{E_i}^{\infty} [f(E, E_{FS}) D_s^b(E,z) + f(E, E_{FD}) D_D^b(E,z)] dE \tag{3}$$

$$p(z) = \Sigma_b \int_{-\infty}^{E_i} \begin{matrix} [(1 - f(E, E_{FS})) D_S^b(E,z) + \\ (1 - f(E, E_{FD})) D_D^b(E,z)] \end{matrix} dE \tag{4}$$

where E_i represents the intrinsic Fermi level inside the carbon nanotube.

D_S^b, D_D^b are the bth subband source and drain local state density.

f(E) represents the Fermi distribution function.

E_{FS} and E_{FD} represent the Fermi energies at the source and the drain respectively.

The scrutiny of DMG-CNTFET device is completed using state of the art industrial standard Atlas 2-D numerical device simulator by Silvaco INC.

TABLE I. PARAMETERS OF SMG AND DMG CNTFET

Usage	SMG-CNTFET	DMG-CNTFET
Channel doping(cm^{-3})	2×10^{18}	2×10^{18}
Channel length(nm)	20	L_1=10, L_2=10
Gate oxide thickness(nm)	2	2
Gate workfunction(eV)	4.4	M_1=4.7, M_2=4.4
CNT radius(nm)	0.8	0.8
Source/drain region length(nm)	20	20

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V. RESULTS AND DISCUSSION

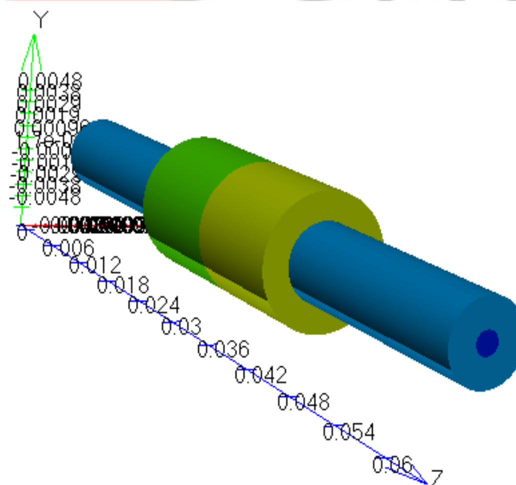

Fig 3 (a) DMG-CNTFET schematic structure

The response of the CNT-FET with the structure of the device simulated at atlas is shown in Fig. 3 (a). The simulation are done at room temperature (T=300k). It is followed by two characteristics I-V curves of the device which includes the transfer curve presented in Fig. 3 (b) and the output curves presented in Fig. 3 (c). In fig 3 (b) DMG-CNTFET output characteristics are shown. These output characteristics are obtained at V_{GS} = 1 V.

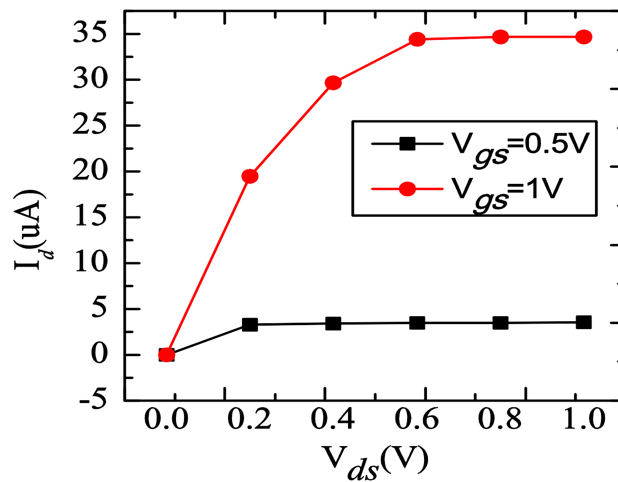

Fig 3(b) Output characteristics of DMG-CNTFET

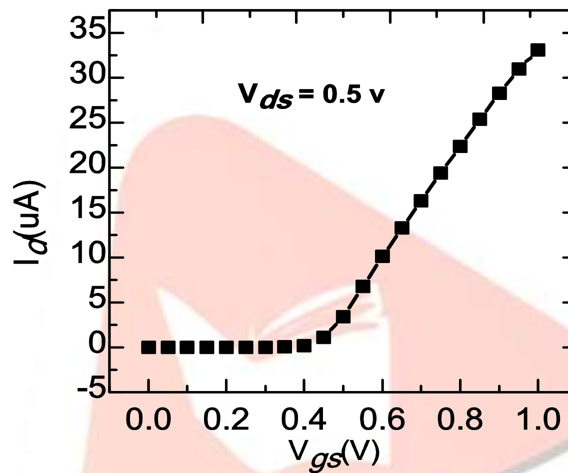

Fig. 3(C) Transfer characteristics of DMG-CNTFET at V_{DS}=0.5V

In fig 3 (c) transfer characteristics are shown. These characteristics are obtained for V_{DS} = 0.5 V.

In fig 4 comparison between output characteristics of conventional CNT-FET and DMG-CNTFET is shown. By comparing output characteristics of conventional CNT-FET and double metal gate CNT-FET it is observed that I_{on} of DMG-CNTFET is smaller than C-CNTFET. On the other hand I_{off} of the new structure is much lesser as compared to previous one. Thus ratio of on current to off current of DMG-CNTFET is much higher than C-CNTFET. We can see drop in conductance at drain for DMG-CNTFET, and rise in transconductance is obtained in case of DMG-CNTFET.

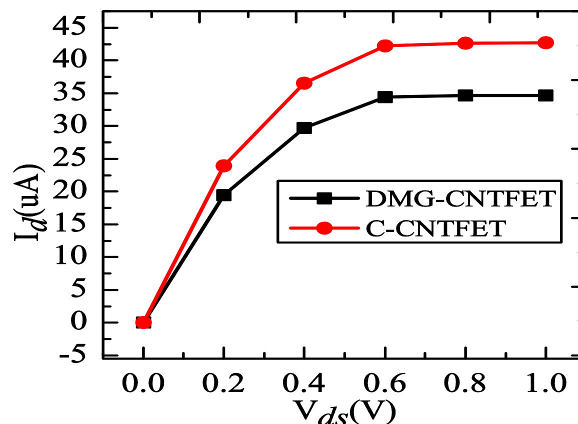

Fig 4. Comparison between output characteristics of DMG-CNTFET and C-CNTFET at V_{gs}=1V

VI. CONCLUSION

In this research paper the simulation of the DMG-CNTFET is done. This device is based on the double metal gate material having different work functions. We have been examined the DMG-CNTFET by developing the full quantum 2-D simulation. In this paper various comparisons between C-CNTFET and DMG-CNTFET have been made. There is a comparison of on currents, off currents and threshold voltages for same values of gate and source voltages. It is clear from the comparison plot that the DMG-CNTFET is better than C-CNTFET because of high on-off current ratio. There is considerable increase in voltage gain of DMG-CNTFET. Therefore for future CMOS circuit application DMG-CNTFET is a prime candidate.

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