DESIGN OF RIPPLE CARRY ADDER USINGQUANTUM-DOT CELLULAR AUTOMATA

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ABSTRACT: Quantum-Dot Cellular Automata (QCA) is an emerging nanotechnology, with the potential for faster speed, smaller size, and lower power consumption than transistor-based technology. The basic logic circuits of the system are inverter and majority gates. Quantum-Dot Cellular Automata has a simple cell as the basic element. The cell is used as a building block to constructgates and wires. These structures were designed with minimum number of cells by using cell minimization technique. This project utilizes the QCA characteristics to design the Ripplecarry adder. A Ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry-in of the succeeding next most significant full adder. Multiple full adder circuits can be cascaded in parallel to add an N-bit number. The layout of a ripple-carry adder is simple, which allows fast design time. The experimentation with the proposed designs have been successfully verified through the QCADesigner tool.

Keywords: Quantum dot cellular automata, Ripple carry adder, Majority gates, QCADesigner

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I.INTRODUCTION

Transistors cannot get much smaller than their current size once it is fabricated. The area and complexity are the major issues in circuit design. The quantum dot cellular automata can implement digital circuits with faster speed, smaller size and low power consumption, even though the design of logic modules in QCA is not always straightforward. Over several decades Quantum dot Cellular Automata has gained a lot of attention as it offers extremely low power, operation at very high frequency (usually in Tera-Hertz) and high density for implementing any digital logical circuit.

The main motivation of scaling is to provide high performance devices which can operate at very high frequency ranges usually in Tera-Hertz and have low power consumption. In QCA the information storing procedure is different, as position of electrons decide the logic states. Dr. Criag Lent first proposed this novel idea. In the QCA technology the primitive structure is a QCA cell. In this paradigm the QCA cell consists of four quantum dots at the four corners of a square geometry where mobile free electrons are pushed and are confined to any of two quantum dots at the opposite diagonals.

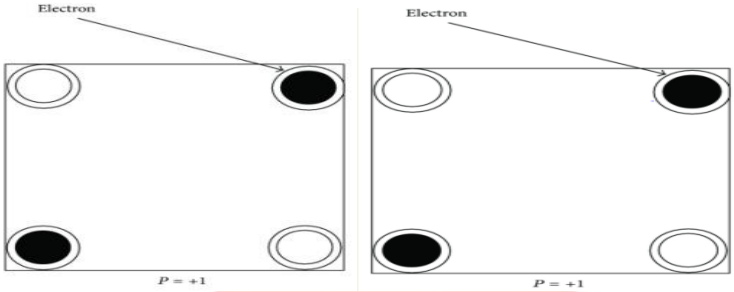
In QCA the dataflow from one point to another is accomplished by means of columbic interaction of the electrons of neighbouring cells. Polarization of one QCA cell affects the polarization of its neighbouring cells, therefore, a specific arrangement of QCA cells results in

desired implementation of a Boolean function.The basic logic circuits used in this technology are the inverter and the Majority Gate (MG), using this other logical circuits can be designed.

II.QCA TECHNOLOGY

1.BASIC QCA CELL

In contrast to electronics based on transistors, QCA does not operate by thetransport of electrons, but by the adjustment of electrons in a small limited area ofonly a few square nanometers. QCA is implemented by quadratic cells, the so-called QCA cells. In these squares, exactly four potential wells are located, one in each corner of the QCA cell. In the QCA cells, exactly two electrons are locked in. They can only reside in the potential wells. The potential wells areconnected with electron tunnel junctions. They can be opened for the electrons totravel through them under a particular condition, by a clock signal. Without any interaction from outside, the twoelectrons will try to separate from each other as far as possible, due to the Coulombforce that interacts between them. As a result, they will reside in diagonally locatedpotential wells, because the diagonal is the largest possible distance for them toreside.



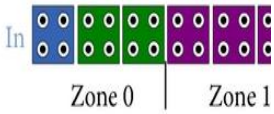
2.QCA LOGIC

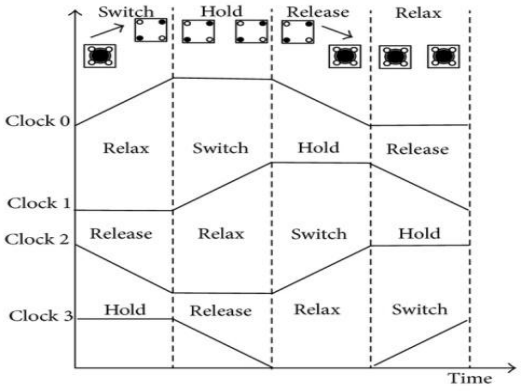
Coulombic forces will cause adjacent cells to interact. The state of thecells will always tend to the lowest energy. We can take advantage ofthis to transmit information through a "wire" by forcing the polarizationof a cell at one end.

3.QCA CLOCKING

Clock is one of the important features to control CMOS circuits. Similarly QCA circuit is also controlled by clock [1-5]. In order to control the potential barrier which exists when the electrons present in the quantum dots as they try to move along the tunnel junction and another barrier comes into play when switching occurs between the cells. In order to synchronize the flow of information, clocks are necessary. Four different clocking zones are present in QCA clocking

A) Switch phase- This phase give rise to polarization. Here initial starts of tunneling of electrons are held strongly due to obstruction caused by the polarization effect between the dots.



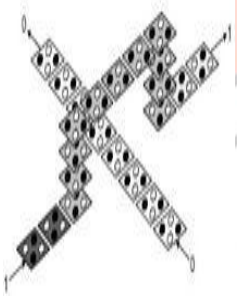


B) Hold phase-As the name of this phase depicts the electrons will be strongly held in their previous position within the cell as polarization remains same as achieved in the last phase.C)Release phase-In this phase QCA cell's polarization is lost and it is converted back into its normal un-polarized state. As a result the obstruction between dots is reduced and the electrons can move through dots.

D**)** Relax phase–The obstruction between the quantum dots remain as same as obtained in the release phase and therefore the cell's state remains same.

4.QCA CROSSOVER

In designing of QCA circuit sometime it requires to crossover a wire for interconnection of components. Mainly two types of crossover are available, one is multilayer and other is coplanar. In multilayer crossover, multiple layers are used for the interconnection of component. In coplanar crossover method, wire crossing is performed by two different types of cell. One wire has cells with 90^0 orientation Fig (a) and other wire has cells with 45^0 orientation Fig (b).



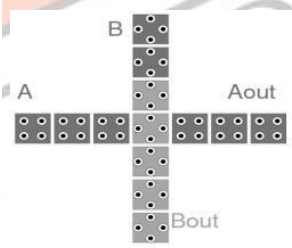


Fig (a) Fig (b)

III.EXISTING WORK

Various types of QCA devices were constructed using different physical cell arrangements. QCA inverter can be implemented by positioning and rotation of cells. In our implementation, positioning of QCA cell is used to invert the output from input logic level. In the two cell inverter, the first cell is placed normally and the second cell is placed adjacent to the first cell, but 10nm vertically below from the cell. Here the electrostatic interaction is inverted because the quantum dots of different polarizations are misaligned between the cells. The AND and OR gates are realized by fixing the polarization to one of the inputs of the majority gate to either P = −1

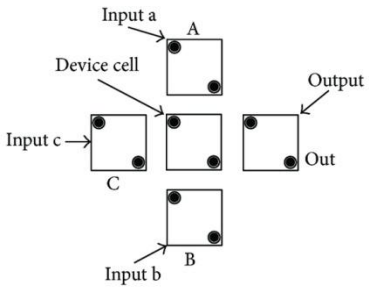
(logic "0") or P = 1(logic "1"). Arithmetic circuits with less number of cells count have been designed using efficient XOR gate ,and it saves the area of occupation on the chip. efficient adders and subtractors were designed by Integrating those efficient xor gate structures. It achieves speed performances higher than all the existing QCA adders. Those designs proved to be efficient in term of parameters like cell count, cell area, total area and latency and the complexity. The QCADesigner 2.0.3 were used to carry out the simulations with cell size of 18x18 nm, cell spacing of 2nm, Dot diameter of 5nm, 12800 number of samples, and radius effect f 65.000000 nm.

IV.PROPOSED WORK:

This project deals with designing Ripple carry adder circuit using Quantum-Dot Cellular Automata. This design composed of MAJORITY gates to implement thelogic structure. Ripple carry adder can be designed by integrating the fulladders.The advantage of using this QCA technology, reduces the size, increases the execution speed with a considerable power consumption.

A.MAJORITY GATES

The basic QCA gate is 3-input majority gate. In it QCA cell is used as a basic building block. The 3- input majority gate can be made by using 5 QCA cells arranged in two different ways.



In 3 input majority gate 3 cell will work as input cells, now the centre cell will be affected by the sum of the coulomb forces of 3 input cells, so the centre cell's electrons adjustment will be the majority of the adjustment of 3 input cells. Finally the 5^{th} cell will give the output according to centre cell adjustment. So expression of three input majority gate can be given by (1).

$$M_3(A,B,C)=AB+BC+CA \quad ...(1)$$

By using three input majority gate we can make AND & OR gate by taking one input as '0' or '1' as in (2) and (3).

$$A.B=M_3(A,B,0) \quad ...(2)$$

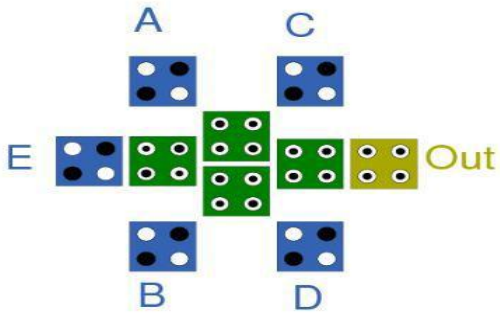
$$A+B=M_3(A,B,1) \quad ...(3)$$

A NOT gate can also be made by QCA cells by inverting the position of electrons in QCA cell , so that input logic '0' will result as output '1' and input logic '1 will result as output '0'

Researchers have designed 5-input majority gate based QCA circuits. These are more efficient in terms of area and faster than the previous designs. Some of the 5-input majority gate structures have been presented. The logic function of 5-input majority voter can be expressed below,

$$M_5(A,B,C,D,E)=ABC+ABD+ABE+ACD+ACE+ADE+BCD+BCE+BDE+CDE$$

The new proposed 5-input majority gate structure is shown in Fig below.

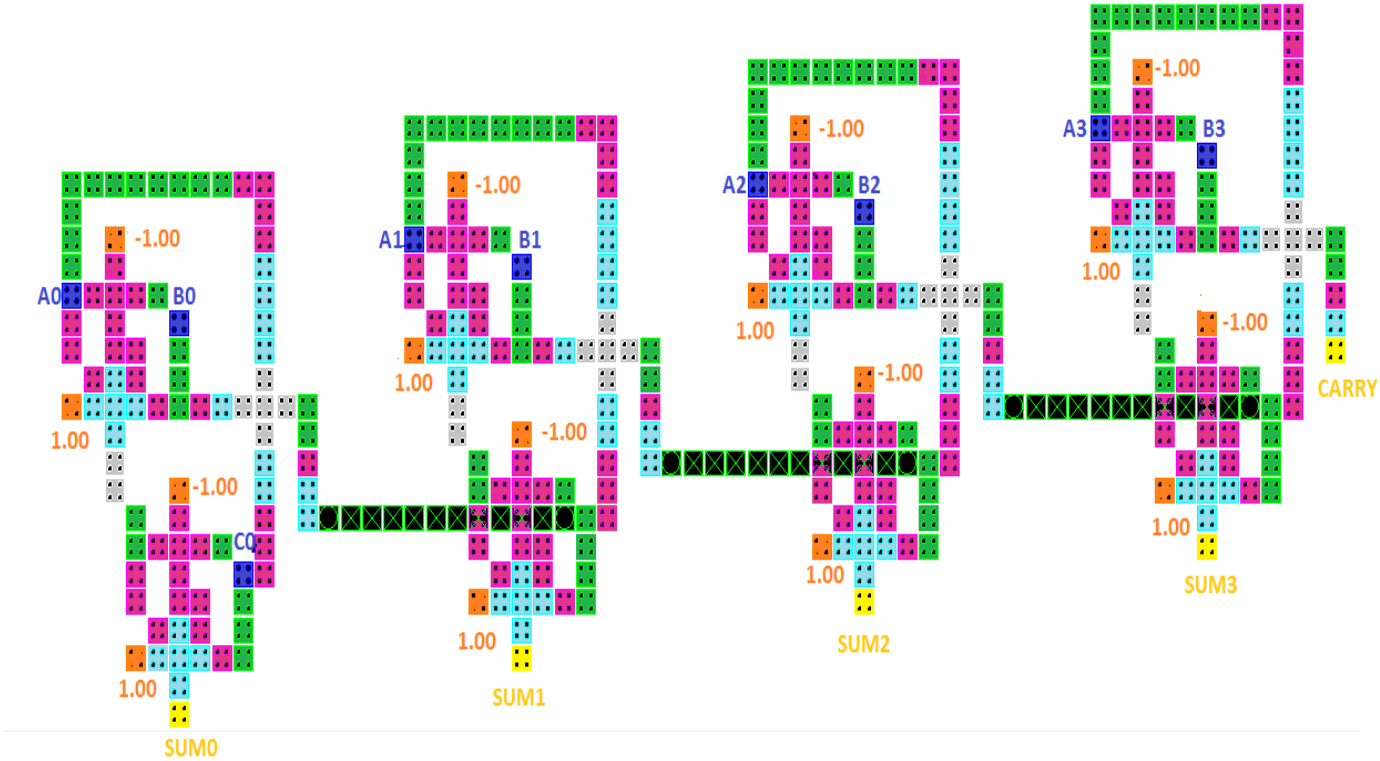


Where A, B, C, D, E are 5 inputs and output cell is indicated by 'OUT'. Remaining medium cells are device cells which aggregate the coulombic forces of all input cells and drive it to the output cell.

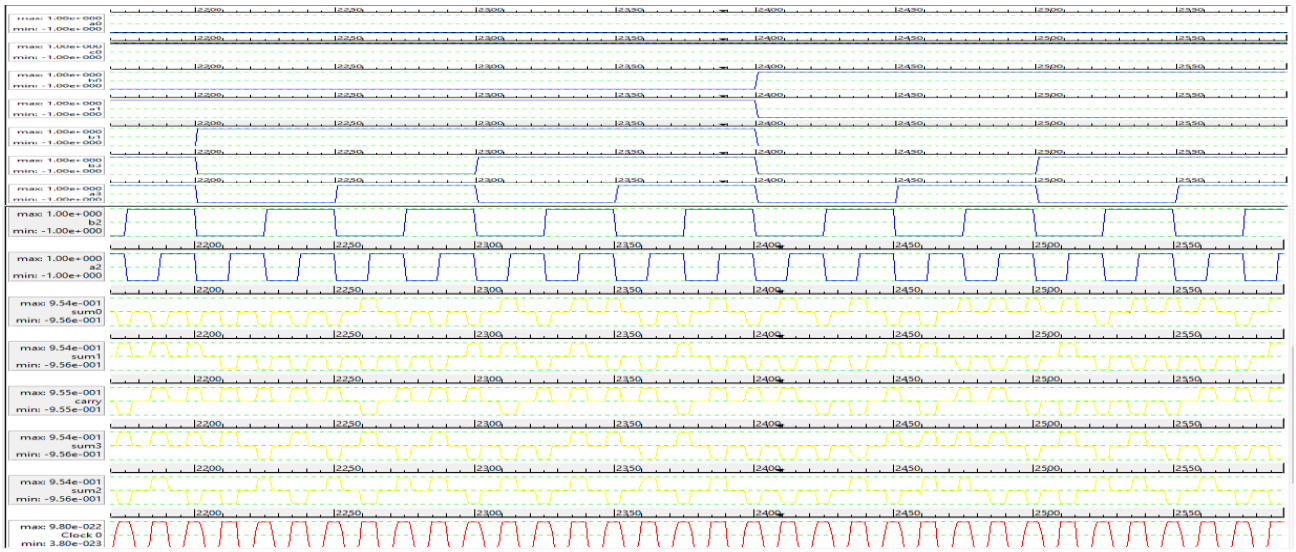
B.RIPPLE CARRY ADDER

It is possible to create a logical circuit using multiple full adders to add *N*-bit numbers. Each full adder inputs a *C*in, which is the *C*out of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder (under the assumption that *C*in = 0). The layout of a ripple-carry adder is simple, which allows fast design time utilizing efficient five input majority gates; however, the ripple-carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit.

- **QCA DESIGN OF RIPPLE CARRY ADDER**



- **SIMULATION RESULT**



V.CONCLUSION

During course of the project much progress has been made on basic logic gates and tested using QCADesigner software. The operation of circuits has been verified using truth table. The basics circuits such as adders, half adders, full adders, subtractor, half subtractor, full subtractor were studied, implemented and verified using QCADesigner. Further using this basic circuits, work has been done and ripple carry adder is designed and output has verified. In this work the design of ripple carry adder uses only less number of gates which reduces the sizes. And this also reduces the power consumption and increase the speed comparing to the CMOS technology.

VI.FUTURE WORK

Planned improvement for future work includes design of multipliers using basic adders and subtractor circuits. Work regarding clocking for stimulation of multipliers circuits has been in progress. And design of various types of multipliers circuits can be designed and implemented from this work. This work can be used to achieve various advantages and development in QCA technology. Further research work can be in this project in future to bring progressive development in VLSI.

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