DESIGN OF SCHMITT TRIGGER USING FINFET

Arul Selvi.V[1],Divya.A[2], Krithiga.K.R[3], Rajat Kumar Dwibedi[4]

[1,2&3]Students of B.E, Department of Electronics and Communication Engineering,
Jeppiaar SRR Engineering college, Chennai.
Assistant professor[4], Department of Electronics and Communication Engineering,
Jeppiaar SRR Engineering college, Chennai.

Abstract: The leakage power dissipation has become each of the foremost dominant factors in total power consumption and nonetheless a challenge for the VLSI designers because it doubles every year in keeping with Moore‟s law, leakage power consumption might dominate total power consumption. As leakage current goes to be a limiting issue for consecutive thinning out of transistors. Owing to the smaller feature sizes in nm technologies, shorter channel lengths cause sub threshold current to extend once the semiconductor device is within the off state. The lower sub threshold voltage offers rise to magnified sub threshold current furthermore, as a result of transistors cannot be converted fully. In order to reduce the leakage current we apply the FINFET technology with MTCMOS technique. During this paper, we tend to propose a brand new leakage reduction technique, named “Dual sleep techniques”, “Variable body biasing” which might be applied to general logic circuits furthermore as memory.

Index Terms: MTCMOS, FINFET, Schmitt trigger, power gating techniques, sleep transistor.

I.INTRODUCTION

With each technology generation as the device dimension is scaled down the complexity And performance estimation of the VLSI ICs is increases. The present scaling scenario exploits the fact that at sub-nanometer leakage of current in standby mode will become a major limiting factor to present available technologies. Idle circuit Metal Oxide Semiconductor (MOS) devices will not able to properly turn-off, as a result of which “off-state current” will flow through the circuit. So FinFET has advantage over CMOS.

II.SINGLE GATE MOSFET

The silicon metal oxide semiconductor field effect transistor (MOSFET) is one of the major and vital components in the semiconductor world. Since its first practical use 50 years ago, the MOSFET has a vital use in integrated circuits (ICs) to serve as a basic operating device in switching functions for digital circuits and as an amplifier device for analog applications. While the basic planar structure of the MOSFET has remained mostly unchanged, its size has been shrunk by many orders of magnitude over the past thirty years. The trend showing an exponentially increasing number of transistors on a chip was first predicted in 1965 and has since come to be known as „Moore‟s Law‟ shows a plot of the minimum feature size in the

MOSFET, the gate length, over time. The main driving forces behind gate length scaling are the higher switching speed and packing density that result from making the transistors smaller.

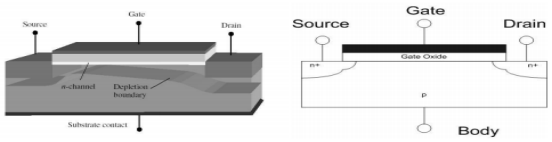


Figure 1. structure of bulk MOSFET

III.FINFET TECHNOLOGY

Complementary Metal Oxide Semiconductor (CMOS) Technology is facing enormous challenges to channel length below 90nm, such as Gate leakage current, under the threshold leakage current and drain induced lowering of the barrier (DIBL) current, any FinFETs overcome these problems in the CMOS. It is clear that the future of the technology of materials should show greater mobility, greater stability, and the scalability against the process and reduces the effects of variations of short channel effects. Due to the scaling of deep submicron processes in the memory, the variations in temperature, power supply voltage and the variations of the process put the most important challenges for the future of the design of the memory and the high-performance device. At this time, it has been proposed to replace the CMOS transistors in the SRAM with FinFET.

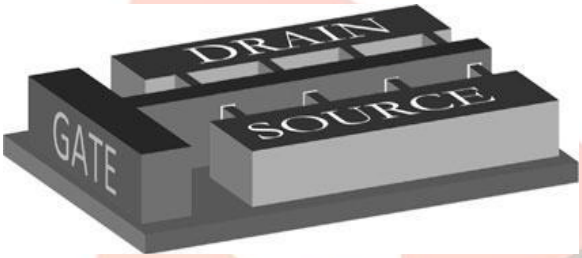


Figure 2. Multi-fin FinFET

Threshold of the inverter depends upon the pull-up and pull-down ratio of the transistors.

IV.EXISTING SYSTEM

Schmitt Trigger:

Schmitt trigger is a bi-stable networks that square measure wide used to enhance the Immunity of a circuit to noise and disturbances. It‟s smart as a noise rejecter. Schmitt trigger make use of waves, so it's wide used for changing analog signals into digital ones and to reshape sloppy, or distorted rectangular pulses. Physical phenomenon of the trigger eliminates noise creating a cleaner and additional reliable signal. The output of a Schmitt trigger changes state once a positive going input passes the higher trigger purpose (UTP) voltage and when negative going input passes the lower trigger purpose voltage.

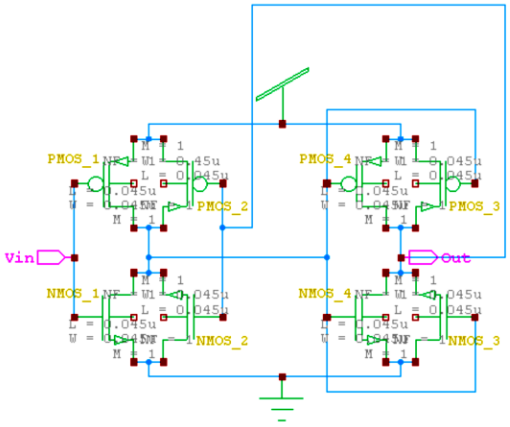


Figure 3.Schmitt Trigger Circuit design

Schmitt Trigger Circuit design using FINFET and MTCMOS technology:

Double gate FINFET technique is applied on Schmitt Trigger Circuit. Here self-determining management of front and back gate in decigram FINFET will be expeditiously wont to develop performance and scale back power consumption. In non-critical ways self-determining gate management will be wont to be a part of along parallel transistors. A parallel semiconductor device try consists of 2 transistors with their supply and drain terminals tied along. The second gate is side opposite to the standard gate in Double-Gate (DG) FINFETS, that has been certain for his or her prospective to superior management short channel effects, additionally on management discharge current. The operations of FINFET is recognized as short gate (SG) mode with semiconductor device gates connected along, the freelance gate (IG) mode wherever self-determining digital signals ar wont to drive the 2 device gates, the low power and optimum power mode wherever the rear gate is connected to a reverse-bias voltage to cut back discharge power and therefore the hybrid mode, that employs a arrangement of low power and self-determining gate modes.

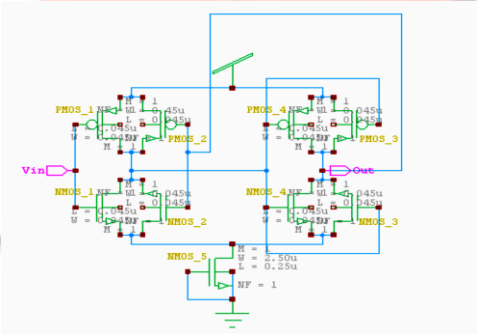


Figure 4.MTCMOS technology

V.PROPOSED SYSTEM
DUAL SLEEP TECHNIQUE:

Dual sleep Technique uses the advantage of using the two extra pull-up & pull-down transistors in sleep mode either in OFF/ON state. To all logic circuitry the dual sleep portion is designed as common. For a certain logic circuit less number of transistors are enough to apply.

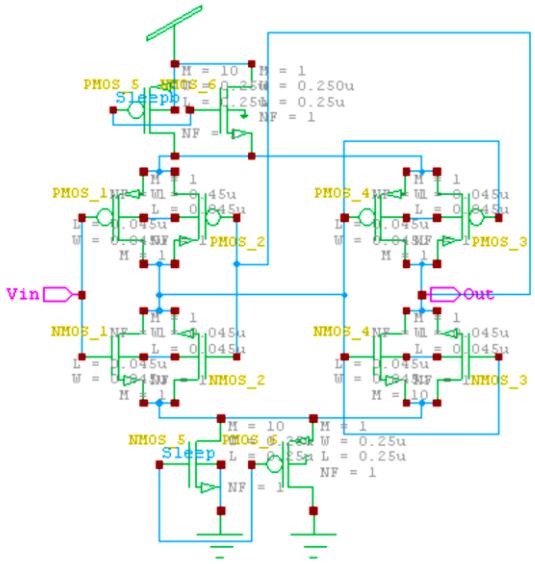


Figure 5.Dual sleep technique

VARIABLE BODY BIASING:

This is another new leakage reduction technique, which we call the "Variable Body Biasing" technique. This technique in figure 6 uses two parallel connected sleep transistors in Vdd and two parallel connected sleep transistors in GND. The source of one of the pMOS sleep transistor is connected to the body of other pMOS sleep transistor for having so called body biasing effect. Similarly the source of one of the nMOS sleep transistor is connected to the body of other nMOS sleep transistor for having the same effect as for pMOS sleep transistors. So, leakage reduction in this technique occurs in two ways. Firstly, the sleep transistor effect and secondly, the Variable Body Biasing effect. It is well known that pMOS transistors are not efficient at passing GND; similarly, it is well known that nMOS transistors are not efficient at passing Vdd. But this Variable Body Biasing technique uses pMOS transistor in GND and nMOS transistor in Vdd, both are in paralleled to the sleep transistors, for maintaining exact logic state during sleep mode.

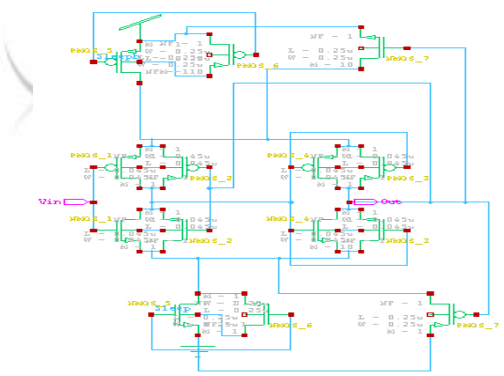


Figure 6.variable body biasing technique

VI. SOFTWARE TOOLS

Tanner Software:

Today"s semiconductors and electronic systems are complex that designing them would be impossible without electronic design automation (EDA). This primer provides a comprehensive overview of the electronic design process, and then describes how design teams use Cadence tools to create the best possible design in the least amount of the time.

Tanner EDA Design Tools:

- S-edit - a schematic capture tool
- T-SPICE - the SPICE simulation engine integrated with S-edit
- W-edit - waveform formatting

S-EDIT:

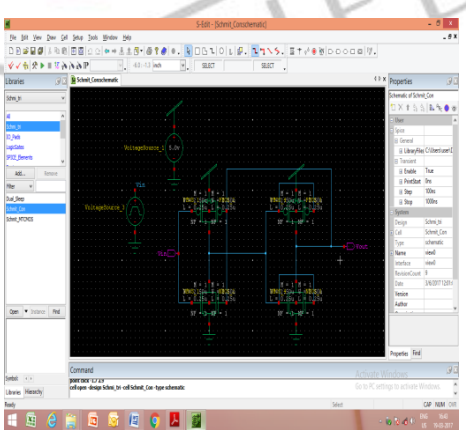
- S-Edit is a powerful design capture & entry tool that can generate netlists directly usable in T-Spice simulations.
- Provides an integrated environment for editing circuits, setting up and running simulations and probing the results.
- It also provides the ability to perform SPICE simulations of the circuit
- These circuits that can be driven forward into a physical layout.

T-SPICE:

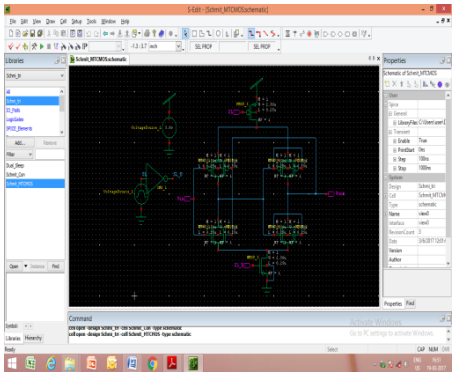
- The role of T-Spice is to help design and verify a circuit"s operation.
- T-Spice simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication.

7. RESULTS AND ANALYSIS

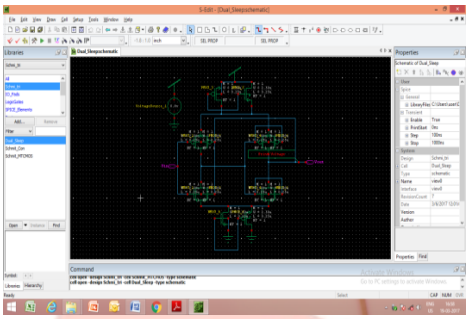
A. DESIGN OF SCHMITT TRIGGER CIRCUIT IN S-EDIT.



B.DESIGN OF MTCMOS SCHMITT TRIGGER CIRCUIT



C.DESIGN OF DUAL SLEEP SCHMITT TRIGGER CIRCUIT



D.DESIGN OF VARIABLE BODY BIAS SCHMITT TRIGGER CIRCUIT

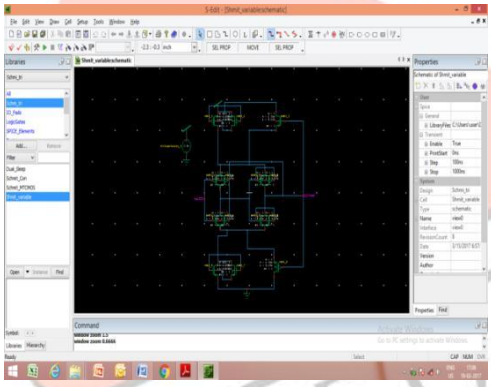


TABLE 1: In the below table we show the comparison result of power consumptions for each circuit

CIRCUITS	POWER CONSUMPTION
Schmitt trigger	6.649718e-003
MTCMOS	5.860874e-006
Dual Sleep	1.153564e-006
Variable body bias	8.394071e-008

VIII. CONCLUSION

We have concluded that power is reduced by two techniques. In existing system, we have obtained a power with some range. And in proposed method, there is a change in power reduction. We have analyzed a Sleep Transistor Approach and MTCMOS schemes to reduce the leakage current in FinFET based Schmitt trigger. These power gating techniques offers reduced standby leakage, without any effect on the system performance. These power gating techniques are most promising for lower VDD operation in FinFET technologies. Implementation based on MTCMOS techniques has been proposed to get faster speed with low power voltage supply. Also by using Dual Sleep transistor method and Variable body biasing method we can get high threshold voltage that is applied to the circuit and power consumption will be reduced. On comparing the existing method, the power consumption will be reduced more in the proposed method.

IX. REFERENCES

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