FPGA Based Vedic Multiplier

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Abstract:

FIR filters, Microprocessors, DSP and communication application Multipliers are used. To carry higher order multiplication number of adders and compressor required are more to carry out partial product addition. As the need of high speed processor are increasing the need of low power high speed multiplier is also increasing. In this paper, a high performance, high throughput and area efficient architecture of a multiplier for the Field Programmable Gate Array (FPGAs) is proposed. The multiplier is design using vertical and crosswise structure of ancient Indian Vedic multiplier. As per the proposed architecture, for two 4-bit numbers; the multiplier and multiplicand, each are grouped as 2-bit numbers so that it decomposes into 2×2 multiplication modules. The coding is done in VHDL and the FPGA synthesis is done using Xilinx.

Keywords: **FPGA, Multiplier, Vedic Mathematics**

I. INTRODUCTION

In different computing application role of multipliers is very crucial. To obtain the design targets like high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI implementation many researchers are trying to design multiplier. High processing speed resulting in fast arithmetic operation is today's need for many real time and image processing applications. In the below sections, the hardware architecture of 2 x 2 and 4 x 4 Vedic multiplier are displayed. Vertical and crosswise excluding all other arithmetic operations, multiplication is one of the important operations and hence development of fast multiplier circuit has been an area of research over decades. Using techniques of Vedic mathematics focus is mainly given on reducing time delay of signed multiplier. Ancient Indian Vedic Mathematics consists of sixteen mathematical formulae originated from the Atharvaveda. The arithmetic operations like multiplication, division, square root, and cubing, squaring and finding cube root are time consuming processes for machine as well as man sixteen principles or word formulae which are referred as sutras are used Vedic mathematics for fast and easy solution of different time consuming process. This is a very interesting field and presents some effective algorithms which can be applied to various branches of Engineering. The primary motivation is to reduce the delay.Maintaining the Integrity of the Specifications. For software part we are using VHDL language. VHDL stands for VHSIC Hardware Description Language and VHSIC stands for Very High Speed Integrated Circuits. VHDL is being used for documentation, verification, and synthesis of large digital designs. This key feature of the VHDL saves a lot of design effort, since the same VHDL code can theoretically achieve all three goals. In this work VHDL is used because of its portability, flexibility, and readability [1].

II. VEDIC MATHEMATICS

The ancient Vedic Mathematics was rediscovered by
Swami Bharati Krisna Tirthaji (the former Shankaracharya of Puri, India) in 1911 [1]. Due to this phenomenal characteristic, Vedic mathematics has become a wide topic of research in abroad. Entire mechanics of Vedic mathematics is based on 16 sutras and 13 up-sutras meaning corollaries which are enlisted

These are the 16 basic sutra of Vedic mathematic: [3]

1) (Anurupye) Sunyamanyat -If one is in ratio, the other is zero.
2) ChalanaKalanabyham -Differences and similarities.
3) Ekadhikena Purvena- By one more than the previous One.
4) Ekanyunena Purvena - By one less than the previous one.
5) Gunaksamucchayah-Factors of the sum is equal to the sum of factors.
6) Ginitasamucchayah-The product of sum is equal to sum of the product.
7) Nikhilam Navatascharamam Dashatah -All from 9 and last from 10.
8) Paravartya Yojayet-Transpose and adjust.
9) Puranaprranabhyam - By the completion noncompeting.
10) Sankalana-vyavakalanabhyam -By addition and by subtraction.
11) Sheshanynkena Charmena- The remainders by the last digit.
12) Shunyam Samyasamucchaye -When the sum is same then sum is zero.
13) Sopantyadvayamantyam -The ultimate and twice the penultimate.
14) Urdhva-tiryagbhyam -Vertically and crosswise.
15) Vyashtisamanstih -Part and Whole.
16) Yavadunam- Whatever the extent of its deficiency.

Vedic mathematics reduces the otherwise cumbersome looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works.

III. PROPOSED MULTIPLIER DESIGN

2 bit Vedic multiplier module:

The method is used for two, 2 bit numbers A and B Where A=a1a0 and B=b1b0 as shown in Fig 1.first the LSB are multiplied which gives final product of least significant bit (Vertical).The Least significant bit of multiplicand is multiplied with next higher bit of multiplier and added with product of least significant bit of multiplier and multiplicand of next higher bit (multiplicand).The sum gives the final product of second bit and carry is added with partial product obtained. The third corresponding bit is sum and fourth bit of final product is carry. [2]

$$s0=a0b0; \quad (1)$$

$$c1s1=a1b0+a0b1; \quad (2)$$

$$c2s2=c1+a1b1; \quad (3)$$

The final product is c2s2s1s0.This method of multiplication is applicable to all types.

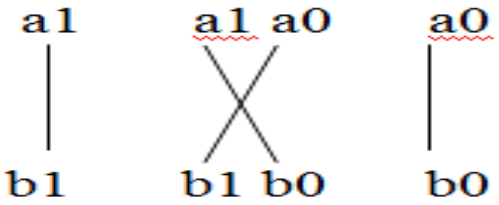

Figure 1: The Vedic Multiplication method for two 2-bit binary numbers

The implementation of 2 bit Vedic multiplier module consists of four input AND gates and two half adders which is shown in Fig 2.The architecture of 2 bit Vedic multiplier is same as the architecture of 2 bit array multiplier. In 2bit Vedic multiplier, the total delay is only 2- half adder delays are same as the array multiplier. So we move on to the implementation of 4x4 bit Vedic multiplier which is having 2x2 bit multiplier as basic building block.

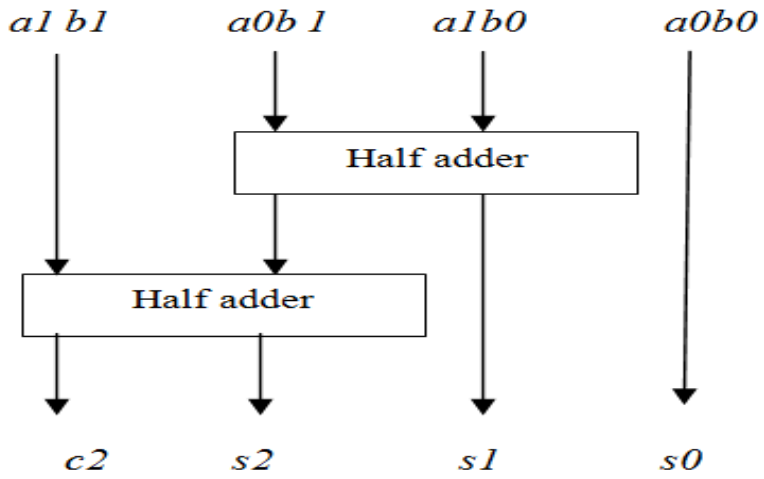

Figure 2:2x2 Vedic multiplier

4 bit Vedic multiplier module.

Analyse the 4x4 multiplication by using A=A3A2A1A0

And B=B3B2B1B0. The final result is S7S6S5S4S3S2S1S0. Divide A and B into two parts, say A3A2 & A1A0 for A and B3B2 & B1B0 for B. [2]

A3A2 A1A0 multiplicand
B3B2 B1B0 multiplier

A3 A2	A3 A2	A1 A0	A1 A0
X	X	X	X
B3 B2	B1 B0	B1 B0	B3 B2

Figure 3: The Vedic Multiplication method for two 4-bit binary numbers

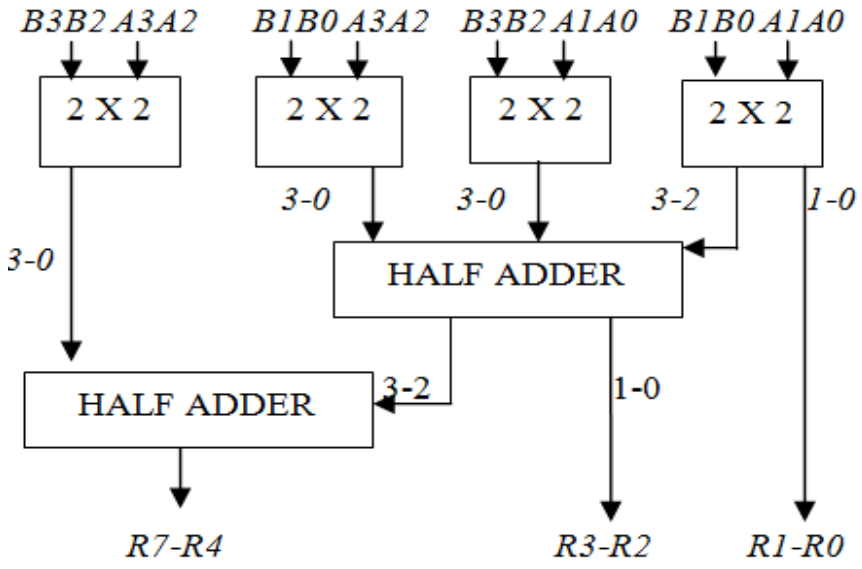

Figure 4: 4x4 Vedic multiplier

IV. LINE DAIGRAM AND ALGORITHM

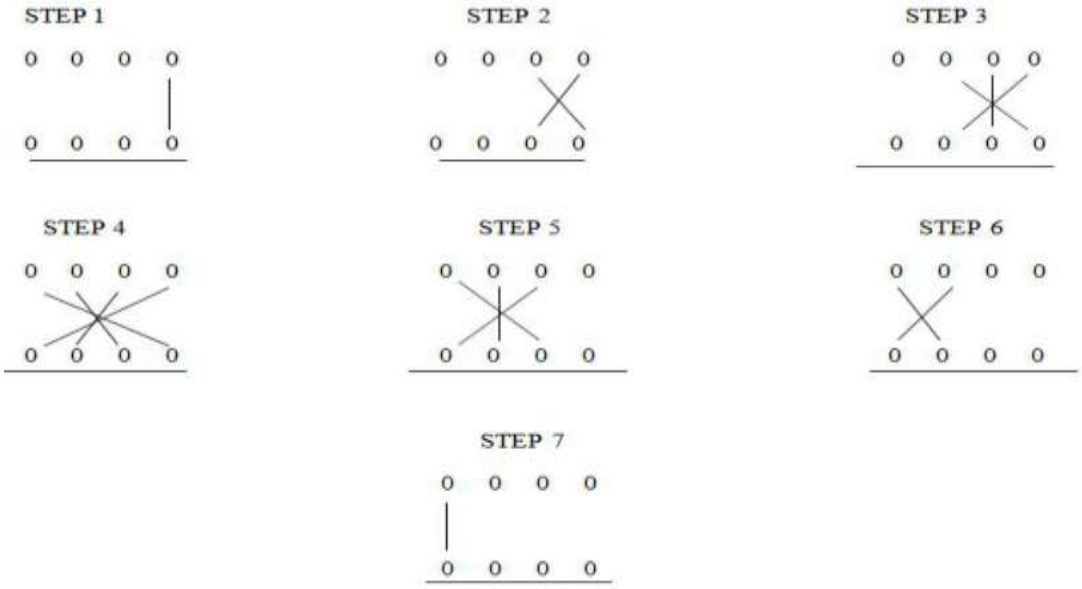

Figure 5: Line diagram

1. Least significant bits are multiplied which gives the least significant bit of the product (vertical)
2. .LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position.
3. All the four bits are processed with crosswise multiplication and addition to give the sum and carry.
4. The same operation continues until the multiplication of two MSBs to give the MSB of the product

V. SIMULATION RESULTS

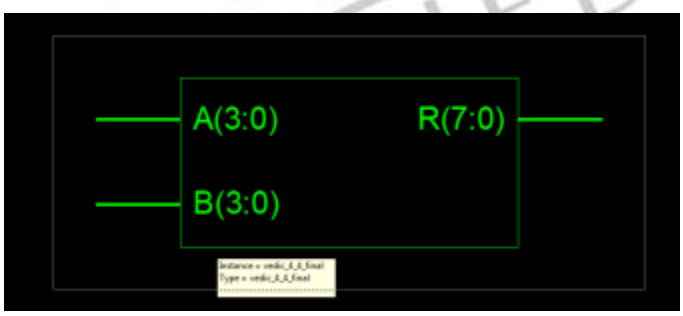

Figure 6: RTL SCHEMATIC

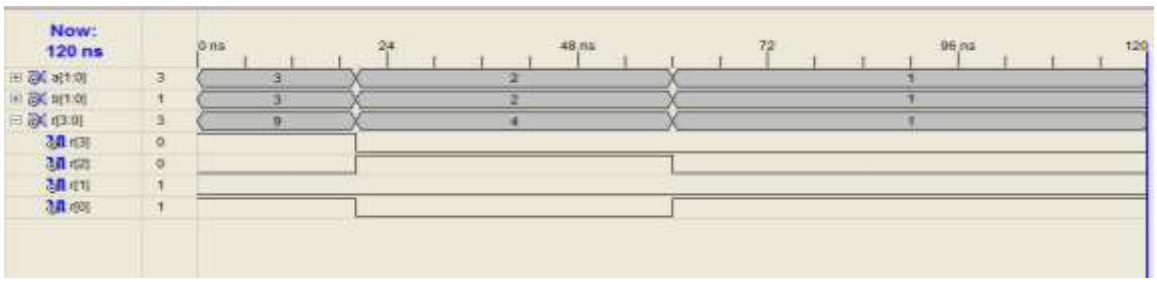

Figure 7: Result for 2 × 2 bit Multiplier

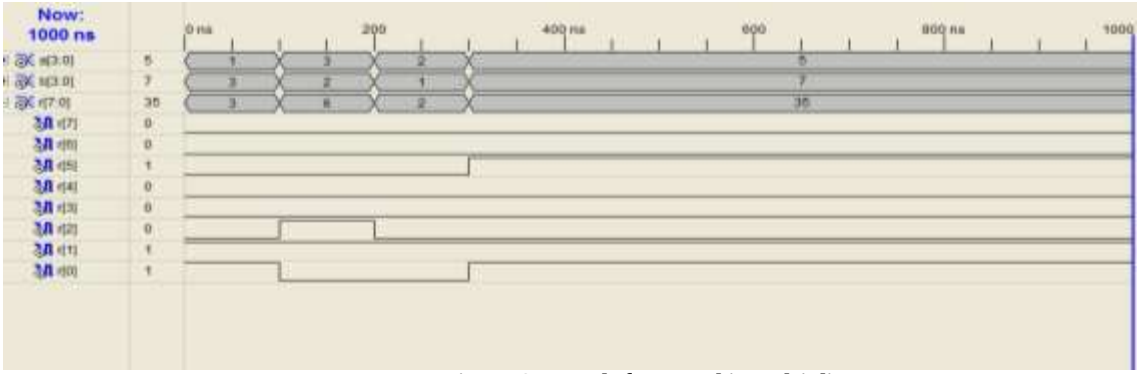

Figure 8: Result for 4 × 4 bit Multiplier

VI. CONCLUSION

In this work, using techniques of Vedic mathematics Vedic multiplier is designed efficiently. A 4 bit multiplier is design using 4 2 bit adders. Also the FPGA implementation of proposed work is done on Spartan-6 and result is displayed on LCD of Spartan-6 board.

VII. REFERENCES

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