A 32 Bitmac Unit Design Using DADDA Mutliplier and Reversible Logic (DKG) Gate

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Abstract— In digital signal processing, the multiply–accumulate is the common and most important operation as it is used in number of computations. Multiplier–accumulator (MAC unit) is the hardware unit which performs this operation. Multiply-Accumulate (MAC) unit has it's major applications in MP, logic units and digital signal processors, as it is the unit which determines the delay of the overall system. MAC units are involved in designs such as Computation which are Nonlinear like FFT/IFFT, Discrete Cosine or wavelet Transform (DCT). A Large variety of techniques have been developed in algorithmic and structural levels to intensify the efficiency of the multiplier which is achieved by reducing the partial products and the approaches used in their addition. Multiply Accumulate (MAC) unit are used in developing for various high performance application. So, for reducing the power and area constraints the MAC unit will be implemented by using DADDA Multiplier algorithm. For this XILINX ISE 14.1 tool is used.

Index Terms— MAC unit, DADDA Multiplier, Vedic Multiplier, Reversible logic gates, Kogge stone Adder.

I. INTRODUCTION

In general MAC architecture[8] consists of a multiplier, adder and an accumulator ,where the output of the multiplier will be summed to the already existing accumulator result by the means of adder. Microprocessors also uses this MAC unit massively. In DSP applications like FFT/IFFT there will be repetitive use of multipliers and adders. The capability of the entire computation mainly depends on the delay of the adder and multiplier stages. Among the operational blocks in digital system, multiplier exhibits considerably large delay, so multiplier plays very dominant part in the achievements of the any functional block.

For further improvement of performance parameters of the MAC unit such as power, area and speed, several ways has been existed in the design of the MAC unit by making use of numerous verities of multipliers in order to gain improvement in performance parameters.

The main key to the proposed architecture is to develop the MAC unit by replacing the normal or conventional multiplier by DADDA multiplier and using reversible logic in the adder. In VLSI models, fast switching of signals leads to large power dissipation ,here the information lost will dissipate in the form of heat i.e $kT*\log_2$ joules[1] .Here k is the Boltzmann's constant and the absolute temperature at which mathematical operations are performed. To reduce this dissipation of power here reversible logic[6]will be applied and the performance parameters will be considered with respect to different existing MAC units.

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II. DIFFERENT EXISTING METHODS

Different MAC units has been developed using wide varieties of Multipliers and Adders .Some of them are conventional multiplier like binary multiplier ,BOOTH multiplier and VEDIC multiplier etc..

1. MAC UNIT using Conventional(BINARY) Multiplier

MAC unit is developed by using conventional (Binary) Multiplier and Carry Ripple Adder. Due to its regular structure general multiplier is also known as Array multiplier . Multiplier circuit is normally depends on add and shift algorithm. Partial product term will be obtained by multiplying each bit of multiplier with multiplicand.

The MAC unit[1] is generally represented as below

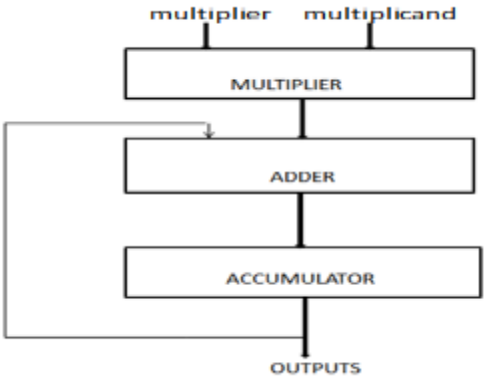
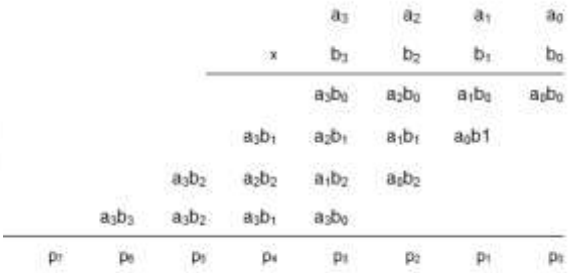


Fig 1: Basic block diagram of MAC unit

The partial product terms are shifted as per the order of the bits and then finally the addition operation will be performed. The normal carry propagate adder is used for performing the addition operation . Here the number of adders required will be N-1. Where the multiplier length is denoted by N.

In general multiplication of two numbers is explained as below



Then the partial products generated are summed with the Accumulator result with the help of Adder. In the Array multiplier the propogation of carry can be achieved by the means of carry ripple Adder. This type of multiplication involves in more partial products generation which in turn consume more time , power, Area so to enhance this some more methods has been evolved .

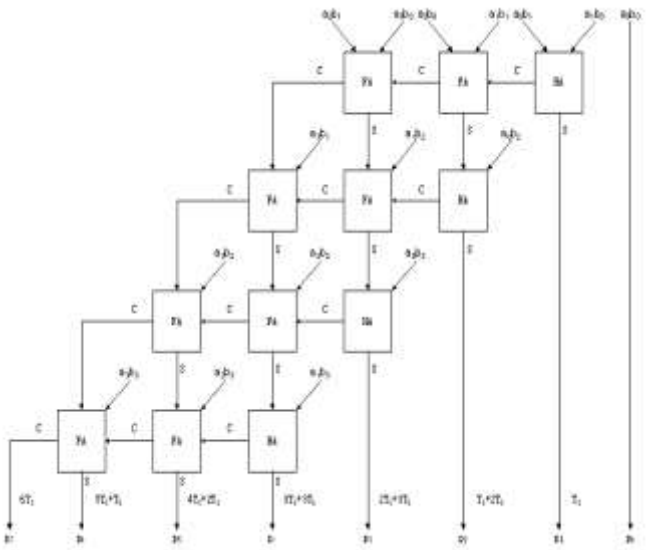


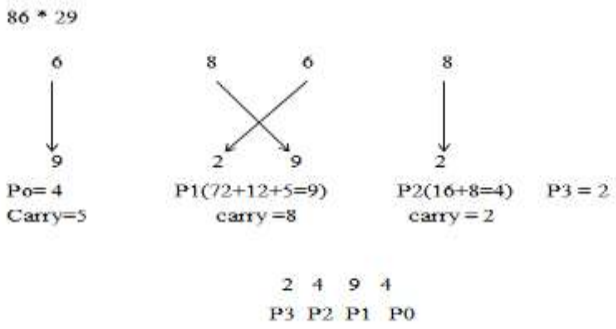
Fig 2: Multiplier implemented with full adders

2. MAC UNIT IMPLEMENTED WITH VEDIC (URDHVA TIRYAKBHAYAM SUTRA)MULTIPLICATION TECHNIQUE

DSP applications require MAC unit which consumes less power and also which would perform faster calculations when compared to MAC Units designed by various earlier Multipliers and Adders.In favor to improve the parameters when compared to earlier ones, here the MAC Unit was designed by VEDIC Method .VEDIC Multiplication [4]was formulated by sri Jagadguru Swami Bharati Krishna Tirthaji (1884 - 1960) .He developed sixteen sutra's from Atharvarna veda . Out of those sixteen sutra's URDHVA TIRYAKBHYAM and NIKHILAM[4] are used for Multiplication purpose .Here the MAC Unit is designed using VEDIC Multiplier which uses URDHVA TIRYAKBHAYAM sutra .

URDHVA TIRYAKBHAYAM SUTRA

Urdhva Tiryakbhayam sutra generally means vertically and crosswise. In this the partial product calculation would become easier as no shift operation is required. An example for Urdhva Tiryakbhyam sutra[1] is explained as follows:



Here kogge stone adder[8] is used for addition purpose in the multiplier which is faster when compared to ripple carry adder[1] and carry skip adder[1] .Due to the reduction of partial product terms the consumption of power would also be reduced.

Here reversible logic gate as the adder in order to reduce the dissipation of power in the MAC unit. While designing the Reversible logic[6] circuit the following aspects should be well observed .

- Fan_outs are not allowed in Reversible logic circuits.
- In Reversible logic circuits Quantum cost should be minimum.
- This Reversible logic gate must have least possible number of constant inputs.
- Reversible logic designs should be simple such that it can generate least number of Garbage outputs.
- Logical depth in Reversible logic must be minimum .

Here DKG gate is used as a reversible logic gate[6] which is 4*4 gate .The same DKG gate can be used as both Full Adder or Full Subtractor . If A=1 it acts as Full adder ,if it is 0 then it acts as subtractor . This is represented as :

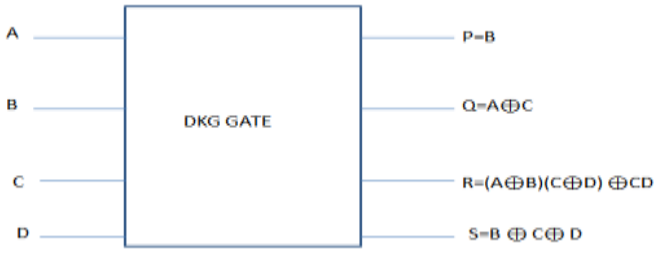
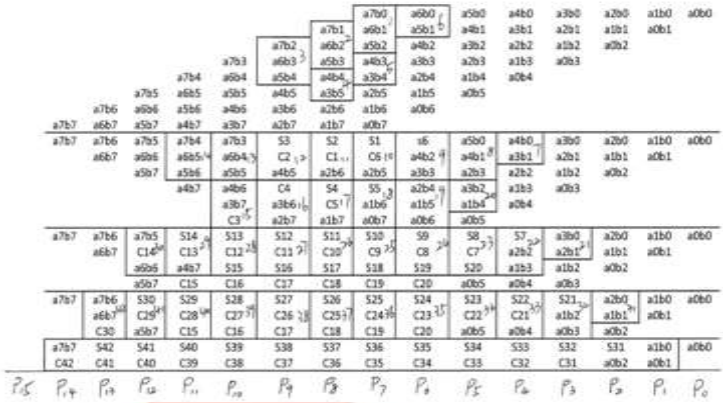


Fig 3: Reversible logic gate

III. PROPOSED METHOD

Although vedic multiplier by using Urdhva Tiryakbhyam sutra[1] is faster but it would create confusion for complex multiplication and the Nikhilam method[4] would absorb large power when compared to conventional Multiplier. So, the approach proposed deals with the MAC unit which will be developed by the help of DADDA Multiplier which would consume less power ,area and also which would perform calculations at a moderate rate. An example of 8 bit DADDA Multiplier.



Here the 32 bit MAC unit is designed by using DADDA Multiplier , final stage of the Multiplier is added with the help of skalansky adder and the adder of the MAC unit is implemented by Reversible logic gate .

IV . RESULTS

The MAC unit using Conventional Multiplier (Binary multiplier) and Vedic Multiplier ,DADDA Multiplier were designed .Their simulation results and comparison is shown below :

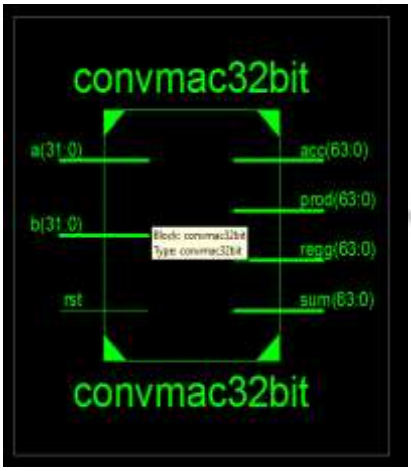


Fig 4: RTL of MAC using conventional (Binary) Multiplier

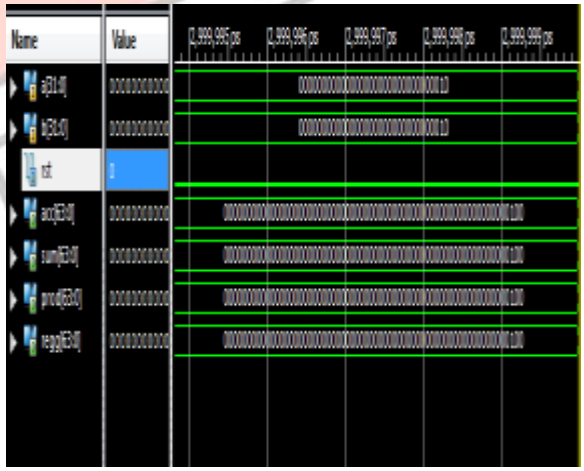


Fig 5: simulation waveforms of 32 bit MAC unit using conventional(binary) Multiplier

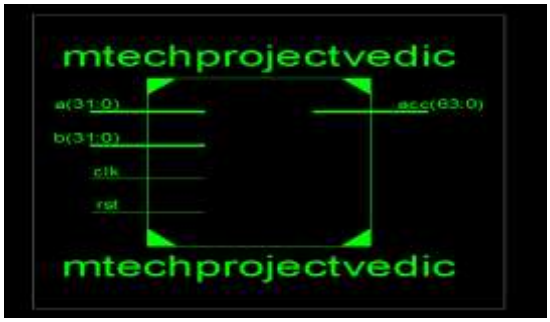


Fig 6:RTL of MAC using Vedic Multiplier

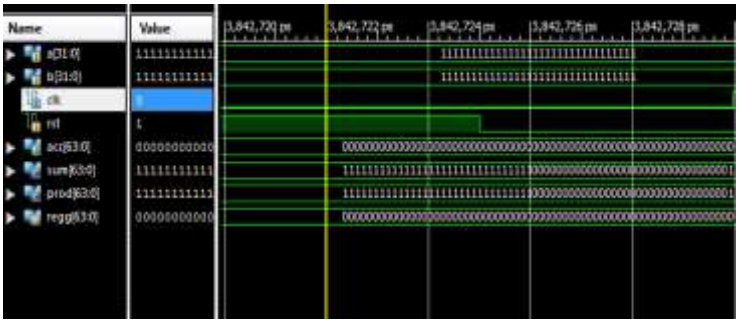


Fig 7: simulation waveforms of 32 bit MAC unit using vedic multiplier

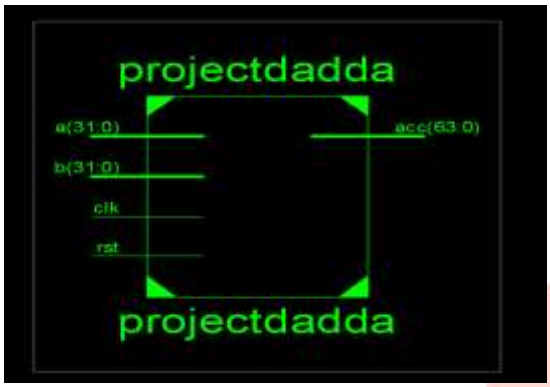


Fig 8 : RTL of 32 bit MAC unit using DADDA Multiplier

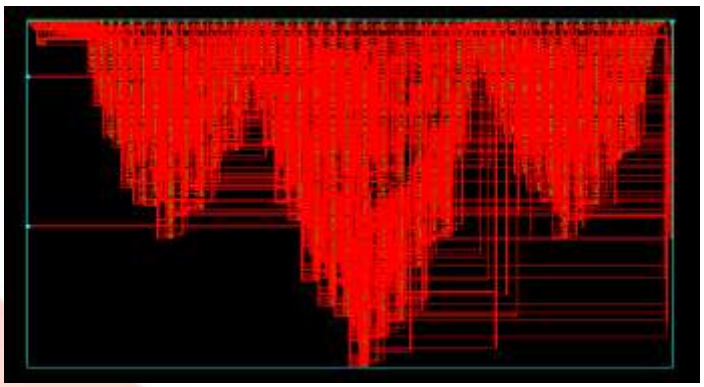


Fig 9: TTL of 32 bit MAC unit using DADDA Multiplier.

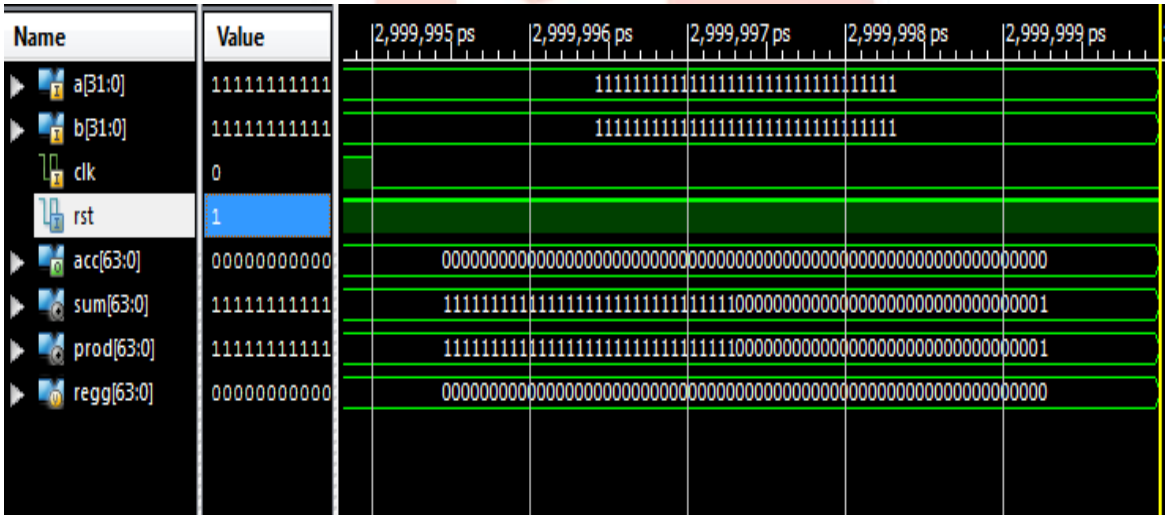


Fig 10 : simulation results of 32 bit MAC unit using DADDA Multiplier

V .Comparison of MAC units designed by using different multipliers

TABLE:1 Comparison of Different MAC units

Parameters	32 bit MAC unit designed by		
	Conventional (Binary)Multiplier	Vedic Multiplier and Reversible logic gate	DADDA Multiplier and Reversible Logic gate
Area	2072	2200	1951
Power(mw)	16	15	14

VI. CONCLUSION

On designing the MAC unit using DADDA Multiplier and by using Reversible logic the results obtained in terms of area and power are better when compared to MAC unit designed by using vedic Multiplication technique and also general Binary Multiplication process. Here there is improvement in terms of area about 10% and smaller change in terms of power and as DADDA Multiplier is faster than many other basic Multipliers this MAC unit is relatively faster.

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