An Efficient Approach for High Speed Circular Convolution Using 4 Bit Urdhva Triyakbhayam Sutra Based Vedic Multiplier

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***Abstract*—Multipliers and dividers are the basic blocks in convolution and de-convolution fabrication, Multipliers and Dividers consumes much of the time for computation, This thesis presents a direct method of computing circular convolution. This approach is simple and easy to implement because of the similarity to computing the multiplication of two numbers. The unique factor of the proposed method is the implementation of multiplier and divider architecture using Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhayam Algorithm. The result shows that the implementation of circular convolution using Vedic mathematics is more efficient than the conventional method in terms of area, speed and delay compared to their implementation using conventional multiplier & divider architectures. In this thesis I have proposed 4bit multiplier using Urdhvatriyagbhayam Sutra, The coding is done in VHDL Software. Simulation and Synthesis are performed using Xilinx ISE design suit 14.2,simulated results for proposed 4x4 bit Vedic convolution circuit shows a reduction in delay of 88% than the conventional method and 41% than the OLA method.**

***IndexTerms*—Convolution,VHDL,multiplier**

I. INTRODUCTION

Presently multipliers considered as most important part of any high speed performance digital system. Particularly in digital signal processing units for operations such as convolution multipliers required and therefore it affects the overall efficiency of the system. Also in other digital system such as processors, communication system and filters multipliers performing the operations of multiplications. The main parameter which defines the performance of any digital device or system is the processing time for example multipliers are digital circuit and performs multiplication of tow numbers but the time taken by it to reach the result is important so it should be highly efficient and faster in terms of calculations. In nowadays the area of research with ample opportunities mainly focused on reducing the propagation delay of the system with low power consumption and less area of fabrication in reference to VLSI industry.

II. MOTIVATION

Under the progress of VLSI based designed systems and devices we have come from a long distance right from single and large size transistors to CMOS circuitry. In [3] presented the research and development of low delay and less power consumption based designed digital system to meet the present requirements. As we know the system performance of a digital system has been improved with the implementation of high speed of operations of adders and multipliers. In this context I referred the new schemes proposed by the researchers to develop more efficient as well as faster multipliers.

III. VEDIC MULTIPLIER

At the earliest Indian time it was Vedic mathematics which was used for the purpose of computation based on the defined sutras. It has been presented that the "Vedic" word came into existence from "Veda" having knowledge house as the meaning defined by Shri Bharti KrishnaTirtha given to describe high speed digital devices and processing unit. In thesis we have conceptually explained Vedic sutras particularly (UT) and how it can be used in the development of high speed multiplier for different applications of digital processors. In general multiplication and addition are basic arithmetic operation can be done as a test number given as multiplicand is added to itself several times as defined by the other test number configured as a multiplier to achieve the output of the multiplication.

IV. PROPOSED METHODOLOGY

The main motive of this paper is to design and implement high efficient digital processor with a low delay which can be integrated with many digital applications. In our work we have proposed Kogge Stone Adder as a prefix adder defined in [20] and named by the researchers Kogge P and Stone H in 1973 by using an Ex-OR gate (performs multiplexer operations) to mitigate the delay.

Kogge Stone Adder as a prefix adder defined in [20] and named by the researchers Kogge P and Stone H in 1973, the concept was developed as KSA is the kind of prefix adder with some special and fast features. It comprises of three parts including preprocessing part, carry generator part and post processing part.

$P=X_i \oplus Y_i$ 1

$G = X_i \ Y_i$ 2

$C_i= G_i$ 3

$S_i= P_i \oplus C_{i+1}$ 4

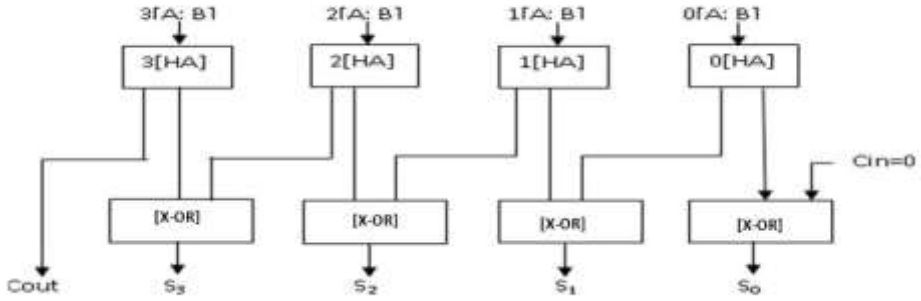

Figure 3.5: Kogge-Stone Adder using X-OR gate

VEDIC MULTIPLICATION

As discussed in the previous chapter we have used UrdhvaTiryakbhayam (UT) sutra of Vedicmaths for multiplication concept which is appropriate for any number system such as decimal, binary or hexadecimal. To understand the concept well we have taken example based learning with two decimal numbers as shown in the figure below.

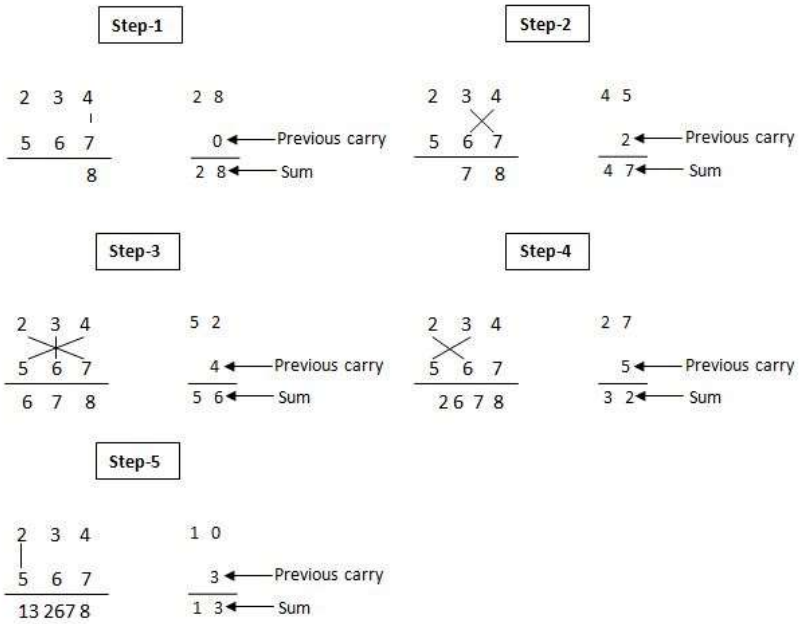

Figure 3.6: Multiplication of two decimal numbers by UT Vedic sutra

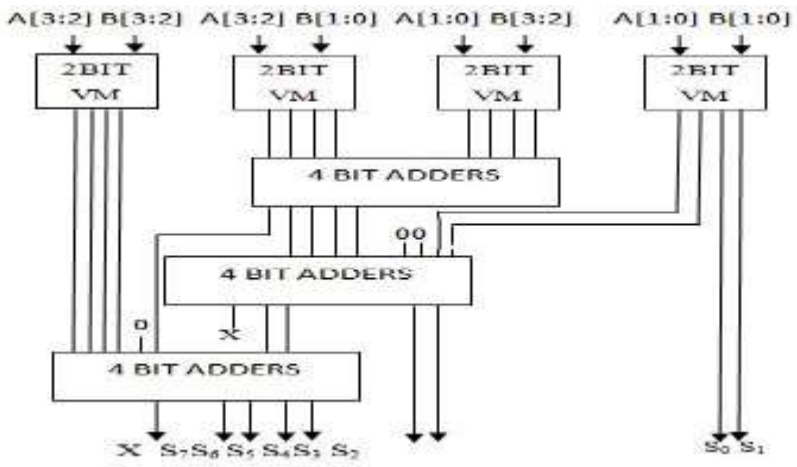

Figure 4.4: 4x4 Vedic multiplier using Kogge-Stone Adder with XOR gate

We have performed simulation using Xilinx 14.2i Spartan 3E series.

Device Utilization Summary			**(Estimated values)**
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	315	3584	8%
Number of 4 Input LUTs	560	7168	7%
Number of Bonded IOBS	72	221	32%

Table1 : Device utilization Summary circular convolution using 4 bit UT sutra based VM

model

Method	**Delay**
Conventional Method inbuilt	62.47 ns
Proposed Circular Convolution Method	16.505 ns

Table2:Comparison between conventional convolution method and Proposed Circular Convolution Method

V. CONCLUSION AND FUTURE WORK

In the digital circuit systems and campaign, digital processor based on low power VLSI plays a vital role for the high and efficient performance. The designing points for assumptions in the case of a better recital in VLSI are speed, area and cost so in our work we have analyzed and focused on these factors. The present scenario of the low power devices advances with latest designing, cost effectiveness cooling and packaging, reliability, and portability. In the thesis work we have performed detailed literature survey and studied prefix adders including CLA, CSA. We have developed an approach towards high efficient and low delay digital processor for this modification of Vedic multiplier using KSA based on X-OR gate designed and implemented which reduces the number of slices, area, and delay.

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