Novel Low Power and High speed CMOS based XOR/XNORs using Systematic Cell Design Methodology

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***Abstract*—The XOR and XNOR gates are the essential blocks of various digital arithmetic and logical units such as digital adder, digital parity generator/checker and digital comparator. Many circuit topologies have been proposed till now of full adder and XOR/XNOR gate design that can be categorised in two categories. First category offers full swing output and second category offers partial swing output. The Systematic Cell Design Methodology is partial swing based logic design method which offers less delay and low power consumption at weak logic '0' and logic '1' generation at output. The proposed 18T design offers least delay and power dissipation as compared with existing design. The existing design TG16T, TGM16T, TGM18T, TF, Hybrid and LPHA-FA offers 6%, 6%, 22%, 28%, 61% and 111% higher average propagation delay than proposed 18T XOR/XNOR design, while offers 16%, 23%, 19%, 9%, 2%, 33% higher average power dissipation than proposed 18T XOR/XNOR design. In this work results are simulated at 1.2Volt and 130nm technology.**

***Index Terms*— Hybrid CMOS logic, XOR/XNOR gate, partial swing logic, full swing logic.**

I. INTRODUCTION

XOR/XNOR gates are one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application-specific DSP architectures and microprocessors. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, division, address calculation, etc. In most of these systems the adder is part of the critical path that determines the overall performance of the system. With the explosive growth, the demand, and the popularity of portable electronic products, the designers are driven to strive for smaller silicon area, longer battery life, higher speed, and enhanced reliability is increases with technology scaling. As Technology scaling increases the transistor count and operating frequency, which push the market demand for more and more function in Integrated circuit. However scaling always increases leakage power dissipation. As channel length reduces which results in increase of power dissipation with respect to technology progresses. To reduce the power consumption different logic design techniques like CMOS complementary logic, Dynamic CMOS, Pseudo NMOS, Dynamic CMOS, CMOS Domino logic, Cascade voltage switch logic (CVSL), Modified Domino logic, Pass Transistor Logic (PTL) have been proposed [1-3]. Power dissipation depend on device structure property like gate oxide thickness, channel length, doping profile etc. as they are due to different physical phenomena Although Static CMOS Logic has been the most popular design approach for the past three decades [4, 5]. By scaling down the feature size of MOSFET devices in nano-meter, the supply voltage should be scaled down to avoid hot- carrier effects in CMOS circuits. To enhance the speed of the CMOS circuits, threshold voltage of the circuits has to be scaled down. The dynamic XOR/XNOR logic gate is one of the most primary building blocks of arithmetic and logic unit (ALU) used in microprocessor. This plays an important role in silicon on chips (SoCs) to design ALU in small die area that reduce manufacturing cost. This system inbuilt ALU occupy more area on silicon chip that dissipate more heat and elevate the temperature of chip. This thing degrades the performance of system. In order to save the chip heat sink is needed that release the internal heat to external environment. As the operating frequency of dynamic XOR improves, dynamic power consumption becomes dominant that introduce heating problem as mentioned above. To overcome this problem, dynamic XOR gate proposed with minimum delay and smaller power consumption.

The remaining paper is organized in the following order. Section II presents the **Review on Published Literature** , Section III describe the **Proposed SCDM based XOR/XNOR gate**, Section IV presents result and analysis[6] and Section V presents the concluding remarks.

II. REVIEW ON PUBLISHED LITERATURE

The recently published novel work can be divided into two categories as they are extracted from the topic: 1) traditional three input XOR gate and 2) its operating methodologies. Cell design methodology (CDM) has been presented to design some limited

functions, such as two-input XOR/XNOR and carry–inverse carry in the hybrid-CMOS style [5, 7, 8]. The predominant results persuade us to improve Cell Design Methodology (CDM) through two stages: 1) generating more complex functions and 2) rectifying some remaining flaws. The flaws in previously published CDM include containing some manual steps in the design flow and generating a large number of designs in which the predominant ones would be determined after the completion of simulations. Therefore, in the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input basic gates in arithmetic circuits have been chosen. If the efficiency of the circuits is confirmed in such a competitive environment, it can show the strength of the methodology. In the second stage, CDM is matured as systematic CDM (SCDM) in designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell (EBC) using binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the CDM. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product (PDP) as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets. The motivation to use this methodology is the presence of some unique features and the ability to produce some efficient circuits that enjoy all these advantages.

The SCDM divides a circuit structure into a main structure and optimization-correction mechanisms. In the main structure, it considers features including the least number of transistors in critical path, fairly balanced outputs, being power ground- free, and symmetry. The mechanisms have the duty of completing the functionality of the circuits, avoiding any degradation on the output voltage, and increasing the driving capability. The dynamic consumption optimization comes from the fact of well-balanced propagation delay. This feature is advantageous for applications in which the skew between arriving signals is critical for proper operation, and for cascaded applications to reduce the chance of making glitches [9]. Power-ground-free main structure leads to power reduction.

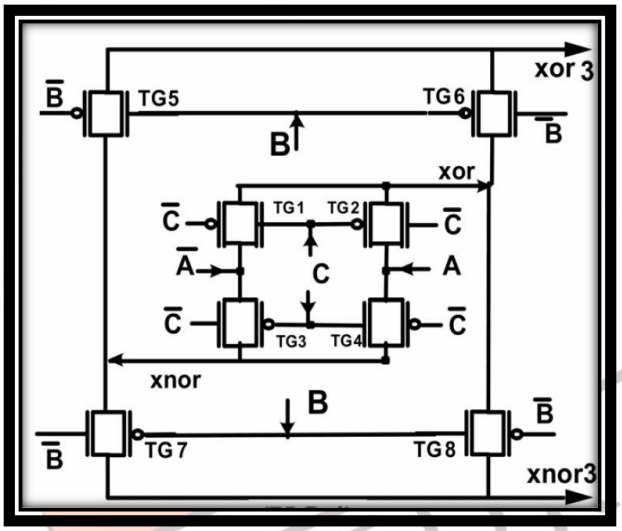

Fig.1 Three input XOR/XNOR using transmission gate(TG16T)[11]

The degradation in all output voltage swing can thus be completely removed, which makes the design sustainable in low *V*DD operations and low static power dissipation. The methodology has high flexibility in target and systematically considers it in the three design steps. This can lead to efficient circuits in terms of performance, power, power delay product, energy delay product, layout area.

The fast evolution of microelectronics fabrication processes demands a new cell library generation or a library technology migration. The well-organized systematic methodology leads to automated flow, which can reduce design time and costs, provide consistency in the cell library generation process, increase the range of simulation capabilities at the characteristics step, as well as minimize the risk of errors [7, 10]. Recently published article on hybrid type systematic cell design methodology (SCDM) applied on three circuits as shown in Fig.1, Fig.2 and Fig.3. The Three input XOR/XNOR based transmission gate using 16 transistors (TG16T)[11] shown in Fig.1. Another three input XOR/XNOR based transmission gate and mirror circuit using 16 transistors (TGM16T)[11] shown in Fig.2. next is three input XOR/XNOR based transmission gate and mirror circuit using 18 transistors (TGM18T)[11] shown in Fig.3. All three circuit have six inputs (A, B, C and compliment of all three inputs) and two outputs (XOR and its compliment).

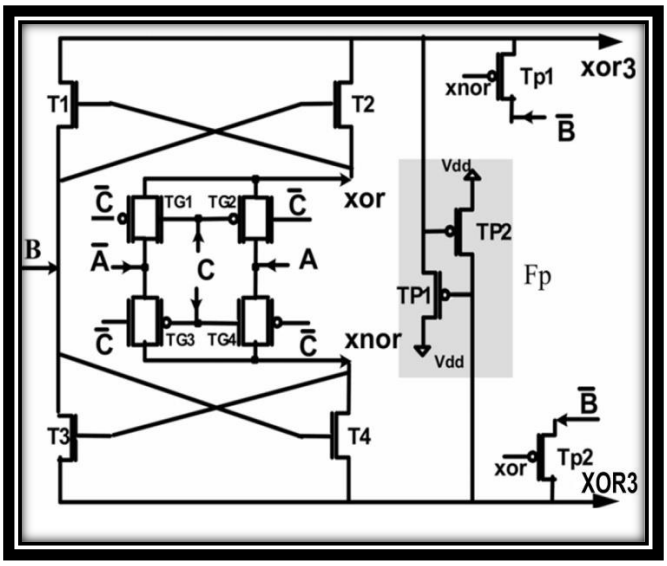

Fig.2 Three input XOR/XNOR using transmission gate and mirror circuit (TGM16T)[11]

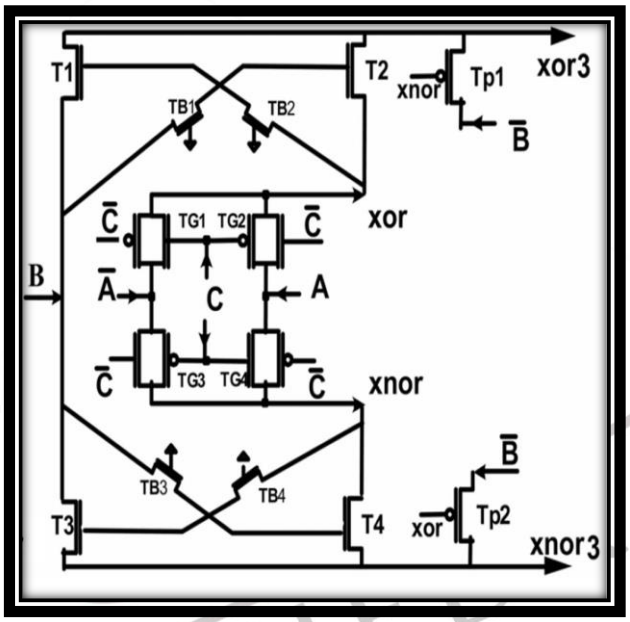

Fig.3 Three input XOR/XNOR using transmission gate and mirror circuit (TGM18T)[11]

III. PROPOSED SCDM BASED XOR/XNOR GATE

The proposed SCDM based design is based on 18 transistors circuit as shown in Fig. 4. As like existing SCDM, The predominant results persuade us to improve Cell Design Methodology (CDM) through two stages merging: 1) generating more complex functions and 2) rectifying some remaining flaws. In this cell, two back to back connected pull-up devices TPP1 and TPP2 are introduced between node XOR3 and XNOR3. The complex function generator connected with feedback transistors using pass transistor TB1, TB2, TB3 and TB4 that helps in power reduction. The proposed cell offers smaller delay and power consumption by eliminating transistors Tp1 and Tp2 from SCDM based XRG2 and XRG3 network.

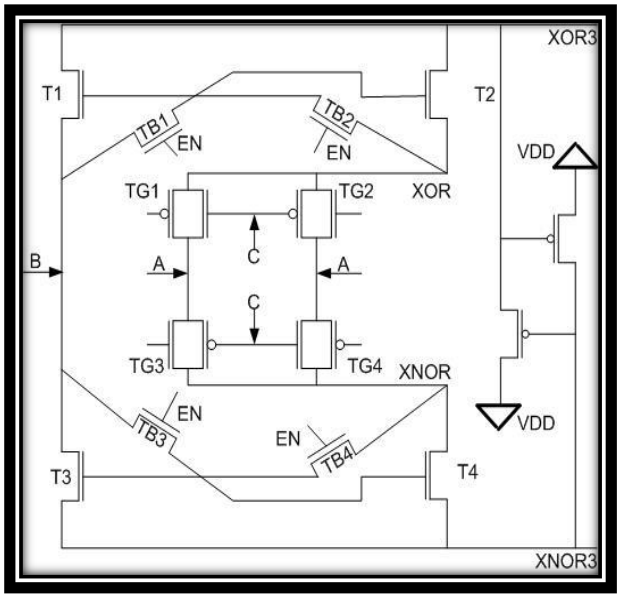

Fig.4 Proposed SCDM based 18T XOR/XNOR gate

IV. Result And Analysis

To analyze the performance of three input XOR/XNOR gate, it is necessary to study the transient analysis and process variation. This comparison have been performed complete study using Hspice [12]. To investigate further several modules with complementary outputs of full adders (FAs) TFA, Hernandez1, Hernandez2, NEWHPSC, Hybrid, 18T_new_FS, and LPHS-FA have been analysed, whose excellence have been confirmed in [13] [14] and [15-17]. Therefore, an approximately fair comparison will take place by selecting them. For fair comparison, this section covers the TG16T[11], TGM16T[11], TGM18T[11], TF[18], Hybrid[16] and LPHA-FA[13] designs for result analysis. . The existing design TG16T, TGM16T, TGM18T, TF, Hybrid and LPHA-FA offers 6%, 6%, 22%, 28%, 61% and 111% higher average propagation delay than proposed 18T XOR/XNOR design, while offers 16%, 23%, 19%, 9%, 2%, 33% higher average power dissipation than proposed 18T XOR/XNOR design. Similarly proposed design offers lower PDP (power delay product) and lower EDP (energy delay product) TG16T[11], TGM16T[11], TGM18T[11], TF[18], Hybrid[16] and LPHA-FA[13]. The transistor count of proposed design is same as TGM18T.

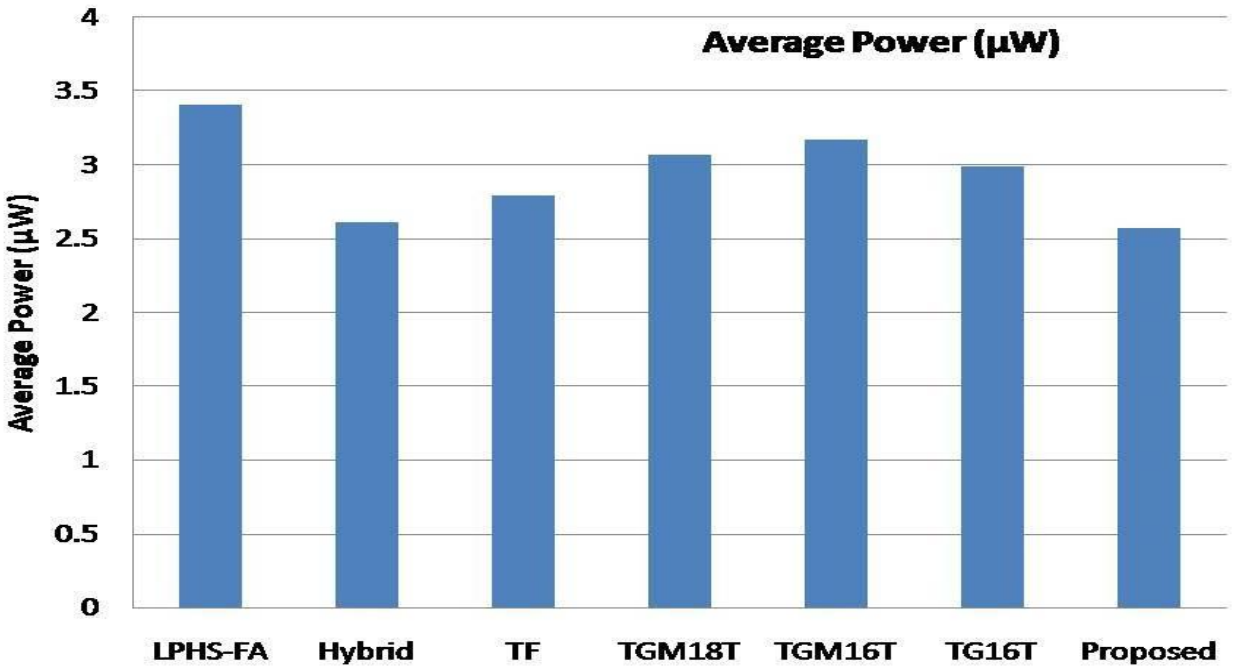

Fig.5 Comparison of average power (µW) at 130nm technology

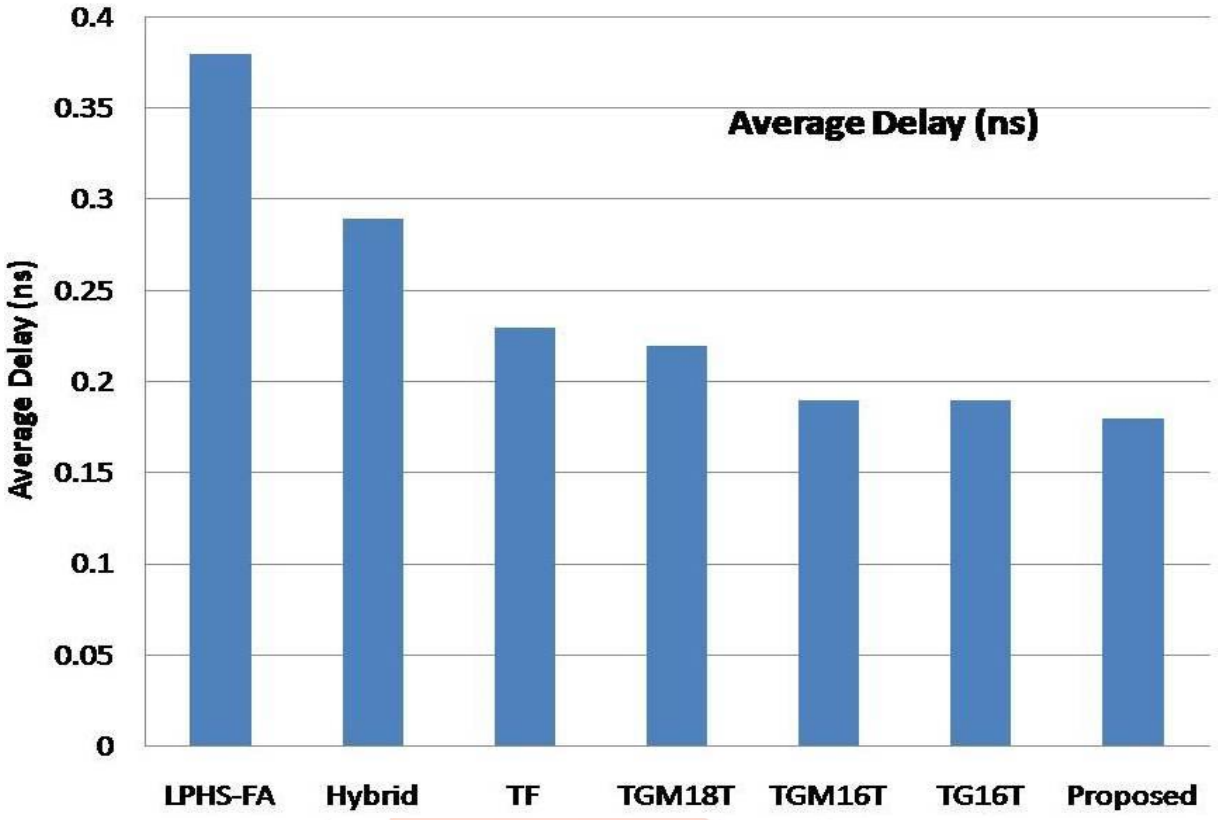

Fig.6 Comparison of average delay (ns) at 130nm technology

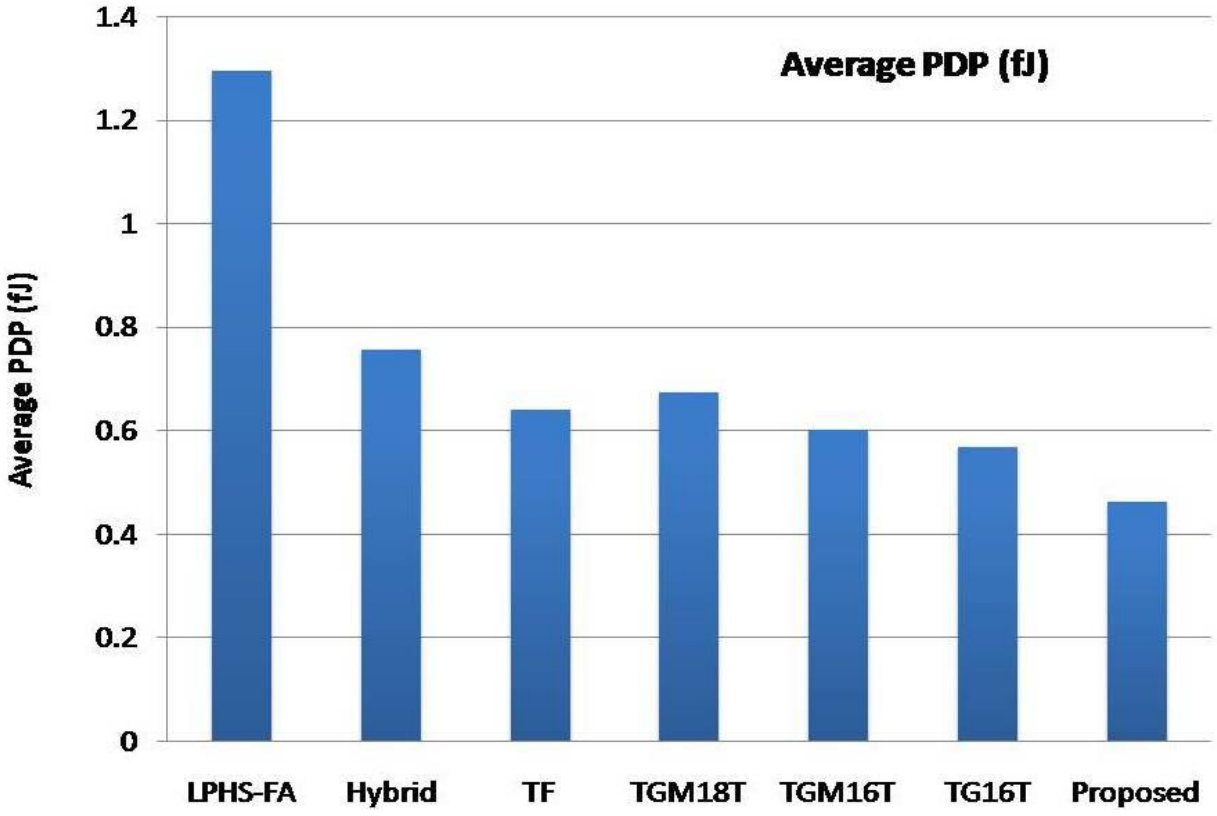

Fig.7 Comparison of average PDP (fJ) at 130nm technology

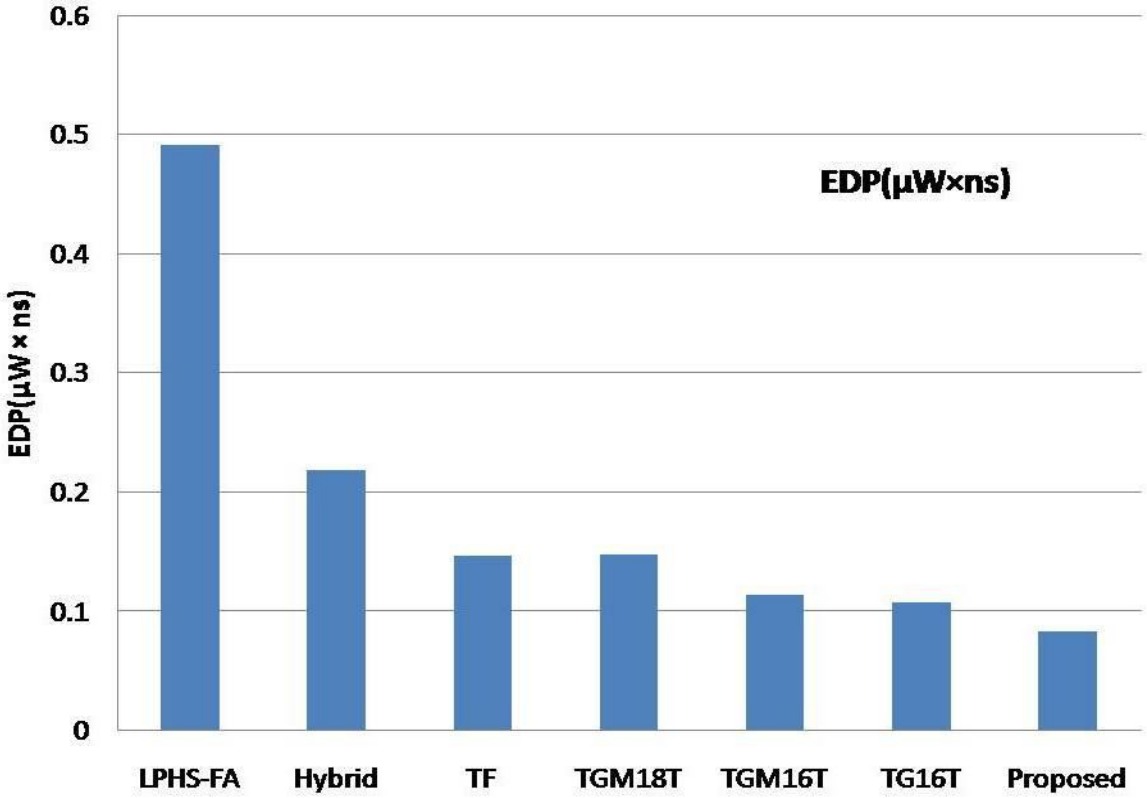

Fig.8 Comparison of EDP (µW×fJ) at 130nm technology

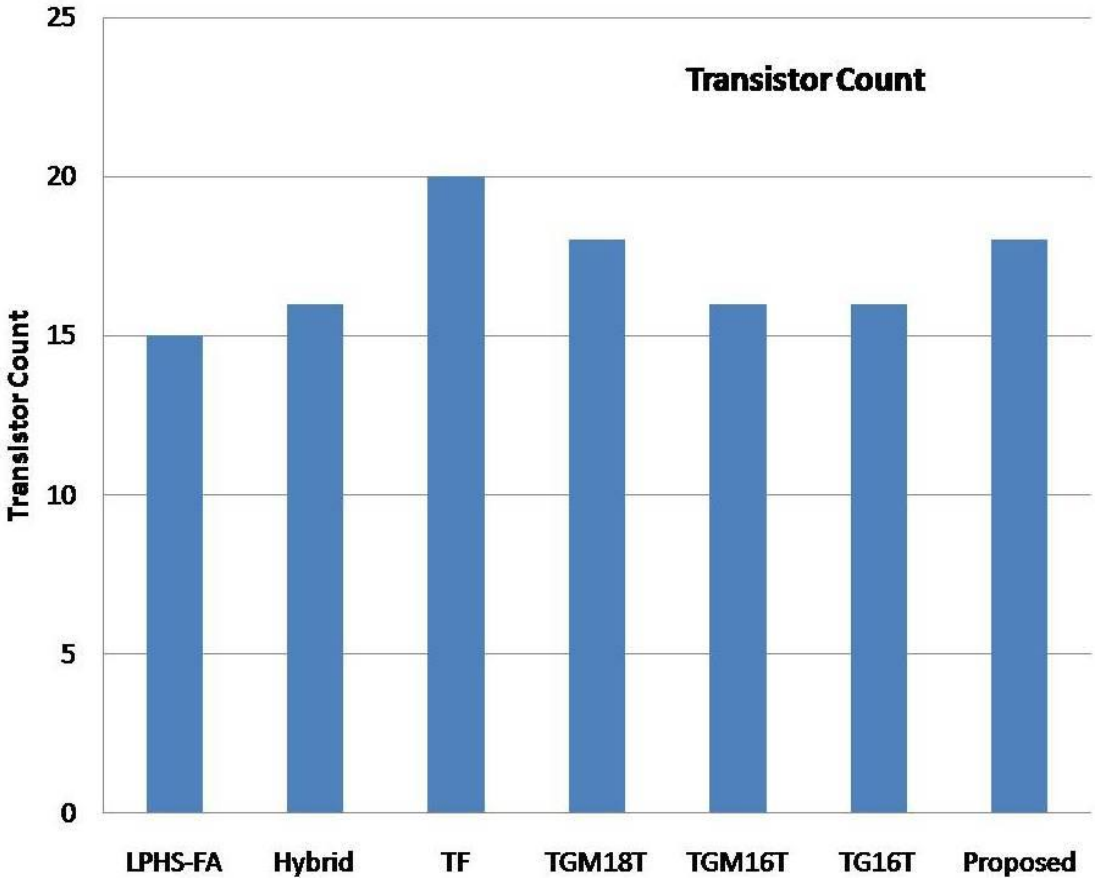

Fig.9 Comparison of transistor count

V. CONCLUSION

The logic gates such as XOR/XNOR are repetitively involved used in high performance data processing units such as Adder, Comparator and Multiplier. Logic gate with optimized delay and power consumption is in demand for high speed integrated circuit. The proposed 18T design offers least delay and power dissipation as compared with existing design. The existing design TG16T, TGM16T, TGM18T, TF, Hybrid and LPHA-FA offers 6%, 6%, 22%, 28%, 61% and 111% higher average propagation delay than proposed 18T XOR/XNOR design, while offers 16%, 23%, 19%, 9%, 2%, 33% higher average power dissipation than proposed 18T XOR/XNOR design. Therefore, this design is best choice for low power and high speed portable device.

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