Design and Analysis of Vedic Multiplier by Using Modified Full Adders

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Abstract— In digital circuits multiplier has important role in calculations. These are the main important blocks in many applications like digital signal processing, microprocessor and microcomputers. The time that required to doing calculation in multiplier is reduced by using Vedic multipliers. Vedic Mathematics is the fastest and low power multiplier. Vedic Mathematics have sixteen sutras but "Urdhva Tiryagbhyam" is mainly used .In this paper 16 bit Vedic multiplier is designed by using modified full adders which has used less number of slices and delay is reduced when compared to existing techniques of Vedic Multiplier. In this paper 16 bit Vedic Multiplier using modified full adder 2 has better performance in terms of delay, memory utilization and number of slices as compare to other modified full adders. Simulation and synthesis are carried on XILINX ISE 14.4 software.

Keyword – Vedic Multiplier, Full Adder using Multiplexer, Ripple Carry Adder, VLSI.

I. INTRODUCTION

Vedic Mathematics is very simple and easy to understand. It improves the speed of calculation. The word 'Vedic' is obtained from the word 'Veda' and its meaning is "store house of all knowledge". Vedic multiplier has applications in many fields like Microprocessors, Fourier transform, Communication and Digital Signal Processing. Ancient Vedic mathematics consists of 16 Sutras and they are related to different branches of mathematics like algebra, arithmetic and geometry. Vedic Multiplier mainly used "Urdhva Tiryagbhyam" (Vertically and Crosswise) which is used for both binary and decimal multiplication. This technique contains generation of partial products and then performs addition simultaneously. This method can be used for 2x2, 4x4……NxN bit multiplication. Vedic Multiplier reduces the power consumption and gives results in less time.

II. VEDIC MULTIPLIER

Vedic Multiplier is designed by using adders and multipliers. In this paper 16 bit Vedic multiplier is designed by using 4 full adders which are designed by using different methods. These modified full adders give different results.

1. FULL ADDER USING HALF ADDERS

In this full adder it is design by using two half adders and an OR Gate. Inputs are 'a', 'b', 'cin' and outputs are 'sum' and 'carry'.

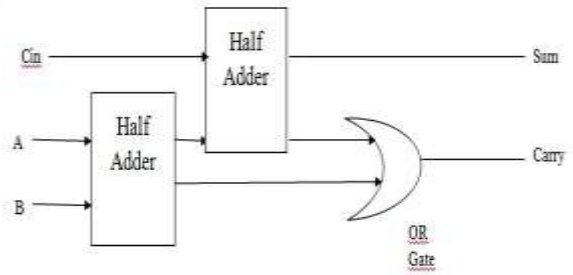

Fig.1: Full Adder using Half Adders

2. MODIFIED FULL ADDER 1

In this full adder it is design by using XOR Gate and 2:1 multiplexer. Inputs for XOR Gate are 'a', 'b', 'cin' and output is 'sum'. The inputs for multiplexer are 'b', 'cin' and select line is 's' and output is 'carry'.

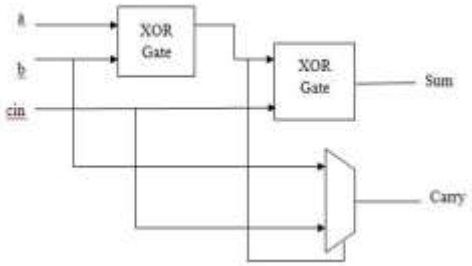

Fig.2: Modified Full Adder 1

3. MODIFIED FULL ADDER 2

In this full adder two 4:1 multiplexer are used. Inputs for first multiplexer are 'c', 'not c', 'not c', 'c' and selection line are 'a' and 'b' and the output is 'sum'. Whereas inputs for the second multiplexer are '0','c','c','1' and selection line are 'a' and 'b' and the output is 'carry'.

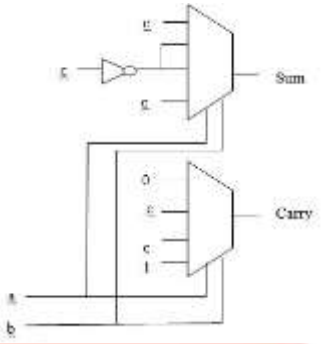

Fig.3: Modified Full Adder 2

4. MODIFIED FULL ADDER 3

In this full adder XOR Gate, XNOR Gate and 2:1 multiplexer is used. Inputs for XOR Gate are 'a' and 'b' and the intermediate output is 'y'. Inputs for XNOR Gate are 'a' and 'b' and intermediate output is 'z'. Inputs for first multiplexer are 'y' and 'z' and selection line is 'cin' and the output is 'sum'. Inputs for the second multiplexer are 'a', 'cin' and the selection line is 'y' and the output is 'carry'.

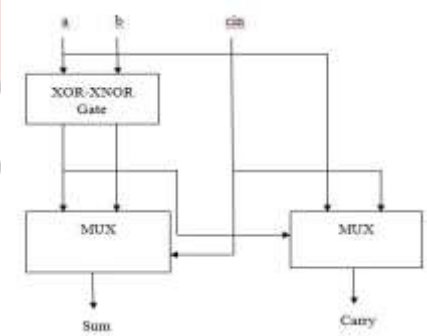

Fig.4: Modified Full Adder 3

By using AOI logic gate counts for various bit adders using full adders are as follows:

1. 4Bit Adder: It consists of 1 half adder and 3 full adders.
2. 6 Bit Adder: It consists of one 4 bit adder and 2 full adders.
3. 8 Bit Adder: It consists of one 6 bit adder and 2 full adders.
4. 12 Bit Adder: It consists of one 8 bit adder and 4 full adders.
5. 16 Bit Adder: It consists of one 12 bit adder and 4 full adders.
6. 24 Bit Adder: It consists of one 16 bit adder and 8 full adders.

These adders are used to design 16 bit Vedic Multiplier.

III. PROPOSED METHODOLOGY

In 16x16 bit multiplier, the multiplicand consists of 16 bits each. The result of multiplication is 32 bits. In this multiplier 8 bit Vedic multiplier, 16 bit adder and 24 bit adder is used. It consists of three sections. In which first set consists of a (7:0) and

b(7:0), second set has a(15:8) and b(7:0), third set has a(7:0) and b(15:8) and fourth set consists of a(15:8) and b(15:8). The output of these is 16 bits. In second section one 16 bit adder and one 24 bit adder is used. In third section 24 bit adder is used. The output of second section is given to 24 bit adder. The output of this adder is (32:8). Lowest bits of output are taken from 8 bit Vedic multiplier output that is (7:0).The Final Output has 32 bits.

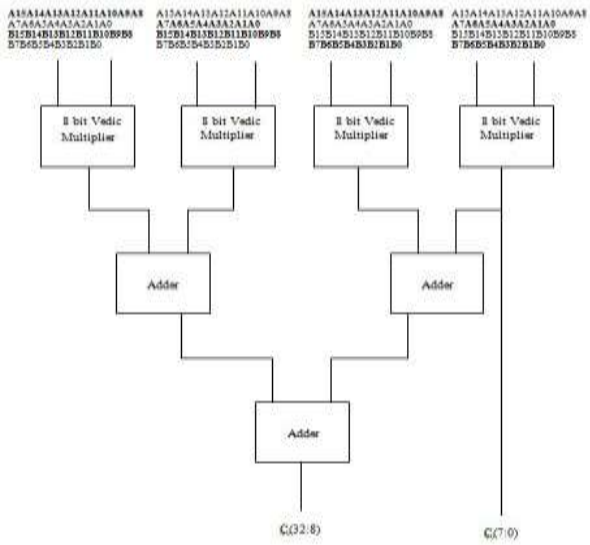

Fig.5:16 bit Vedic Multiplier

IV. RESULTS

The proposed methodology is simulated and synthesized on Xilinx ISE 14.4 software.

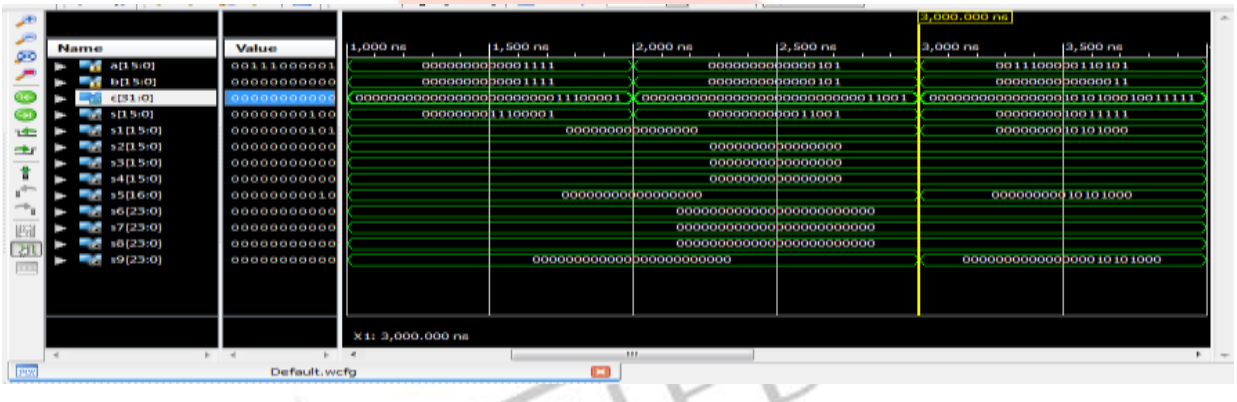

Fig.6: Simulation Results of 16 bit Vedic Multiplier

The first input for 16 bit Vedic multiplier 'a' is "0000000000001111" and 'b' is "0000000000001111" and the output 'c' is "00000000000000000000000011100001". Second input for 'a' is "0000000000000101" and 'b' is "0000000000000101" and the output 'c' is "00000000000000000000000000011001". Third input for 'a' is "0011100000110101" and 'b' is "0000000000000011" and the output 'c' is "00000000000000001010100010011 1".

Table 1: Performance Analysis for 16 bit Vedic Multiplier Using Modified Full Adders.

Parameters	Full Adder	Modified Full Adder 1	Modified Full Adder 2	Modified Full Adder 3
No. of Slices	378	481	376	388
Delay	15.106ns	14.926ns	13.201ns	13.927ns
Memory	314228KB	345524KB	313972KB	314228KB

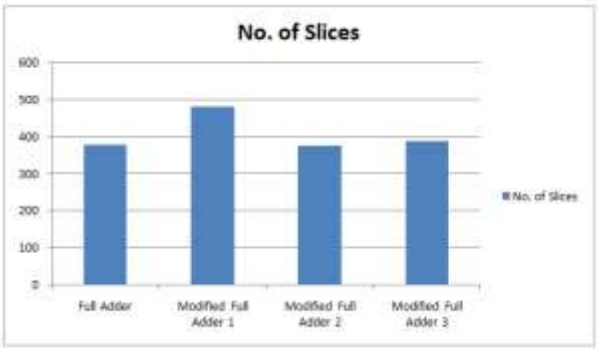

Fig 7: Comparison of Number of slices of 16 bit Vedic Multiplier

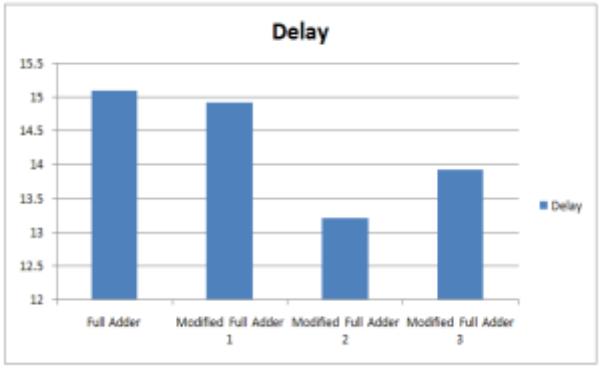

Fig 8: Comparison of Delay of 16 bit Vedic Multiplier

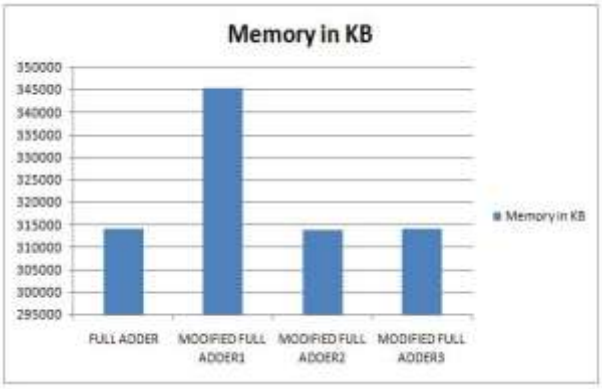

Fig 9: Comparison of Memory Utilization of 16 bit Vedic Multiplier

V. CONCLUSION

This paper presents the proposed architecture of Vedic multiplier by using different adders. In this paper modified full adders are used to design 16 bit Vedic multiplier which improves the performance of 8 bit Vedic multiplier by calculating delay and memory utilization. Modified full adder 2 has better performance in terms of delay, number of slices and memory utilization.

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