Power Analysis of Novel Glitch Resistant DET-FF

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Abstract: This paper presents the design of novel low power glitch resistant DET-FF. The presented glitch resistant DET-FF reduces the delay and average power consumption and increases the speed of the device. To improve the results, the 1P-2N structure combined with the C-element structure. To reduce the area, the two 1P-2N structures are merged. The proposed novel glitch resistant DET-FF is implemented with 32 nm CMOS technology and simulated through the SPICE. The power supply voltage and system clock frequency of proposed novel glitch resistant DET-FF are fixed to 1V and 500 MHz respectively.

Keywords: Average power consumption; Clock networks; Dual edge triggered; Glitch resistant; Power delay product.

I. INTRODUCTION

In this digital era, the flip flops are widely used for data storage. To increase the flip flops reliability, speed and power consumption, the fault resistant capacity must be improved. Therefore, it is needed to design the flip-flops for lowest average power consumption, smallest delay and area and maximum reliability with fault resistant capacity. Presently, the device scaling reduces the supply voltage requirement, transistor size, device capacitances, node charge and increases clock frequency therefore the circuits become vulnerable to the glitches. Voltage transient as a result of the collected charge is called a transient fault. In memory elements transient faults may be produced by the preceding combinational circuit glitches. Voltage supply scaling is a very efficient step to lower the power consumption. In static CMOS circuit designs, power consumption due to the glitches cannot be ignored as the portion of power consumption varies from 9% to 38% [1].

In the field of digital integrated circuits and systems, the energy-efficient circuit design is one of the great challenge for the researchers [2]. In [3-7] the authors presented novel designs which are reduced great power consumption and provide the fault free output with higher performance results. Clock network consumes more power, therefore, this is necessary to reduce the clock count. To reduce the clock count, the true single phase clock (TSPC) technique has been advised with the basic registers [8]. In [9], the authors proposed DET-FF to overcome the built-in clock overlap threat, by using true single phase clock circuits instead of an inverted clock. Power consumption in clock distribution network is very significant, which may account 45% of the total system power [10].

To reduce the clock power consumption, the clock frequency can be scaled down, by sampling the data on both of the falling and rising edges of the clock, without altering the system throughput. The DET procedure reduce the 50% power dissipation of the clock network system. Although DET designs are more complex as compared to single edge triggered (SET) designs, this can be more energy efficient [11]. The dual data rate flip flop (DDR-FF) has a lower clock load by cause of its simple configuration and lower activity factor because of its hard edge quality factor [12]. DET flip flops provide the equal data rate as SET flip-flops at the half of the clock frequency, which leading reduction in power dissipation of digital synchronous logic designs [13-14]. Therefore, we have presented a novel low power glitch resistant DET-FF which can work accurately at low voltage supply.

The rest part of this paper is organized as follows. Section II includes, background study. We have discussed the proposed design in section III. Section IV explains the comparative analysis of different DET-FF designs and finally section V, concludes this work.

II. BACKGROUND STUDY

To reducing the energy consumption and to improve performance of digital systems, presently the many more researchers focus on DET flip flops. In [12], the authors presented a robust dual edge flip-flop by using c-elements, where the direct clock pulses used to latch the data for the reduction of clock dynamic power consumption without any additional pulse generator circuit. This flip flop design offers more robust solution for dual data rate (DDR) flip-flops due to its simplicity with less number of transistors. The dual data rate flip-flop has a lower power dissipation and lower delay due to the lower clock load and lower activity factor [12].

For low-power and high-performance designs, dual-edge-triggering method is a better choice for researchers. In [9], the authors proposed a static DET flip-flop, fig. 1, which totally discard clock overlap threat by using a true single phase clock edge instead of an inverted clock edge in the process. In [9], the authors clarify the issue of clock overlapping by using the true single phase clock (TSPC) circuits and an internal dual-feedback structure.

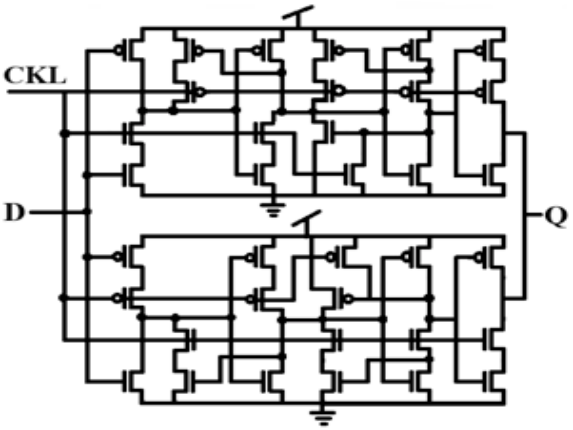

Fig. 1 TSPC design [9]

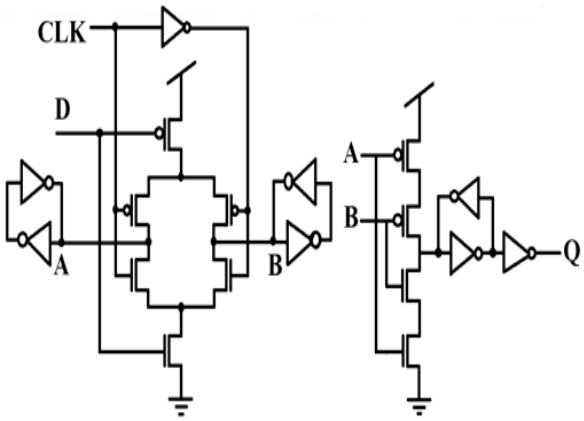

Fig. 2 LG_C design [15]

In [15], the proposed design improved with common Latch-MUX DET flip flops, because of this, their internal circuit node value never changes with the changes in the input signal. The proposed LG_C circuit design [15] presented very much improvement on Latch-MUX DET flip-flop circuit designs in the field of energy dissipation because of glitches at the input node. The glitch free LG_C DET flip flop designed by three C-element circuits, which are two internal latches A and B and one output latch Q, with inverting topology because of the transistor level implementations, presented in fig. 2. To reduce the switching activity, generally the C-element structures are used, accordingly flip flop's latches nevermore follow the input signal over the active mode. In [15], at the input side, to control the input loading the two C-element circuits merged to share transistors connected to the D input.

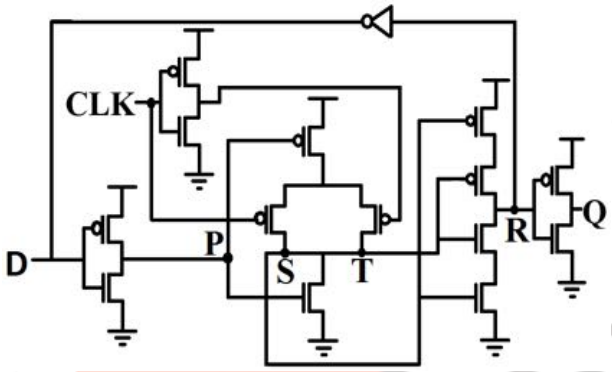

Fig. 3 AGF_DET_FF design [18]

In this research paper we have used 1P-2N three transistor structure [16] with the combination of C-element structure [17]. The existing C-element structure is a 3 terminal structure with the two inputs and a single output. The C-element circuit has the special feature that when it's both inputs are equal, thereupon it behaves like a simple inverter; when the inputs are not equal, thereupon the output will be in its past state.

In [16], the three transistor structure is different from the C-element circuit: i. when the inputs are not equal than the output may not go to the high impedance state. ii. The C-element circuit has four transistors, but these structures have three transistors. In [18], the authors presented Advance Glitch Free Dual Edge Triggered Flip Flop (AGF_DET_FF) design, as shown in fig. 3. This design is totally glitch free design and can reduces the glitches that may be appeared at the input node from the previous circuits. This design also reduces the delay and average power consumption and increases the speed of the device.

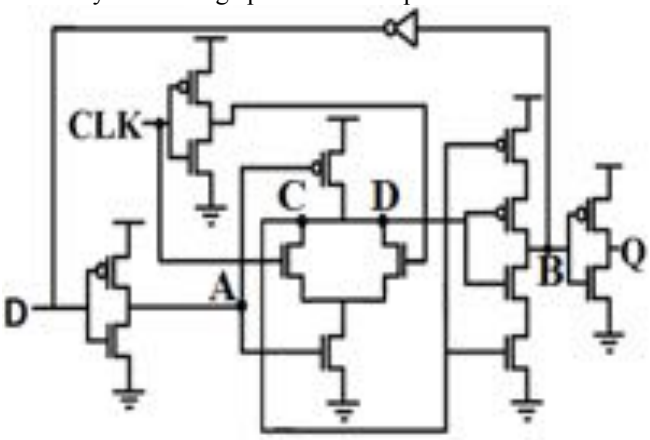

Fig. 4 Novel GR-DET-FF

III. PROPOSED DESIGN

Today, the main goal of the researchers is to achieve small area, low power and high speed in the field of VLSI designing. Consequently, many more approaches have been considered by the researchers in VLSI applications to achieve the motive. We have designed Glitch Resistant Dual Edge Triggered Flip Flop (GR-DET-FF) circuit design, shown in fig. 4. The proposed circuit model consumes less power and provide glitch free output

The working of this design is as follows: case 1, the glitch either filter out at the node B or propagate to the output node Q, case 2, if glitch propagate to the output node, then it is filtered out through the feedback path. Now we can assume that the initial state of nodes A and B to be A=B=0, C=D=1, the output Q=1 and clk=0.

At the node A, if any glitch occurs from the preceding combinational circuit, then the value of the node A will be changed from 0 to 1. Now A=1 and clk=0, the first 1P-2N structures output C=0. For the second 1P-2N structure, A=1 and clk=1, so its output D=0. Now C=0 and T=0, therefore, C-element circuits output is B=0, so output Q becomes Q=1. Consequently, there is no change in the output state.

Now again we can assume that the initial state of nodes A and B to be A=B=1, C=D=0, output Q=0 and clk=0. If any fault occurs at the node A, then the value of the node A will be changed from 1 to 0. For the first 1P-2N structure, A=0 and clk=0 therefore, C=1. For the second 1P-2N structure, A=0 and clk=1, for this input combination its output goes to the high impedance state means in its previous state that is D=0. Now C=1 and D=0, so C-element circuits output also goes to the high impedance, B=1 and output Q=0, consequently, again there is no change in the output state. As a matter of fact, the erroneous input is left out without any penalty in time, area and power consumption. Consequently, the proposed novel GR-DET-FF is completely glitch resistant and has high speed and high efficiency as compared to other designs.

IV. COMPARATIVE ANALYSIS

The comparative analysis of the proposed GR-DET-FF, performed through the SPICE simulator with Predictive Technology Model (PTM) 32 nm CMOS technology [19] with a power supply of 1V. Existing DET-FF designs, which are discussed in the background study section, are also performed. The channel lengths of all of the transistors are fixed to 32 nm. To simulate the circuit, the temperature is set to 27 ºC and the clock frequency is fixed to 500 MHz. The performance evaluation results are reported in table I.

Table I: Comparative analysis of different DET-FF designs

DET-FF	TSPC [9]	LG_C [15]	AGF_DET_FF [18]	Proposed Design
$P_{avg.\ cons.}$ (µw)	8.425	9.898	5.534	3.246
$t_{p(D-Q)}$ (ps)	66.336	85.297	41.164	30.62
$t_{p(CLK-Q)}$ (ps)	44.213	64.281	30.013	26.12
PDP (fJ)	0.559	0.844	0.228	0.099
No. of transistors	38	28	16	16

The delay, Power and power-delay-product comparisons, expressed in table I, calculated and verified for all DET-FF designs. We note that the GR-DET-FF has the lowest power consumption, lowest propagation delay, lowest Power Delay Product (PDP) and less number of transistors as compared to existing DET-FF designs [9, 15, 18]. Consequently, the proposed GR-DET-FF has high efficiency in comparisons with other discussed DET-FF designs. Comparative analysis of power, delay and area for different glitch free DET-FF designs is shown in fig. 5, which reports that the proposed novel circuit design has the lowest power, smallest area and lower propagation delay in comparison with other existing designs.

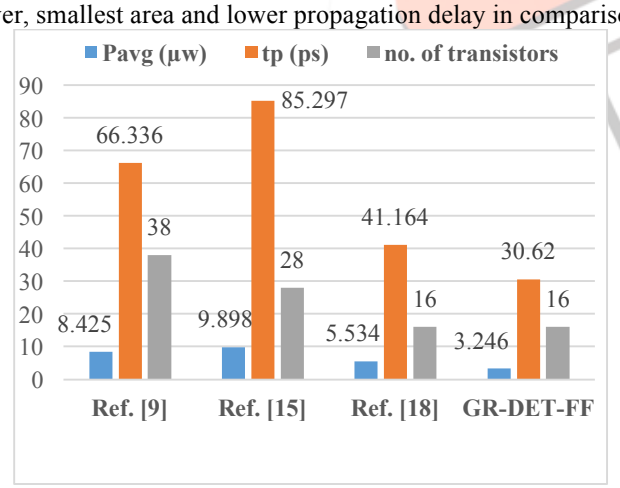

Fig. 5 Power, delay and area comparisons of different proposed designs

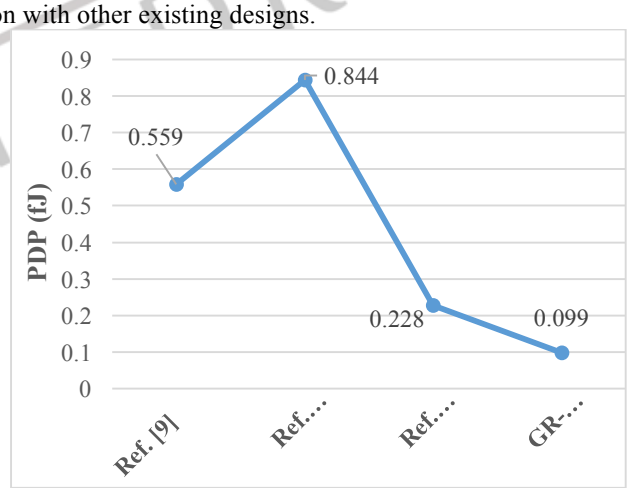

Fig. 6 PDP comparison of different proposed designs

The PDP analysis is shown in fig. 6, which shows that the presented GR-DET-FF has lowest PDP. The average power consumption analysis of GR-DET-FF presented in figures 7, 8, 9 and 10.

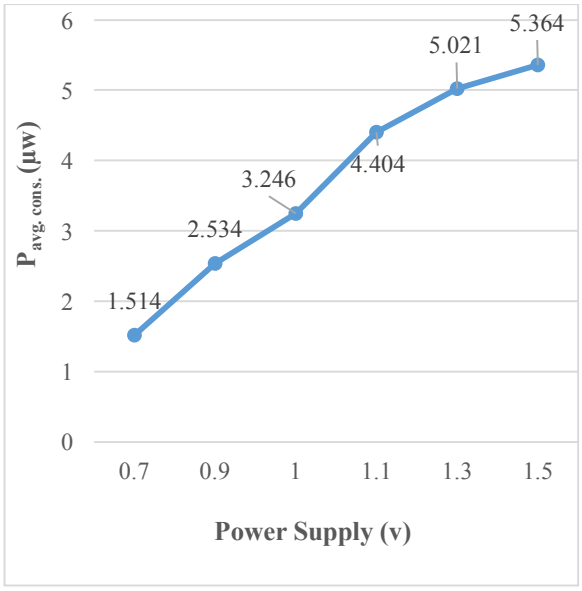

Fig. 7 Average power consumption analysis with different power supply.

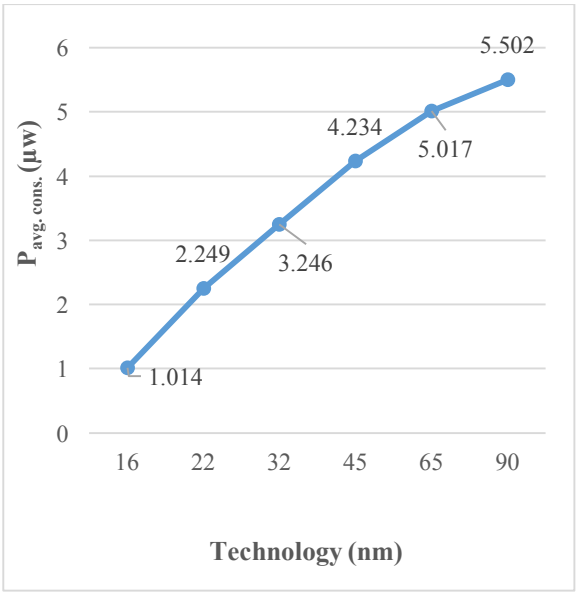

Fig. 8 Average power consumption analysis with different technologies.

The power consumption increases with the power supply increment and also increases with different technologies. Again the power consumption increases with temperature increment and also increases with frequency increment. Also, input and glitch free output waveforms are shown in fig. 11.

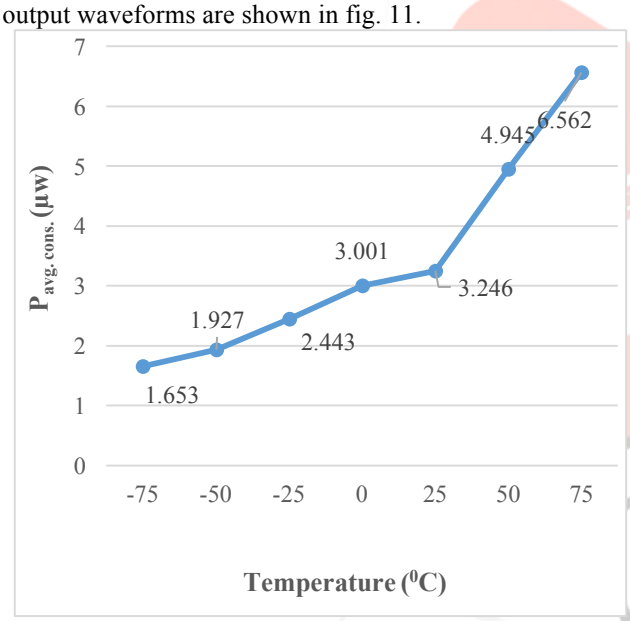

Fig. 9 Average power consumption analysis with different temperatures.

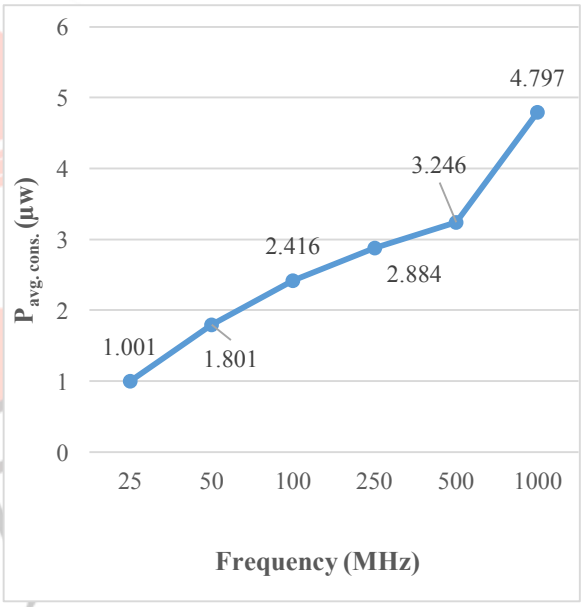

Fig. 10 Average power consumption analysis with different frequencies.

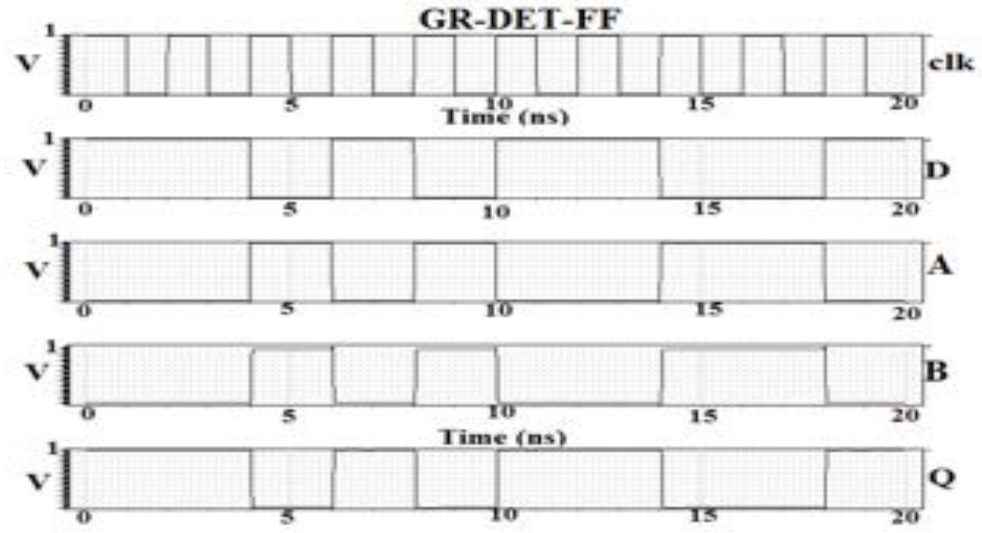

Fig. 11 Simulated Input-Output waveforms of novel GR-DET-FF.

V. CONCLUSION

We have proposed the robust low power and low glitch GR-DET-FF design. For performance improvement, we have combined 1P-2N structure with the C-element circuit. To reduce the input loading, the two structures are merged to share transistors connected with data input. The proposed GR-DET-FF has the lowest power consumption and lowest PDP as compared to discussed existing DET-FF designs. The proposed design has the smallest number of transistors, consequently, occupied small area and has the lowest delay, therefore, provide the high speed and high efficiency.

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