Design of 8 Bit CAM Using MSML Design

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Abstract - Proposed Paper contains Master slave match line (MSML) architecture which is implemented in traditional CAM cell for storing 8 bit of data. Objective of the proposed methodology is to improve searching speed with less power consumption. MSML operation depends on two things one is Master Match Line (MML) and slave match line (SML). Design is performed using SPICE in 22nm technology. Various parameters such as temperature, power and delay are calculated for MSML design. Proposed methodology power consumption is found to be 598mw with delay of 5.98ns for 22nm technology.

Index Terms—CAM cell Architecture, MSML Architecture

I.I NTRODUCTION

Memory plays an important role in design of many processors. There are many types of memory available. They are RAM , ROM & CAM. In case of RAM, user will give the address of the data and RAM will return the data present in that address.CAM architecture is constructed in such a way that when user gives the data CAM will look through entire memory to detect the data present.CAM has advantages and disadvantages. Advantage of CAM cell is that it operates in single clock cycle because of which searching speed is more when compared to RAM .Power consumption is less for CAM. However disadvantage of CAM is complex circuit to design. Memory has significant effect on the execution of the chip. Many techniques for CAM architecture has been implemented previously such as CAM architecture using Pipelining [1] ,Match Line Design [2], Voltage Swing [3] and Pipeline using Match Line design [4].

(1) CAM cell is implemented using pipelining concept. Here Searching speed is less and power consumption is also more.
(2) An implementation of the Match Line design is carried out for 4 bit CAM.
(3) Voltage swing inside the Match Line is reduced.
(4) Power is estimated for CAM architecture using pipeline module.

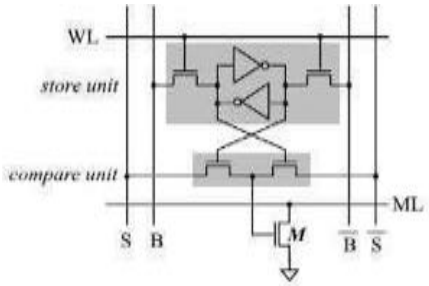
To overcome these power consumption and improved searching speed, proposed technique called Master Slave Match Line (MSML) is implemented in CAM architecture. Fundamental idea behind this MSML architecture is to combine Master-slave architecture and Charge sharing technique thereby reducing the power consumption inside the Matchline. This paper is given as follows. Section 2 explains about the Conventional CAM architecture and MSML architecture. Section 3 explains about circuit level implementation of MSML architecture using 22nm technology. Section 4 explains about the simulation results for MSML architecture. Conclusion are given in Section 5.

II. ARCHITECTURE OF MASTER SLAVE MATCH LINE:

Unlike conventional Content addressable memory which uses one match line to pursuit task, MSML configuration utilizes one Master Match Line (MML) and several Slave Match Line (SML) to perform searching. Power consumed by match line is reduced because of charge shared by mismatched SML. Fig.1.explains about the CAM architecture.

Fig.1.CAM Architecture

CAM architecture consists of two units, Store unit and compare unit. Store unit consists of 6T RAM cell in which whatever data is loaded in bitline (B) are getting stored. Comparison unit consists of xor logic which compares the data present in the store unit and the input data that is loaded in Serial Line (S). Pull down transistor (M) is present in CAM architecture mainly



to make Match Line charge or discharge to either VDD or GND.

MSML Architecture:

There are three operations that is performed in MSML architecture. They are explained below.

Search operation:

In Normal CAM cell, there are two modes of operation available. In precharge phase both FML & MML values are set to high value. In Evaluation Phase when one or more SML are mismatched, FML values goes low.

Precharge Phase:

When PRE=1, the values of MML and FML are set to high and all the SMLs gets the value zero. Because of pull down transistor going to low, charge sharing path gets separated.

Match Evaluation:

In the Evaluation Phase, PRE=0 and data are loaded in the search line. There are two parts in cam cell design .SML1 and SML2 .Due to this two parts there is possibility of four outcomes in this phase. Exact match occurs only when both SML's are same. Different cases are explained below.

Case1 (SML's Match)

In this condition Both FML & MML are set to high values and the SML1,SML2 are set to low value. (i.e.Zero).Under this condition there is no conduction in charge sharing path.

Case2 (One of the SML Match)

Under this phase, Either one of the SML is matched, Suppose if SML1 is matched and SML2 is in mismatch.one of the transistor gets on because of which voltage of SML2 gets increased due to charge is distributed to SML2 by MML. Once charge sharing gets completed both MML and SML2 will have same voltage values.

The final voltage equation due to charge sharing concept is given in the equation (1)

Where CMML and CSML2 are the capacitances of MML and SML2 individually and VMML is the underlying voltage of MML.

$$Vb = \frac{CMML}{CMML + CSML2} VMML \cong \frac{2}{3} VMML \qquad (1)$$

Case3 (SML'S Mismatch)

If both SML1 and SML2 are mismatched, Charge sharing path conducts and because of this MML charge gets distributed to both SML.

The final voltage equation is given in the equation (2).

$$Vb = \frac{CMML}{CMML + CSML1 + CSML2} VMML \cong \frac{1}{2} VMML \qquad (2)$$

Case 2 consumes less power when compared with Case 3. MSML design using traditional CAM cell is given in Fig.2.

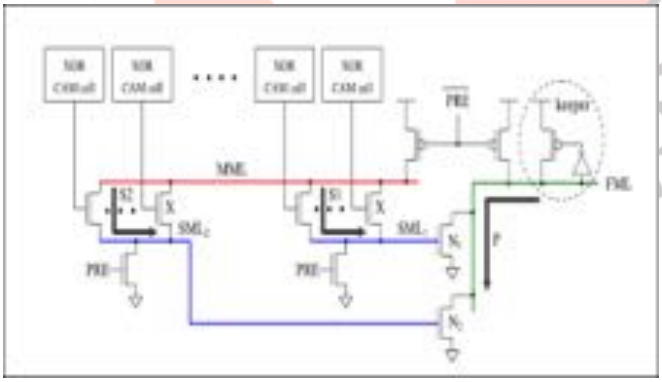


Fig.2.CAM Cell using MSML Design

III. POWER AND DELAY CALCULATION:

For CAM cell performance depends on Power, Speed. Various parameters such as temperature, delay and Power are calculated for various type of CAM cell.

Power Estimation:

There are two types of power in every circuit. They are static or leakage power and Dynamic power. Static power is due to leakage current. Dynamic power is due to switching between two nodes.

Dynamic power is determined from the condition (3) as follows.

VDD is the supply voltage and αJ is toggling probability.

$$\text{Power} = V_{DD}^2 * f * \sum_{i=1}^{j} \alpha_j * C_j \qquad (3)$$

CJ is the node capacitance and f is the frequency of input signal (clock).

Delay Estimation:
Delay calculation is explained using elmore delay model. RC circuit is given in Fig.3.

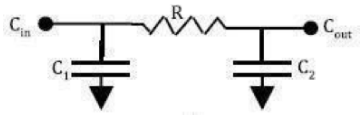


Fig.3.RC Circuit

Propogation Delay is calculated using Equation 4.

$$tpd = 0.69R\,(C1+C2) \qquad (4)$$

IV. CIRCUIT LEVEL IMPLEMENTATION OF MSML DESIGN:

CAM Cell configuration is executed in SPICE level as appeared in Fig. 4. Configuration is done in 22nm innovation to examine the execution in innovation scaling situations.

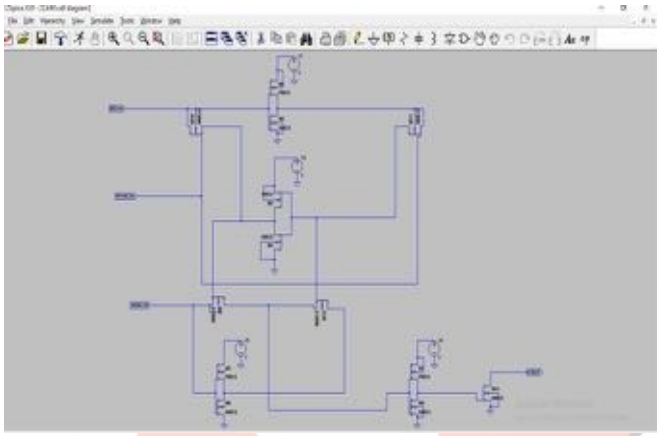
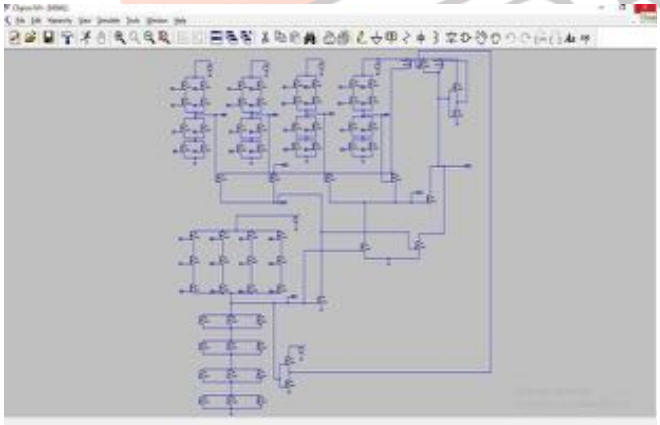


Fig.4.Circuit Level implementation of CAM cell

Fig.4 shows circuit diagram of Traditional CAM cell using SPICE. Fig.5. shows Circuit diagram of proposed MSML design.

Fig.5.Circuit diagram of MSML architecture



V. SIMULATION RESULTS:

Simulation results for proposed MSML design using 22nm is explained in Fig.6.

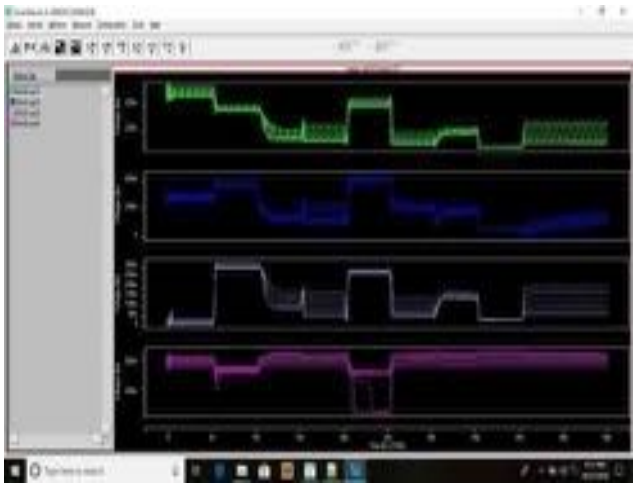


Fig.6.Waveform for MSML architecture at different temperatures

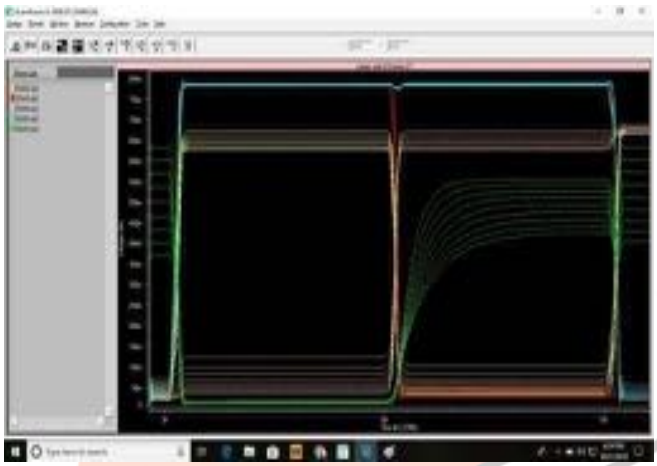


Fig.7.Characteristic Waveform of Master slave Match Line Design

The figure 7 portrays the simulation yield of MSML type CAM plan. Temperature is varied from 27ºC to 97°C for MSML design and power is calculated for every 10°C change in temperature. From the Waveform it is observed that from 27 to 37 degree the power consumption gets reduced from 598mw to 592mw with delay of 5.28ns. From 37 to 47 degree the power consumption is reduced from 592mw to 582mw with delay of 5.23ns. From 47 to 57 degree the power consumption is reduced from 582mw to 572mw with delay of 5.25ns. From 57 to 67 degree the power consumption is reduced from 572mw to 568mw with delay of 5.31ns. From 67 to 77 degree the power consumption is reduced from 568mw to 563mw with delay of 5.33ns. From 77 to 87 degree the power consumption is reduced from 563mw to 560mw with delay of 5.35ns. From 87 to 97 degree the power consumption is reduced from 560mw to 534mw with delay of 5.40ns.

Table I shows control utilization and delay in 22nm for 1V supply for different temperature From 27ºC to 37ºC, Power is diminished from 598 to 592 at 5.28ns. From the table it is seen that as the temperature expands control esteem gets decreased at various timespan.

CAMTemp (°C)	Time (ns)	Power (mw)
27ºC	5.28	598
37ºC	5.23	592
47ºC	5.25	582
MSML57ºC	5.31	572
67ºC	5.33	568
77ºC	5.35	563
87ºC	5.40	560
97ºC	5.45	534

CONCLUSION

MSML configuration conveys most productive execution among other CAM cell plans is obvious from power examination table. MSML configuration devours 10% less power than NOR Architecture in 22nm and NAND architecutre expends 7% more power than MSML plan in 22nm under different temperatures. This work can be connected to manufacture low power fast memory which can improve the speed.

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