A Grid-Connected Dual Voltage Source Inverter with Power Quality Enhancement in Micro Grid

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Abstract **- This paper presents a Dual Voltage Source Inverter (DVSI) scheme to enhance the power quality and reliability of the micro grid system. The proposed scheme is comprised of two inverters, which enables the micro grid to exchange power gene rated by the Distributed Energy Resources (DER) and also to compensate the local unbalanced and nonlinear load. The control algorithms are developed based on Instantaneous Symmetrical Component Theory (ISCT) to operate DVSI in grid sharing and grid injecting modes. The proposed scheme has increased reliability, lower bandwidth requirement of the main inverter, lower cost due to reduction in filter size, and better utilization of micro-grid power while using reduced dc-link voltage rating for the main inverter. These features make the DVSI scheme a promising option for micro grid supplying sensitive loads. The topology and control algorithm are validated through extensive simulation and experimental results.**

keywords **- Grid-connected inverter, instantaneous symmetrical component theory (ISCT), micro grid, Power quality.**

INTRODUCTION

In the present scenario the technological advancements and environmental concerns lead the power system to a typical shift with more renewable energy sources integrated to the network by means of distributed generations (DG). These DG units with consequent control of local generation and storage facilities from a micro grid. In a micro grid, power from variable renewable energy sources such as fuel cells, photovoltaic (PV) systems, and wind energy systems are connected to grid and loads with power electronic converters. A grid interactive inverter plays a dominant role in interchanging power electronic converters. A grid connected inverter plays a main role in exchanging power from the micro grid to the grid and the connected load. This micro grid inverter can either work in a grid sharing mode while delivering a part of local load or in grid injecting mode, by injecting power to the main grid. Power quality maintenance is another major aspect that has to be concerned while main grid is connected by micro grid system. The growth of power electronic devices and electrical loads with unbalanced nonlinear currents has degraded the power quality in the power distribution network. Furthermore, if there is a significant amount of feeder impedance in the distribution network, the propagation of these harmonic currents distorts the voltage at the point of common coupling (PCC). At the same point, automation in industries has reached to a top level of sophistication; on the other hand plants like automobile manufacturing, chemical factories, and semiconductor manufacturing units require clean power. For serving these utilities, it is necessary to compensate nonlinear and unbalanced load currents.

Load compensation and power injection is done by grid interactive inverters in micro grid have been given in the literature. A single inverter system with power quality enrichment is discussed in. The key focus of this work is to understand dual functionalities in an inverter that would provide the amative power injection from a solar PV system and also works as an active power filter, compensating unbalances and the reactive power required by other loads connected to the system.

In, a voltage regulation and power flow control scheme for a wind energy system (WES) is proposed. A distribution static compensator (D STSTCOM) is not only utilized for voltage regulation but also for active power injection. This control scheme controls the power balance at the grid terminal through the wind fluctuations with sliding mode control. A multifunctional power electronic converter for the DG power system is explained in. this scheme has the capability to inject power generated by WES and also to work as a harmonic compensator. Most of the literature considered here in this area discuss the topologies and control algorithms to supply load compensation capability in the same inverter in addition to their active power injection. When a grid-connected inverter is used for both active power injections as well as for load compensation, the inverter capacity that can be utilized for achieving the preceding aim is decided by the existing instantaneous micro grid real power. Taking into account the case of a grid-connected PV inverter, the existing capacity of the inverter to supply the reactive power becomes less during the maximum solar insulation periods. At the same time, the reactive power to regulate the PCC voltage is very much needed during this time. It indicates that providing multi functionalities in a single inverter degrades either the real power injection or the load compensation capabilities.

This paper demonstrates a dual voltage source inverter scheme (DVSI), in which the power generated by the micro grid is injected as real power by the main voltage source inverter (MVSI) and reactive, harmonic, and unbalanced load compensation is performed by auxiliary voltage source inverter (AVSI). This has an advantage that the rated capacity of MVSI can always be used to inject real power to the grid, if sufficient renewable power is available at the dc link. In the DVSI scheme, as total load power is supplied by two inverters, power losses across the semiconductor switches of each inverter are reduced. This increases its reliability as compared to a single inverter with multifunctional capabilities. Also, smaller size modular inverters can operate at high switching frequencies with a reduced size of interfacing inductor, the filter cost gets reduced. Moreover, as

the main inverter is supplying real power, the inverter has to track the fundamental positive sequence of current. This reduces the bandwidth requirement of the main inverter. The inverters in the proposed scheme use two separate dc links. Since the auxiliary inverter is supplying zero sequence of load current, a three-phase three-leg inverter topology with a single dc storage capacitor can be used for the main inverter. This in turn reduces the dc-link voltage requirement of the main inverter. Thus, the use of two separate inverters in the proposed DVSI scheme provides increased reliability, better utilization of micro grid power, reduced dc grid voltage rating, less bandwidth requirement of the main inverter, and reduced filter size. Control algorithms are developed by instantaneous symmetrical component theory (ISCT) to operate DVSI in grid-connected mode, while con-sidering nonstiff grid voltage. The extraction of fundamental positive sequence of PCC voltage is done by *dq*0 transformation. The control strategy is tested with two parallel inverters connected to a three-phase four-wire distribution system. Effectiveness of the proposed control algorithm is validated through detailed simulation results.

I.DUAL VOLTAGE SOURCE INVERTER

A. System Topology

A Topology of the structure, the proposed DVSI topology is appeared in Fig. It comprises of an neutral point clamped (NPC) inverter to take in AVSI and a three-leg inverter for MVSI. These are associated with grid at the PCC and providing a nonlinear and unbalanced load. The primary work of the AVSI is to reward the reactive, harmonics, and unbalance segments in load streams. Here, load streams in three stages are given by ila, ilb, and ilc, individually. Likewise, ig(abc), iμgm(abc), and iμgx(abc) demonstrate grid streams, MVSI ebbs and flows, and AVSI ebbs and flows in three stages, separately. The dc link of the AVSI infers a split capacitor topology, with two capacitors C1 and C2. The MVSI conveys the accessible power at distributed vitality asset (DER) to grid. The DER can either be a dc source or an air conditioner source with dc link coupled by rectifier.

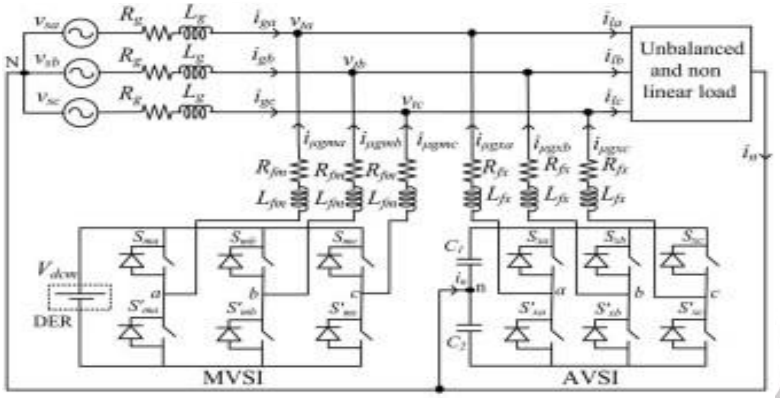


Fig. 1. Topology of proposed DVSI scheme.

Typically, sustainable power sources like energy components and PV create power at variable low dc voltage, while the variable speed wind turbines produce power at variable air conditioning voltage. Subsequently, the power created from these sources use a power molding stage before it is associated with the contribution of MVSI. In this investigation, DER is being spoken to as a dc source. An inductor filter is utilized to dispose of the high-frequency exchanging segments produced because of the exchanging of power electronic switches in the inverters. The system considered in this investigation is expected to have some measure of feeder resistance Rg and inductance Lg. Because of the nearness of this feeder impedance, PCC voltage is influenced with harmonics. Segment III depicts the extraction of crucial positive arrangement of PCC voltages and control strategy for the reference current generation of two inverters in DVSI scheme.

A. Design of DVSI Parameters

AVSI*:* The important parameters of AVSI like dc-link voltage (V_{dc}), dc storage capacitors (C_1 and C_2), interfacing inductance ($Lf\ x$), and hysteresis band ($\pm hx$) are selected based on the design method of split capacitor DSTATCOM topology [16]. The dc-link voltage across each capacitor is taken as 1.6 times the peak of phase voltage. The total dc-link voltage reference (V_{dcref}) is found to be 1040 V.

Values of dc capacitors of AVSI are chosen based on the change in dc-link voltage during transients. Let total load rat-ing is *S* kVA. In the worst case, the load power may vary from minimum to maximum, i.e., from 0 to *S* kVA. AVSI needs to exchange real power during transient to maintain the load power demand. This transfer of real power during the transient will result in deviation of capacitor voltage from its reference value. Assume that the voltage controller takes *n* cycles, i.e., *nT* seconds to act, where *T* is the system time period. Hence, maximum energy exchange by AVSI during transient will be *nST* . This energy will be equal to change in the capacitor stored energy. There

$$\frac{1}{2}C_1(V_{\mathrm{dcr}}^2 - V_{\mathrm{dc1}}^2) = nST \qquad (1)$$

where V_{dcr} and V_{dc1} are the reference dc voltage and maximum permissible dc voltage across C_1 during transient, respectively. Here, S = 5 kVA, V_{dcr} = 520 V, V_{dc1} = 0.8*V_{dcr} or 1.2 * V_{dcr},

n = 1, and T = 0.02 s. Substituting these values in (1), the dc-link capacitance (C_1) is calculated to be 2000 μF. Same value of capacitance is selected for C_2.

The interfacing inductance is given by

$$L_{fx} = \frac{1.6\,V_m}{4\,h_x f_{\max}}. \qquad (2)$$

Assuming a maximum switching frequency ($f_{\max}$) of 10 kHz and hysteresis band (h_x) as 5% of load current (0.5 A), the value of L_{fx} is calculated to be 26 mH.

1) ***MVSI****:* The MVSI uses a three-leg inverter topology. Its dc-link voltage is obtained as 1.15 * V_{ml}, where V_{ml} is the peak value of line voltage. This is calculated to be 648 V. Also, MVSI supplies a balanced sinusoidal current at unity power factor. So, zero sequence switching harmonics will be absent in the output current of MVSI. This reduces the filter requirement for MVSI as compared to AVSI . In this analysis, a filter inductance (L_{fm}) of 5 mH is used.

B. Points of interest of the proposed Scheme

The different points of interest of the proposed DVSI conspire over a solitary inverter plot with multifunctional abilities are talked about here as takes after:

1) **Increased Reliability**: DVSI plot has expanded unwavering quality, because of the lessening in disappointment rate of segments and the diminishing in system down time cost. In this plan, the aggregate load current is shared amongst AVSI and MVSI and thus diminishes the disappointment rate of inverter switches. In addition, in the event that one inverter comes up short, the other can proceed with its activity. This decreases the lost vitality and consequently the down time cost. The lessening in system down time cost enhances the dependability.

2) **Reduction in Filter Size**: In DVSI plot, the current provided by every inverter is decreased and consequently the present rating of individual filter inductor diminishes. This decrease in current rating lessens the filter measure. Additionally, in this plan, hysteresis current control is utilized to track the inverter reference streams. As given in (2), the filter inductance is chosen by the inverter exchanging frequency. Since the lower current evaluated semiconductor gadget can be exchanged at higher exchanging frequency, the inductance of the filter can be brought down. This abatement in inductance additionally decreases the filter estimate

3) .**Improved Flexibility**: Both the inverters are bolstered from partitioned dc links which enable them to work freely, in this manner expanding the adaptability of the system. For example, if the dc link of the primary inverter is disengaged from the system, the load remuneration ability of the assistant inverter can in any case be used.

4) **Better Utilization of Micro grid Power***:* DVSI scheme helps to utilize full capacity of MVSI to transfer the entire power generated by DG units as real power to ac bus, as there is AVSI for harmonic and reactive power compensation. This increases the active power injection capability of DGs in micro grid

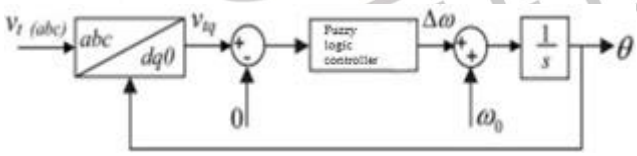
5) **Reduced DC-Link Voltage Rating***:* Since, MVSI is not delivering zero sequence load current components; a single capacitor three-leg VSI topology can be used. Therefore, the dc-link voltage rating of MVSI is reduced approximately by 38%, as compared to a single inverter system with split capacitor VSI topology.

II. CONTROL STRATEGY FOR DVSI SCHEME

A. Fundamental Voltage Extraction

The control calculation for reference current generation utilizing ISCT requires adjusted sinusoidal PCC voltages. Due to the nearness of feeder impedance, PCC voltages are misshaped. Thusly, the crucial positive sequence parts of the PCC voltages are removed for the reference current generation. To change over the misshaped PCC voltages to adjusted

Fig.2.Control strategy of DVSI Scheme



$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \qquad (3)$$

where

$$C = \sqrt{\tfrac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

sinusoidal voltages, dq0 transformation is used. The PCC voltages in natural reference frame (vta, vtb, and vtc) are first transformed into dq0 reference frame as given by

With a specific end goal to get θ, an altered synchronous reference outline (SRF) stage bolted circle (PLL) is utilized.

The schematic outline of this PLL is appeared in Fig. 2. It principally comprises of a corresponding necessary (FUZZY) controller. In this PLL, the SRF terminal voltage in q-hub (vtq) is contrasted and 0 V and the blunder voltage along these lines acquired is given to the fuzzy controller. The frequency deviation Δω is then added to the reference frequency ω0 lastly given to the integrator to get θ. It can be demonstrated that, when, θ = ω0 t and by utilizing the Park's change network (C), q-hub voltage in dq0 outline ends up zero and consequently the PLL will be bolted to the reference frequency (ω0). As PCC voltages are mutilated, the changed voltages in dq0 outline (vtd and vtq) contain normal and wavering parts of voltages. These can be spoken to as

$$v_{td} = \overline{v}_{td} + \widetilde{v}_{td}, \quad v_{tq} = \overline{v}_{tq} + \widetilde{v}_{tq} \tag{4}$$

$$\begin{bmatrix} v^{+}_{ta1} \\ v^{+}_{tb1} \\ v^{+}_{tc1} \end{bmatrix} = C^{T} \begin{bmatrix} \overline{v}_{td} \\ \overline{v}_{tq} \\ 0 \end{bmatrix}. \tag{5}$$

where vtd and vtq represent the average components of vtd and vtq, respectively. The terms vtd and vtq indicate the oscillating components of vtd and vtq, respectively. Now the fundamental positive sequence of PCC voltages in natural reference frame can be obtained with the help of inverse dq0 transformation as given by These voltages v+ ta1, v+ tb1, an v
+ tc1 are used in the reference current generation algorithms, so as to draw balanced sinusoidal currents from the grid.

B. Instantaneous Symmetrical Component Theory

ISCT was created basically for unbalanced and nonlinear load pay by dynamic power filters. The system topology appeared in Fig. 3 is utilized for understandin .

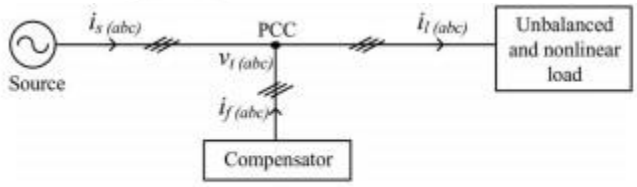


Fig. 3. Schematic of an unbalanced and nonlinear load compensation scheme.

The source neutral current must be zero. Therefore

$$i_{sa} + i_{sb} + i_{sc} = 0. \tag{6}$$

1) The phase angle between the fundamental positive sequence voltage (v+ ta1) and source current (isa) is φ

$$\angle v^{+}_{ta1} = \angle i_{sa} + \phi. \tag{7}$$

2) The average real power of the load (Pl) should be supplied by the source

$$v^{+}_{ta1}\, i_{sa} + v^{+}_{tb1}\, i_{sb} + v^{+}_{tc1}\, i_{sc} = P_l. \tag{8}$$

Solving the above three equations, the reference source currents can be obtained as
Where β = tan√ φ 3 . The term φ is the desired phase angle between the fundamental positive sequence of PCC voltage and

$$\begin{aligned} i^{*}_{sa} &= \left(\frac{v^{+}_{ta1} + \beta(v^{+}_{tb1} - v^{+}_{tc1})}{\sum_{j=a,b,c} v^{+2}_{tj}} \right) P_l \\ i^{*}_{sb} &= \left(\frac{v^{+}_{tb1} + \beta(v^{+}_{tc1} - v^{+}_{ta1})}{\sum_{j=a,b,c} v^{+2}_{tj}} \right) P_l \\ i^{*}_{sc} &= \left(\frac{v^{+}_{tc1} + \beta(v^{+}_{ta1} - v^{+}_{tb1})}{\sum_{j=a,b,c} v^{+2}_{tj}} \right) P_l \end{aligned} \tag{9}$$

source current. To achieve unity power factor for source current, substitute β = 0 in (9).
CThus, the reference source currents for three phases are given by

$$i^{*}_{s(abc)} = \left(\frac{v^{+}_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}} \right) P_l \tag{10}$$

where i ∗ sa, i ∗ sb, and i ∗ sc are fundamental positive sequence of load currents drawn from the source, when it is supplying an average load power Pl. The power Pl can be computed using a moving average filter with a window of one-cycle data points as given below

$$P_l = \frac{1}{T} \int_{t_1 - T}^{t_1} (v^{+}_{ta1}\, i_{la} + v^{+}_{tb1}\, i_{lb} + v^{+}_{tc1}\, i_{lc}) dt \tag{11}$$

Where t1 is any arbitrary time instant. Finally, the reference currents for the compensator can be generated as follows:

$$i^{*}_{f\,(abc)} = i_{l\,(abc)} - i^{*}_{s\,(abc)}. \tag{12}$$

Condition (12) can be utilized to create the reference filter streams utilizing ISCT, when the whole load dynamic

III. Control of DVSI

Control technique of DVSI is created such that grid and MVSI together offer the dynamic load power, and AVSI supplies rest of the power segments requested by the load. 1) Reference Current Generation for Auxiliary Inverter: The dc-link voltage of the AVSI ought to be kept up consistent for appropriate task of the helper inverter. DC-link voltage variety happens in helper inverter because of its exchanging and ohmic misfortunes. These misfortunes named as Ploss ought to likewise be provided by the grid. An articulation for Ploss is determined depending on the prerequisite that normal dc capacitor current is zero to keep up a steady capacitor voltage. The deviation of normal capacitor current from zero will reflect as an adjustment in capacitor voltage from an enduring state esteem. A fuzzy controller is utilized to produce Ploss term as given by

$$P_{\text{loss}} = K_{Pv}\, e_{\text{vdc}} + K_{Iv} \int e_{\text{vdc}} dt \qquad (13)$$

Where evdc = Vdcref − vdc, vdc represents the actual voltage sensed and updated once in a cycle. In the above equation, KP v and KIv represent the proportional and integral gains of dc-link fuzzy controller, respectively. The Ploss term thus obtained should be supplied by the grid, and therefore AVSI reference currents can be obtained as given in (14). Here, the dc-link voltage fuzzy controller gains are selected so as to ensure stability and better dynamic response during load change

$$i^{*}_{\mu gxa} = i_{la} - \left(\frac{v^{+}_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}})$$
$$i^{*}_{\mu gxb} = i_{lb} - \left(\frac{v^{+}_{tb1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}) \qquad (14)$$
$$i^{*}_{\mu gxc} = i_{lc} - \left(\frac{v^{+}_{tc1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)(P_l + P_{\text{loss}}).$$

2) Reference Current Generation for Main Inverter: The MVSI supplies balanced sinusoidal currents based on the available renewable power at DER. If MVSI losses are neglected, the power injected to grid will be equal to that available at DER (Pμg). The following equation, which is derived from ISCT can be used to generate MVSI reference currents for three phases (a, b, and c)

$$i^{*}_{\mu gm(abc)} = \left(\frac{v^{+}_{t(abc)1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right) P_{\mu g} \qquad (15)$$

Where Pμg is the available power at the dc link of MVSI.The reference currents obtained from (14) to (15) are tracked by using hysteresis band current controller (HBCC). HBCC schemes are based on a feedback loop, usually with a two-level

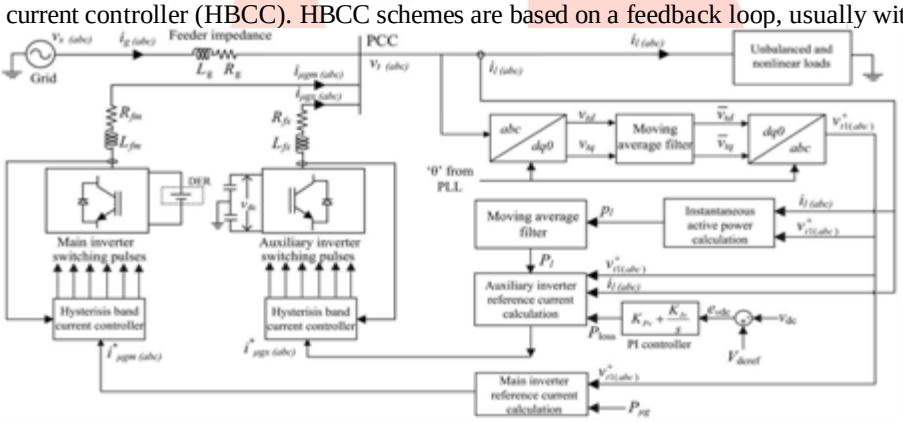


Fig 4.Control strategy of DVSI

Comparator. This controller has the advantage of peak current limiting capacity, good dynamic response, and simplicity in implementation. A hysteresis controller is a high-gain proportional controller. This controller adds certain phase lag in the operation based on the hysteresis band and will not make the system unstable. Also, the proposed DVSI scheme uses a first-order inductor filter which retains the closed- loop system stability. The entire control strategy is schematically represented in Fig.3.4. Applying Kirchhoff's current law (KCL) at the PCC in Fig. 3.4

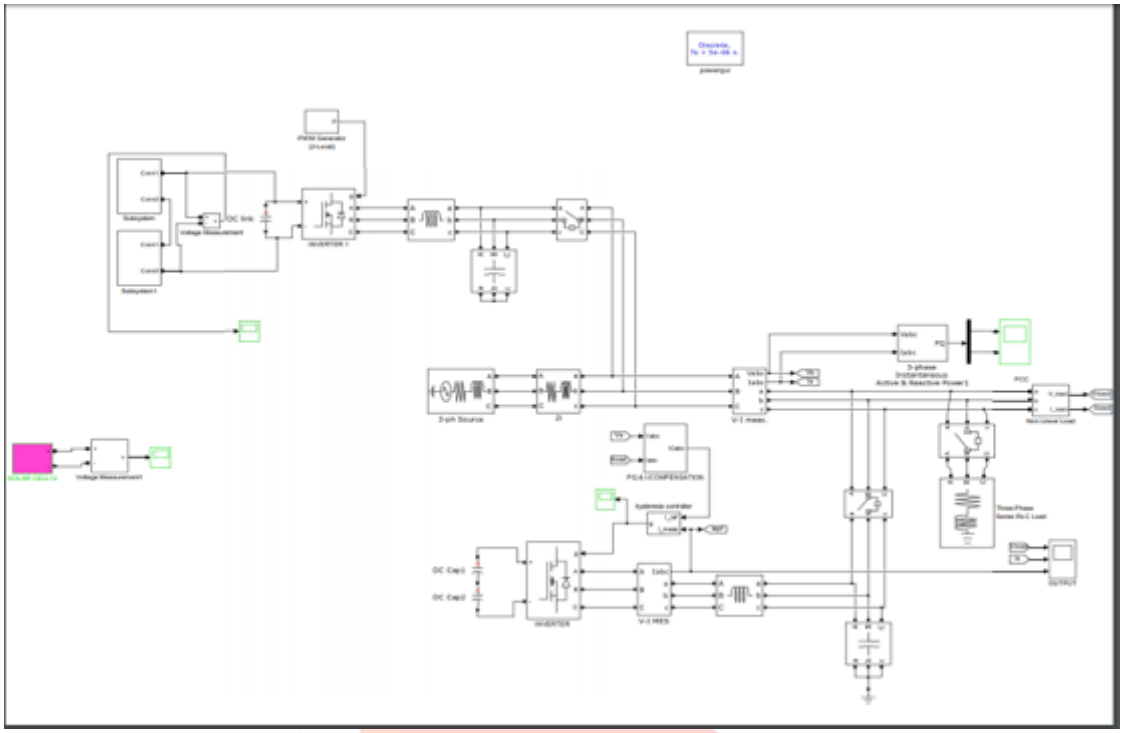
By using (14) and (16), an expression for reference grid current in phase-a (i ∗ ga) can be obtained as

$$i_{\mu gxj} = i_{lj} - (i_{gj} + i_{\mu gmj}), \quad \text{for } j = a, b, c. \qquad (16)$$
$$i^{*}_{ga} = \left(\frac{v^{+}_{ta1}}{\sum_{j=a,b,c} v^{+2}_{tj}}\right)[(P_l + P_{\text{loss}}) - P_{\mu g}]. \qquad (17)$$

It can be observed that, if the quantity (Pl + Ploss) is greater than Pμg, the term [(Pl + Ploss) − Pμg] will be a positive quantity, and i ∗ ga will be in phase with v+ ta1. This operation can be called as the grid supporting or grid sharing mode, as the total load power demand is shared between the main inverter and the grid. The term, Ploss is usually very small compared to Pl. On the other hand, if (Pl + Ploss) is less than Pμg, then [(Pl + Ploss) − Pμg] will be a negative quantity, and hence i ∗ ga will be in phase opposition with v+ ta1. This mode of operation is called the grid injecting mode, as the excess power is injected to grid.

IV. SIMULATION RESULTS AND ANALYSIS

In order to valid the effectiveness of the topology in mitigating the mismatch in dual voltage source inverter are simulated in MATLAB/Simulink environment. The simulated system is shown in Fig 4.1 and system specifications are listed in Table 1.



The simulated system is shown in Fig 5. And system specifications are listed in Table 1.

IV .1 SYSTEM PARAMETERS

Table 4.1 System parameters for Simulink model

Parameters	Values
Grid voltage	400 V(L–L)
Fundamental frequency	50 Hz
Feeder impedance	R_g = 0.5 Ω, L_g = 1.0 mH
AVSI	$C_1 = C_2$ = 2000 μF V_{dcref} = 1040 V Interfacing inductor, L_{fx} = 20 mH Inductor resistance, R_{fx} = 0.25 Ω Hysteresis band ($\pm h_x$) = 0.1 A
MVSI	DC-link voltage, V_{dcm} = 650 V Interfacing inductor, L_{fm} = 5 mH Inductor resistance, R_{fm} = 0.25 Ω Hysteresis band ($\pm h_m$) = 0.1 A
Unbalanced linear load	$Z_{la} = 35 + j19$ Ω $Z_{lb} = 30 + j15$ Ω $Z_{lc} = 23 + j12$ Ω
Nonlinear load	3 ϕ diode bridge rectifier with DC side current of 3.0 A
DC voltage controller gains	K_{Pv} =10, K_{Iv} = 0.05

IV. 2. SIMULATED OUTPUT OF GATE PULSES FOR DVSI

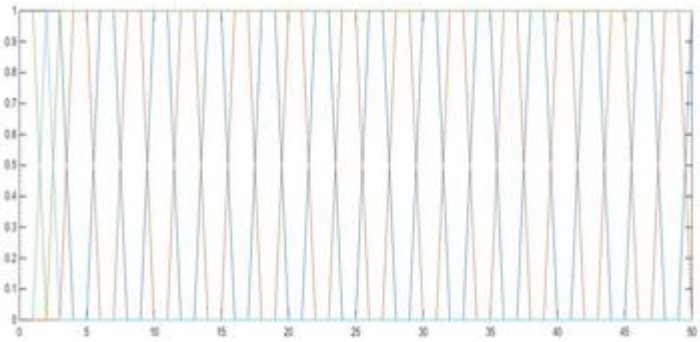


Fig 4.2 output waveforms for gate pulses inverter switches

IV. 3. SIMULATED DIAGRAM OF REAL AND REACTIVE POWER

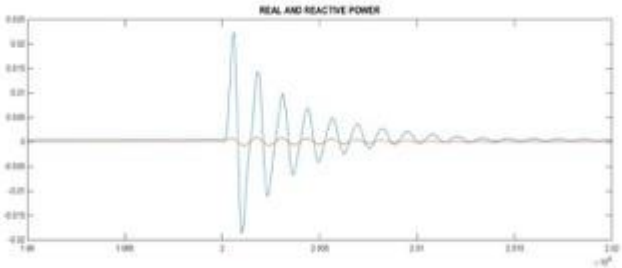


Fig 4.3 output waveforms for real and reactive power

IV.4. SIMULATED DIAGRAM OF DC LINK VOLTAGE

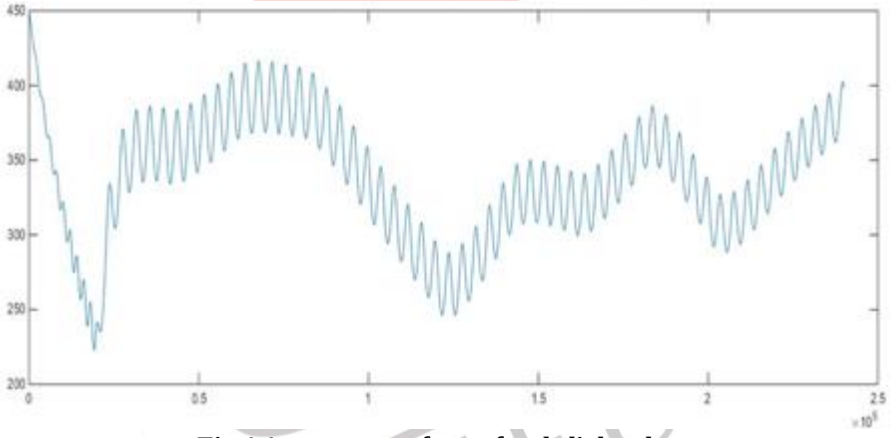


Fig 4.4 output waveforms for dc link voltage

IV.5. SIMULATED DIAGRAM OF GATE PULSES FOR INVERTER SWITCHES

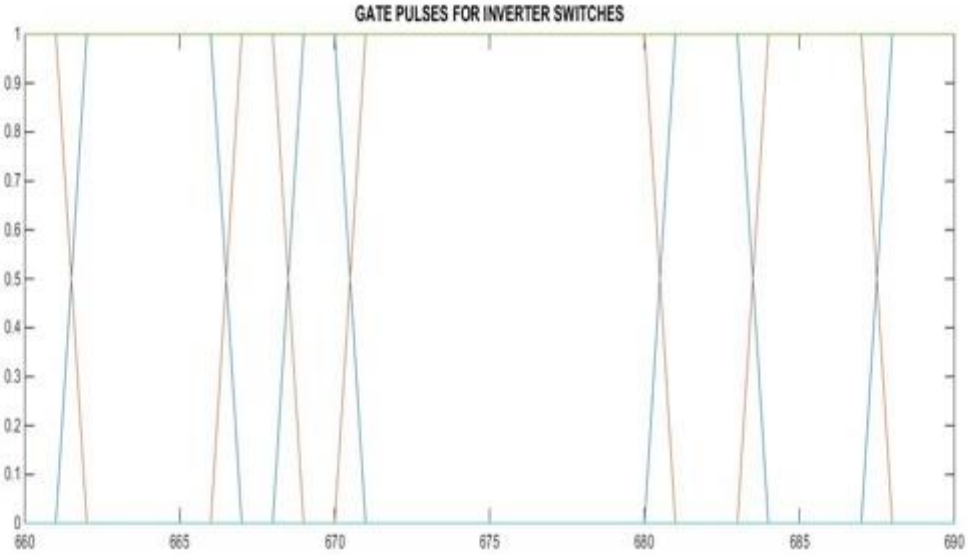


Fig 4.5 output waveforms for gate pulses for inverter switches

IV.6. SIMULATED DIAGRAM OF SOLAR CELL VOLTAGE

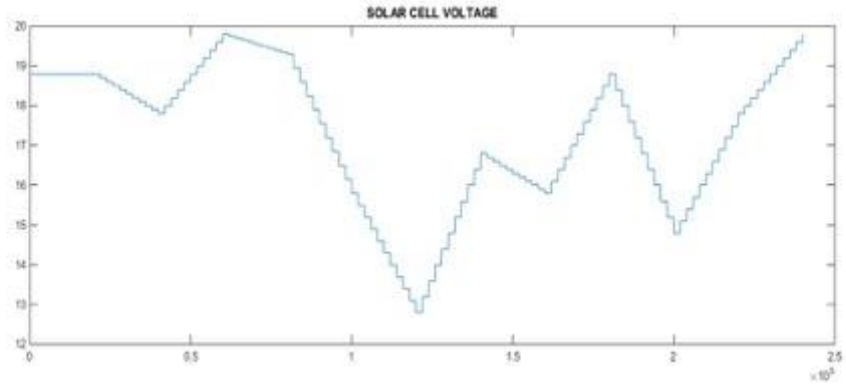


Fig 4.6 output waveforms for solar cell voltage

IV.7. SIMULATED DIAGRAM OF ACTIVE POWER

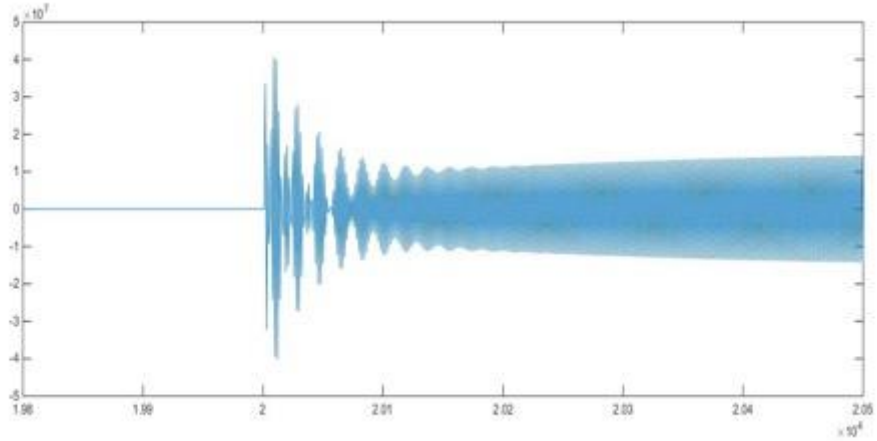


Fig 4.7 output waveform for active power

IV.8. SIMULATED DIAGRAM OF AVSI CURRENTS

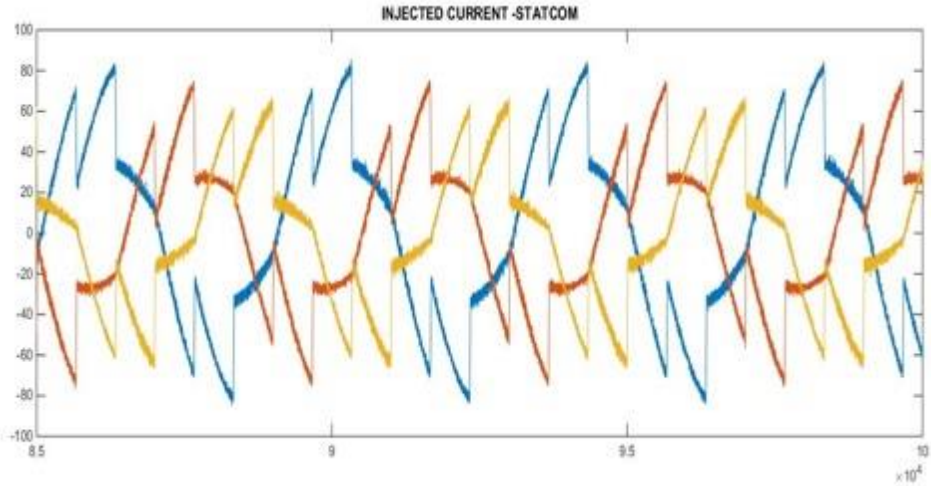


Fig 4.8. Output waveform for AVSI currents

Fig. 4.8 shows the plots of load currents (il(abc)), currents drawn from grid (ig(abc)), currents drawn from MVSI (iμg(abc)), and currents drawn from the AVSI (iμx(abc)), respectively. The load currents are unbalanced and distorted. The MVSI supplies balanced and sinusoidal currents during grid supporting and grid injecting modes. The currents drawn from grid are also perfectly balanced and sinusoidal, as the auxiliary inverter compensates the unbalance and harmonics in load currents.

V. CONCLUSION AND FUTURE SCOPE

The DVSI scheme proposed here for micro-grid systems with improved power quality. Control Algorithms are designed to generate reference currents for DVSI using ISCT. The proposed scheme has the capability to exchange power from distributed generators (DGs) and also to compensate the local unbalanced and nonlinear load. The performance of the proposed scheme

has been validated through simulation results. As compared to a single inverter with multifunctional capabilities, a DVSI has many advantages such as, lower cost due to the reduction in filter size, increased reliability and more utilization of inverter capacity to inject real power from DGs to micro-grid. Here the usage of three-phase, three-wire topology for the main inverter reduces the dc-link voltage requirement. Thus, a DVSI scheme is a suitable interfacing option for micro-grid supplying sensitive loads.

Researches have been going on to enhance the power quality in the grid system and also different types of inverters and different types of controllers which are based upon artificial intelligence techniques are undergoing. By this there are very much advantages than the present system

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