Investigation of Low Power Sample and Hold Circuit for Analog to Digital Converter

[1]Shivali
[1]student
[1]career point university Hamirpur h.p.

***Abstract* - Sample and hold circuit is an important part of an analog to digital converter. Being part of the ADC sample and hold is consuming high power. For low power consumption, various sample and hold circuits like Bootstrap Circuit, Low-Power Bootstrapped S/H Circuit without Multiplier Circuit & Boosted Driver Circuit are investigated for better performance and low power consumption at different frequency applications such as audio, Bluetooth and video frequencies. The effect of the low-power bootstrapped sample and hold (S/H) circuit without multiplier appears in the medium and high-frequency applications which reduce the power consumption without disturbing the signal-to-noise and distortion ratio (SNDR). All the introduced bootstrapped sample and hold (S/H) circuits were simulated using 90nm, 65nm & 45nm CMOS technology on LT Spice VIII. As a result, the planned low power bootstrapped sample and hold (S/H) circuit without multiplier save 78% to 93% for 90nm & 65nm while 84% to 94% for 45nm of the power consumption.**

***keywords* - ADC, Sample and Hold Circuit, Transmission Gate, Bootstrapped Circuit without Multiplier.**

I. INTRODUCTION

Analog-to-digital converter (ADC) is considered as one of the main electronic blocks in mixed-signal applications. It is used in low-frequency applications such as biomedical applications. Additionally, ADC becomes a bottleneck in digital signal processing applications which is used in medium frequency applications. It is also, used in high-frequency applications such as wireless communication. [1]

Sample and hold (S/H) circuit are one of the main significant analog building blocks, particularly in ADCs. It is the first block of the ADC components in which the input signal seen by the input of the S/H circuit. [2] Thus, it has a significant effect on the whole ADC performance which in turns will affect the overall system. At the circuit level in the low voltage operation. If the sum of the absolute value of the PMOS threshold voltage and that of the NMOS is greater than the supply voltage. The conventional analogue switches consist of transmission gates may not be fully turned on as they are under a higher voltage operation. The MOSFETs expected to be turned on may have extremely poor conductance and would limit the bandwidth of the circuits. Therefore, a bootstrapped technique is required which has been proved in. [3]

The accuracy of the S/H circuit depends mainly on the on-resistance of the sampling switch which will affect the switchlinearity. The bootstrapped S/H circuit keeps the gate-source voltage of the sampling transistor fixed at the supply voltage. This approach keeps the on-resistance small and constant and thus improve the switch linearity and reliability. The objective of this paper is to propose a modified low power bootstrapped S/H circuit for medium and high-frequency applications. [4]The transmission gate has been used as a switching element. The voltage operation will below guarantee the device reliability. It's worth noting that different sampling rates affect the signal to noise and distortion ratio (SNDR), speed and power consumption of the S/H circuit and the overall ADC. Section II illustrates the design of bootstrapped sampling MOS switches with two techniques. Simulation results are presented in section III. Section IV concludes the paper.

II. Design Of Bootstrapped Sampling MOS Switch

The bootstrapped circuit is considered a suitable circuit in low voltage operation. It is connected to the sampling transistor in S/H circuits. The bootstrapped circuit aims to make the on-resistance of the sampling transistor small to improve the on-conductance between the input and output of the sampling switch. This section will present the proposed modified low-power bootstrapped S/H circuit for medium and high-frequency applications. [4] In addition to that, different bootstrapped circuits which are connected to the S/H circuit using a transmission gate will be discussed and compared with the proposed circuit. The principle of the first bootstrapped technique is shown in Fig.1. The single NMOS transistor represents the sampling transistor switch. In the off-state, the gate is grounded, so the device is in cutoff mode. In the on-state, a constant voltage of (VDD) is applied across the gate-source terminals, and a low on-resistance is formed from drain to source independent of the input signal. If the gate voltage exceeds (VDD) for a positive input signal, none of the terminal-to-terminal device voltages exceeds (VDD). [5]

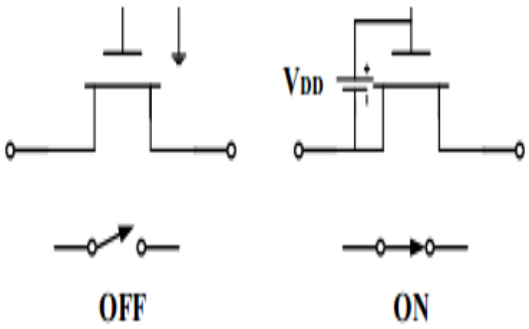


Fig1. Bootstrapped MOS switch

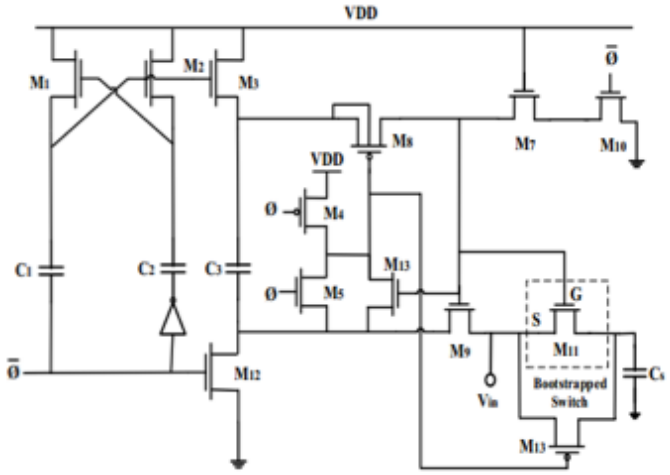


Fig2. S/H with bootstrapped circuit

Fig.2. shows the actual bootstrapped circuit. It operates on a single-phase clock Ø that turns the bootstrapped switch M11 on and off. When Ø is low, transistors M7 and M10 discharge the gate of M11 to ground and thus the bootstrapped circuit in the off phase. In this phase, (VDD) is applied across capacitor C3 by M3 and M12. This capacitor will act as the battery across the gate and source during the on phase. The job of M8 and M9 is to isolate the switch from C3 while it is charging. When Ø is high, the gate of M8 will be pulled down by M5, allowing charge from the battery capacitor C3 to flow onto gate G. This turns on both M9 and M11. M9 enables gate G to track the input voltage S shifted by (VDD), keeping the gate-source voltage constant regardless of the input signal. For example, if the source S is at (VDD), then gate G is at (2VDD); however, (VGS = VDD). The body (n-well) of M8 is connected to its source to repress latch-up. M7 and M13 are not functionally necessary but to improve the circuit reliability [6]. Device M7 reduces the (VDS) and (VGD) experienced by device M10 when Ø is low. The channel length of M7 can be increased to further improve its punch-through voltage. M13 ensures that (VGS8) does not exceed (VDD). M1, M2, C1 and C2 form a clock multiplier that enables M3 to charge C3 during the off phase. The capacitor C3 must be sufficiently large to supply charge to the gate of the switching device in addition to all parasitic capacitances in the charging path. Otherwise, charge sharing will significantly reduce the boosted voltage according to (2), where Cp is the total parasitic capacitance connected to the top plate of C3 while it is across the main switching device M11.

$$VG = VS + (C3 / (C3 + Cp))\,VDD \qquad (2)$$

When the bootstrapped switch is off, a Cds capacitor is formed between the drain and the source of the sampling transistor. It couples the input signal to the sampling capacitors which is composed by the drain-source capacitor of the sampling transistor and the routing parasitic capacitance. The coupling effect degrades the high-frequency performance because Cds induces unequal charges in the comparison cycles, which results in a dynamic offset. Therefore, two crosses coupled metal oxide metal (MOM) capacitors can be used to neutralize the effect. A dummy switch is an alternative solution to reduce the coupling effect. [7]

Bootstrapped have two other techniques to simulate/modify S/H circuit for better results.

i. **Low-Power Bootstrapped S/H Circuit without Multiplier Circuit**

The proposed modified low-power bootstrapped S/H circuit in Fig.3. It is the same as the S/H circuit with the bootstrapped circuit shown in Fig.2 but without the multiplier circuit. The multiplier circuit consists of M1, M2, C1 and C2. In Fig.3, the gate of the NMOS transistor M3 which is responsible for charging the capacitor C3 is biased by the multiplier circuit. On the other hand, in Fig.4, the NMOS transistor M3 is replaced by a PMOS transistor M3 and its gate is biased by the gate of the bootstrapped switch. M3 will charge C3 to (VDD) in the off-sate of the bootstrapped switch while in the on-state, the stored charge in C3 will be applied to the gate-source of the bootstrapped switch. Both circuits make the gate-source voltage of the bootstrapped switch constant and equal to the supply voltage independent of the input signal. This result in small and constant resistance of the sampling switch. The main important feature of the proposed modified low-power bootstrapped circuit is power consumption. It consumes less amount of power compared to the other presented bootstrapped S/H circuit in medium and high-frequency applications.[8] [9] In addition to that, the SNDR will not have degradation even in the high-frequency application when the

input signal is 7 M Hz. A simulation result shows the clock pulses formed on the gate of the sampling transistor M11 and the input signal in Fig.5. Furthermore, it shows a constant gate-source voltage of the sampling switch which independent of the input signal.

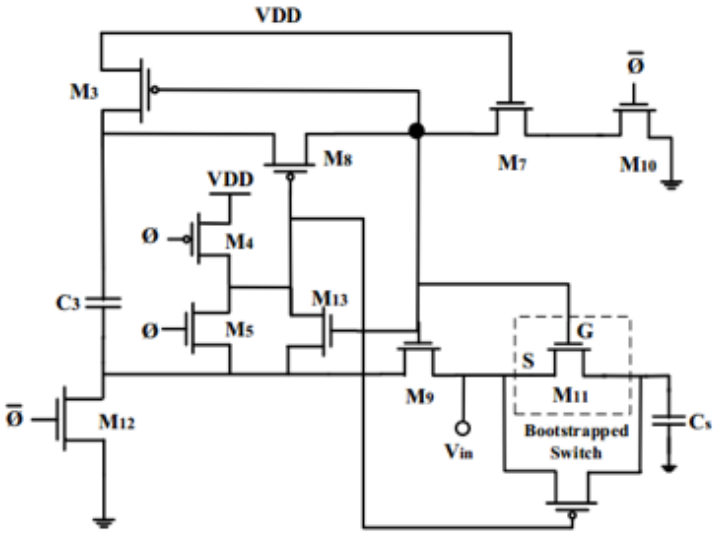


Fig3: Low-power bootstrapped S/H circuit without multiplier circuit.

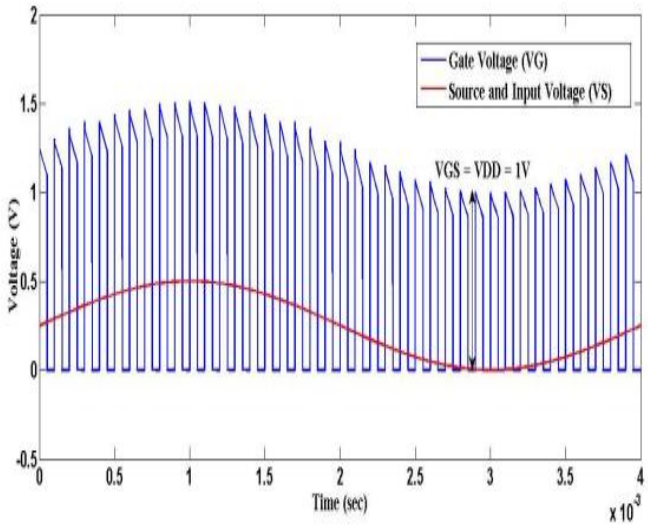


Fig4: M11 Input signal with the clock pulses formed on G for the low-power bootstrapped S/H circuit without multiplier circuit.

ii. The boosted driver circuit is used in sample and hold

Fig.5 shows the second type of bootstrapped technique which is the S/H circuit with the boosted driver. The principle of this circuit is to drive a boosted driver to the S/H circuit made of the transmission gate. It operates by applying a square wave input signal of (VDD). When Ø is high "off-state of the transmission gate S/H circuit", the bottom plate of C2 and the top plate of C1 are charged to (VDD). On the other hand, (VDD) will be applied to each second capacitor plates when Ø goes low "on-state of the transmission gate S/H circuit". Then, M3 will transfer the charges stored in C2 to the gate of MN with an inverted square wave output which is generated according to this equation.

$$Vgate\ MN = 2VDD * (C2/ (C2+CgateMN+Cparasitic)) \quad (1)$$

In other words, the boosted driver output is connected to the gate of the sampling transistor MN. It has an inverted periodical signal switching between (2VDD - ΔV) and the ground. (ΔV) the result from the charge sharing between the capacitor C2 and the parasitic capacitance at the gate of MN a simulation result shows the input clock pulses, the boosted driver output which is inverted boosted clock of 2V and the input voltage in Fig.6 The bandwidth of this circuit is (1/2 ∏ Ron CS), where Ron is the on-resistance of the sampling transistor MN. This technique has the advantages in keeping the on-resistance of the sampling switch small which will result in both low power the sampling switch small which will result in both low power x voltage of the sampling transistor MN is varying as shown in Fig.6 This will make the on-resistance of the sampling transistor MN varies. The effect of this problem will appear in the high-frequency applications where the sampling rate is high which will lead to high power consumption. [10] As a result, using the bootstrapped circuit shown in Fig.3 and Fig.4 ensures that the switch is operating in a manner consistent with the reliability constraints. Because of this switch, (VGS11) is relatively independent of the input signal. The importance of this circuit appears in minimizing the power consumption, especially in the high-frequency applications compared to the S/H circuit with the boosted driver as will be shown in the simulation results section. [10]

In addition to that, it keeps the on-resistance small constant value. The switch linearity is also improved and signal-dependent charge injection is reduced using the transmission S/H circuit. Thus, the bootstrapped circuit increase the settling speed and input bandwidth. [11]

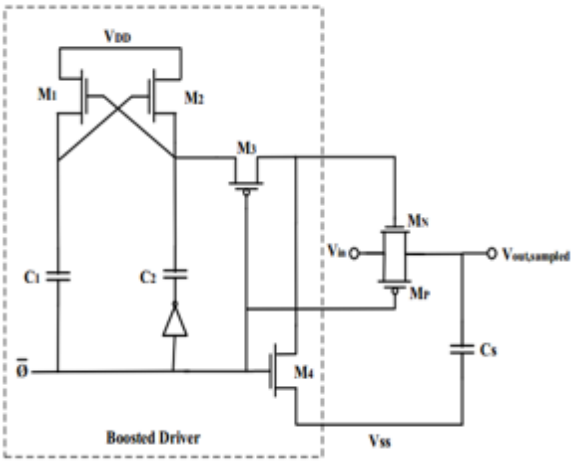


Fig5. S/H circuit with boosted driver

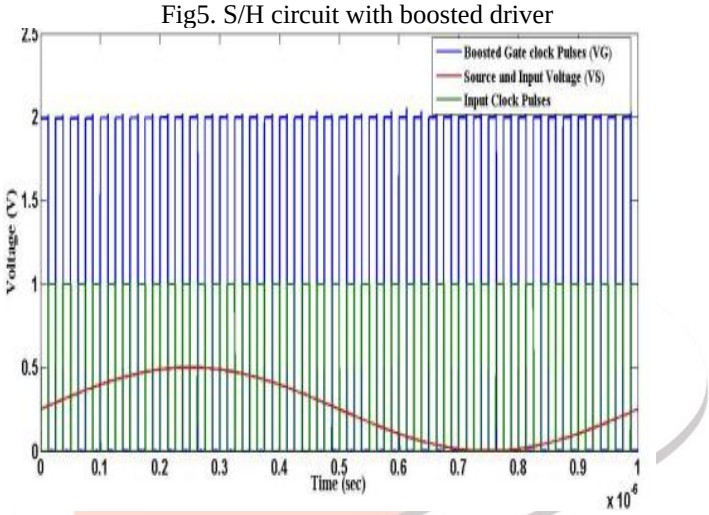


Fig6. Input clock pulses boosted driver output and the input voltage

III. SIMULATION RESULT

The three bootstrapped S/H circuit was simulated using 90nm, 65nm, and 45nm CMOS technology on LT Spice VIII. The input signal is a sine wave with 500 MVP-p amplitude for a 2V, 1.1V& 1V supply voltages respectively. They were tested under 20 kHz, 1 MHz and 7 MHz input signal frequencies. SNDR and the power consumption were measured for the bootstrapped S/H circuits. The sampled output voltage & the FFT for the low-power bootstrapped S/H circuits without multiplier are shown below. The remaining presented bootstrapped S/H circuits have the same shape of the sampled output voltage and the FFT spectrum. As a result, the low-power bootstrapped S/H circuits without multiplier achieves the minimum power consumption among the others without important SNDR degradation for medium and high-frequency applications. For that reason, it is the best candidate in term of lower power consumption and high SNDR.

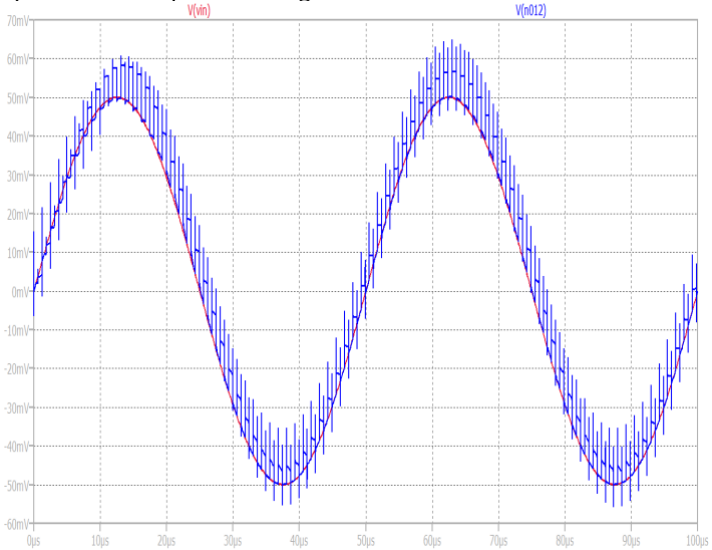
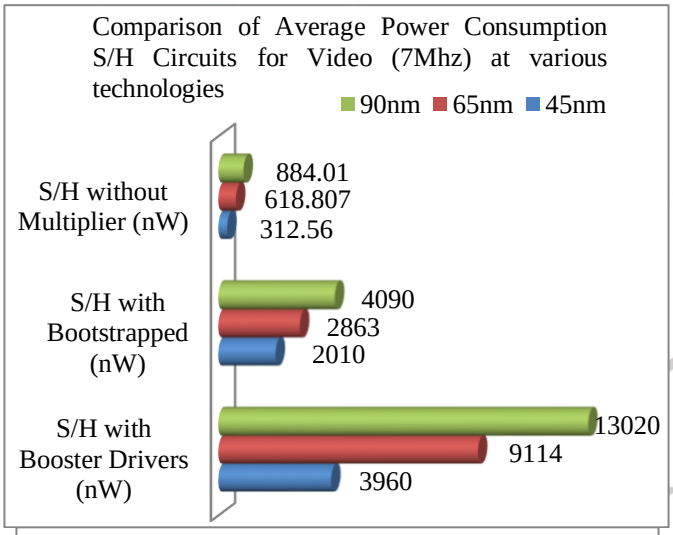


Fig7. The output of Bootstrapped S/H circuit without multiplier 90nm_20KHz

Fig8. SNDR Output of Bootstrapped S/H circuit without Multiplier 90nm_20KHz



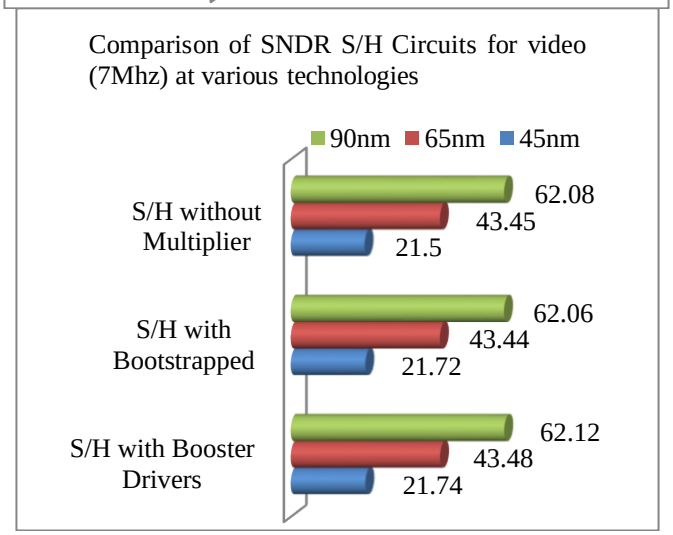


Table1. SIMULATION RESULTS for 90nm Technology

S/H circuits types		S/H with Boosted Driver	S/H with bootstrapped circuit	low power bootstrapped S/H without multiplier
Applications	**Parameters**			

Audio(20KHz)	**SNDR(dB)**	70.33	70.13	70.2
	Average Power Consumption	50.35nw	60.03nw	41.76Nw
	Power Saving (%)			**17%-30%**
	Sampling rate	800KS/s with a sampling capacitor of 0.1pf		
Bluetooth(1MHz)	**SNDR(dB)**	60.04	60.24	60.17
	Average Power Consumption	3.12uw	746.25nw	202.6nw
	Power Saving (%)			**93% - 72%**
	Sampling rate	40MS/s with a sampling capacitor of 0.1pf		
DVB-H(7MHz)	**SNDR(dB)**	62.12	62.06	62.08
	Average Power Consumption	13.02uw	4.09uw	884.01nw
	Power Saving (%)			**93% - 78%**
	Sampling rate	280MS/s with a sampling capacitor of 0.1pf		

IV. CONCLUSION

Being a part of the ADC sample and hold is consuming high power. For low power consumption, Various sample and hold circuits like Bootstrap Circuit, Low-Power Bootstrapped S/H Circuit without Multiplier Circuit & Boosted Driver Circuit are investigated for better performance and low power consumption at different frequency applications such as audio, Bluetooth and video frequencies. A low-power bootstrapped S/H circuit without a multiplier is proposed. The main aim of the low power bootstrapped circuit without a multiplier is to minimize the power consumption for the S/H circuit without affecting the SNDR performance. This is achieved by eliminating the multiplier circuit in and replaced it with a PMOS transistor. As a result, the low-power S/H with modified bootstrapped circuit without multiplier consumes less power as compared to other bootstrapped circuits which reported for medium and high-frequency applications. All the introduced bootstrapped sample and hold (S/H) circuits were simulated using 90nm, 65nm & 45nm CMOS technology on LT Spice VIII. So, the proposed low power bootstrapped sample and hold (S/H) circuit without multiplier saves 78% to 93% for 90nm & 65nm while 84% to 94% for 45nm of the power consumption with signal-to-noise and distortion ratio (SNDR) of 62.08 dB in 90nm 43.45 dB in 65nm & 21.50 dB in 45nm for 7 MHz input frequency signal.

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