Comparative Performance Analysis of XOR-XNOR Function Based High-Speed CMOS Full Adder Circuits

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***Abstract*— this papers presents the realization of full adder designs using Complimentary CMOS Design, Complimentary Pass Transistor Logic Design and XOR-XNOR Design in a single unit. The main motive of this paper is to determine the comparative study of power, delay, power delay product (PDP) of different Full adder designs using CMOS Logic Styles. Simulations results clearly determines that XOR-XNOR type Full adder Design is better compared to Complimentary CMOS style and Pass Transistor Design with respect to power, delay .Power Delay Product Comparison .The power delay product is also important parameter to determines the performance of the design. The XOR-XNOR implementation provides better performance and requires less number of transistors compared to other full adder designs. The implementation of design using GPDK 180nm with supply voltage of 1.8 V in Cadence Virtuoso Schematic Composer and simulations done by using Spectre Environment**

***Index Terms* — XOR, Full adders, XNOR, PTL, XOR-XNOR.**

I. INTRODUCTION

Power consumption and delay are two important considerations for VLSI system designer engineers. Our prime motive is to reduce the power and to get less delay that is nothing but the high speed for any design. Adder is one of the fundamental block present in arithmetic logic unit (ALU), floating point unit .In present arena we need fast arithmetic computation cells like adder and multipliers in the very large scale integration (VLSI) designs. The XOR/XNOR is the basic building block in many circuits like Arithmetic circuits.

Compressors, Comparators, Phase detectors, Code converters, Multipliers, Parity Checkers, Error-detecting and Error-correcting codes. Moreover, adders are very important components in some other applications such as microprocessor and digital signal processing (DSP) architectures. Digital signal processors and Microprocessors mainly rely on highly efficient implementations of generic floating point units and arithmetic logic units(ALU).

Full Adder is one of the core element in many of the complex arithmetic logic circuits like multiplication, division, addition, exponentiation, etc. To perform an arithmetic operation, mainly even a small circuit can consume very low power at extremely low frequency and also it may even take a long time to complete that operation. There are some standard implementations.

Some different logic styles have been used in the past times for design of the full-adder cells[5]-[19] and those techniques are used in this paper. Although they are used for producing similar function and the way of producing transistor count and intermediate nodes are varied. Different logic styles have different advantages such as the size, power dissipation, speed and the wiring complexity of the circuit. Different logic styles have different performance aspects. The propagation delay of a circuit is determined by the number of inversion levels, number of transistors in series, the transistor sizes or channel widths and the intra cell wiring capacitances. The size of the circuit depends on the number of transistors and their sizes and also on wiring complexity of the circuit. In order to get switching point to half of V_{DD} proper sizing should have to be done [1]-[4].

Some may use only one logic style for whole full adder while others can use more than one logic style for their implementation.

II. BACKGROUND

Power is the main criteria in all the electronic design equipment's. So that's why the designers are trying to minimize the power consumption when designing the task. In CMOS circuits mostly the energy consumed is because of switching activity. Thus the number of nodes in the circuit, energy per every node and also the total number of transaction operations per second, all these factors led to the power consumption. Power dissipation is based on the node capacitances of gate, threshold switching activity and circuit size.

There are four reasons for the power dissipation: dynamic power due to the charging and discharging of capacitance in the circuit because of switching transactions and leakage current is because of reverse bias condition in diode structures, sub threshold leakage, short-circuit current power due to rise and fall times, and static biasing power found in some logic styles (i.e pseudo-NMOS) These three are the major components of power dissipation in (CMOS) circuits:

1. *Dynamic Power:* Power consumed by the circuit node capacitance because of transistor switching.
2. *Short Circuit Power:* Power consumed because of current flowing from V_{DD} to ground during switching of the transistor.
3. *Static Power:* Power because of leakage and static currents.

The increase in demand for low power and low voltage VLSI circuits can be investigated different levels of design, such as the architectural, circuit, layout and the process technology. At the device level, reduction in supply voltage and reduction in the threshold voltage to reduce the power consumption, where as in layout use of short channel transistors, poly and diffusion areas, shorter metal lines for connecting two various devices. It reduces capacitances in circuit and device level.

On an architectural level, CAD algorithms are required for fewer number of gates which reduces the overall power consumption. All these techniques employed most of the times reduce power increase of delay [1]-[5].

(A) Complementary CMOS Full Adder(C-CMOS):

The complementary CMOS full adder (C_CMOS) is one of the basic full adder circuit shown in below fig .1(a)

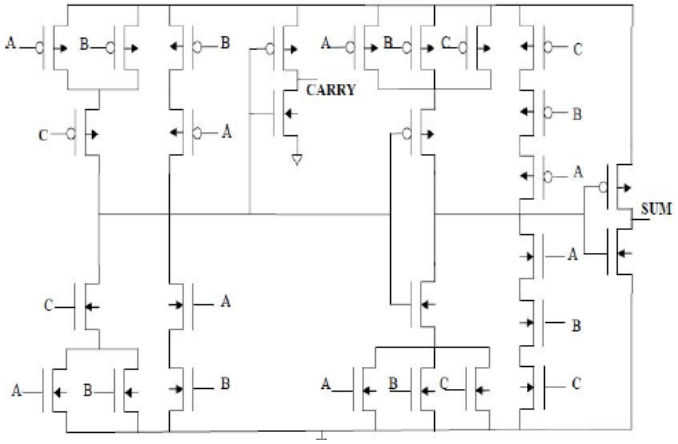


Fig.1(a) C-CMOS Full Adder Cell[3].

The equation for C-CMOS is given as below

Sum =Carry'.(A+B+C) + (A.B.C) Sum = ABC + AB'C' + A'BC' + A'B'C &

.

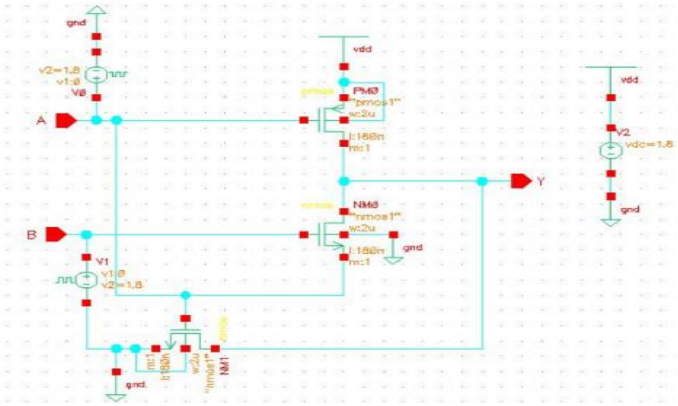
From the equation we have drawn the pull up and pull down networks and from that we have generated the sum and carry outputs. The advantages of the complementary CMOS logic circuit are stability and layout regularity at lower voltages due to smaller number of interconnecting wires and complementary pairs of transistors. The C_CMOS have some robustness against transistor sizing and voltage scaling which can have reliable operation at very low voltages with different transistor sizes.

The second adder is complementary pass transistor logic (CPL) uses 32 transistors with swing restoration. Most CPL gates can have an complexity in interconnection at the layout level with the increase in power and delay. For low power applications Pass Transistor Logic (PTL) is best suitable technique and explanation was given in .The advantage of Pass Transistor Logic (PTL) is that either PMOS or NMOS is enough to implement a complete design [6]-[8] and so number of transistors gets decreased and also smaller input loads, especially for NMOS network and also by this PTL we can eliminate short circuit energy dissipation.

(B)3T XOR:

The modified model of a CMOS inverter and a PMOS pass transistor. Whenever the input B is of logic 1 or logic 0, then the inverter functions like a normal CMOS inverter. And the output Y is the inverter of input A. Whenever the input B is at logic 0, the CMOS inverters output is at high impedance(z). However transistor N3 is in on condition and the output Y gets the same value as input A.

When A=1 and B=0, voltage reduction happens because of threshold drop occurs across the transistor N3 and also the output Y's performance gets deteriorated when compared to the input value. Degradation can be reduced by increasing the W/L ratio of the transistor N3.



Another problem is current back through transistor N1 occurs when A=1 and B=0. The output of the pass transistor is fed back through transistor N1 which it operates in the active region. This can overcome by reducing the W/L ratio of transistor N1.

(C) 8T ADDER USING XOR GATE:

The 8T adder is implemented using 3T Xor gates The sum output is basically obtained by a implementing exclusive OR of the three inputs in The final sum of the products is obtained using a OR logic of PTL type[15].

Thus two stage are required to obtain the sum value as output and at most in both the stage delays are to be added. The voltage drop due to the threshold in the transistors M3 and M6 can be reduced by increasing the aspect ratios of the transistors. The input combinations of all the three inputs have been checked by taking the rise and fall time into considerations. The 8-T XOR based Full Adder is shown in fig .2(b)

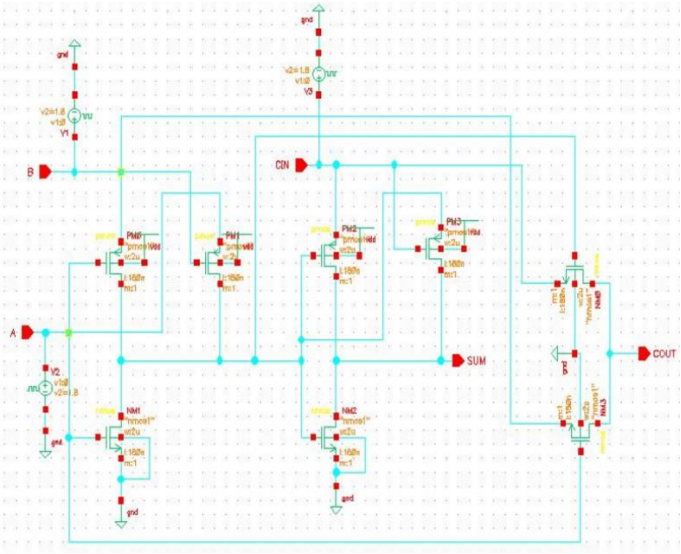


Fig.2(b) XOR based Full Adder cell

(D) 3T XNOR

Similarly like XOR the XNOR also can be performed with the transistors to get better performance and optimized the working functionality is given When A=0 and B=0 transistor then p1 becomes on and N1,N2 becomes off so the output gets charged to VDD. A=0 and B=1 circuit shows logic 0 output, because transistor P1 is off and output node gets discharged by transistor N2. A=1 and B=0 then both transistors P1, N1 are on and output is discharged using N1 and N2 transistors. A=B=1, output gives high logic as N1 is on and thus the logic 1 is sent to the output. The 3-T XNOR based Full Adder is shown in below fig 2(c).

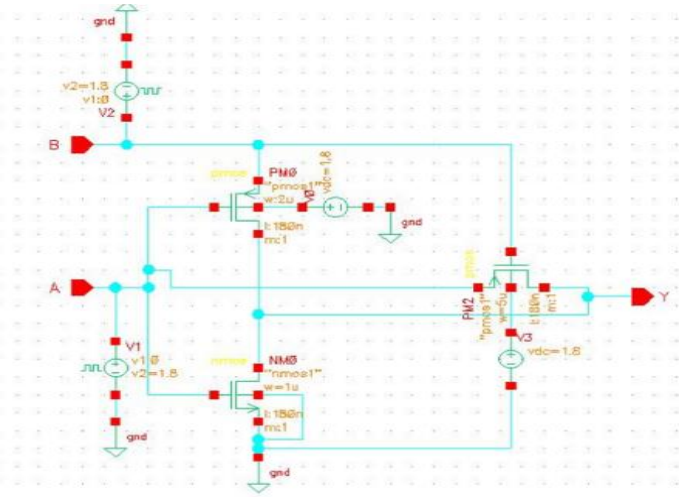


Fig.2(d) 3T XNOR Cell

(E) 8T XNOR

It is implemented by two XNOR gates with one multiplexer block Sum is generated by using two XNOR gates, Carry out is generated by using two transistors multiplexer block. The XNOR gates with eight transistors has been implemented by using 3T XNOR gate, The simulation has performed form 3.0V to 1.2V to check the levels of output signal circuit in which it shows desired voltage levels. The 8T XNOR based Full Adder Cell was shown in below fig .2(d).

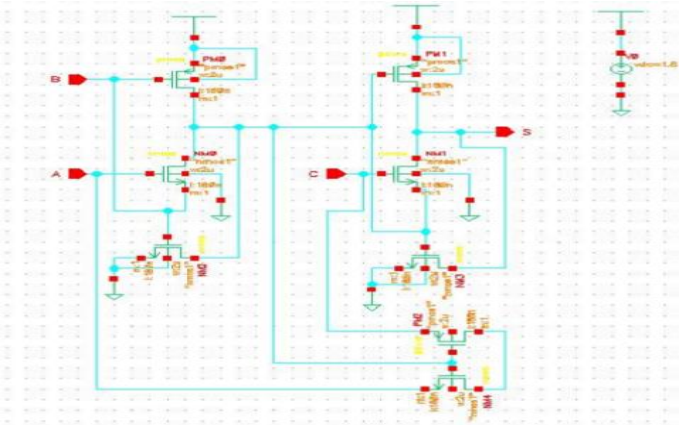


Fig.2(d) XNOR based Full Adder cell

III. PROPOSED ARCHITECTURE

In this proposed adder we will use one XOR and one XNOR and a multiplexer to generate output sum and carry. The expressions for sum and carry are given in below.

$$\text{Sum} = H \text{ XOR } C = H.\ C' + H'.\ C \qquad \text{Cout} = A.\ H' + C.\ H$$

$$\text{Sum} = (A \oplus B \oplus C) = C'\ (A \oplus B) + C\ (A \oplus B)'$$

Where H is (A XOR B) and H' is compliment of (AXNORB).

The proposed adder cell has 16 transistors and is mainly based up on low power XOR-XNOR pass transistor logic and transmission gates.

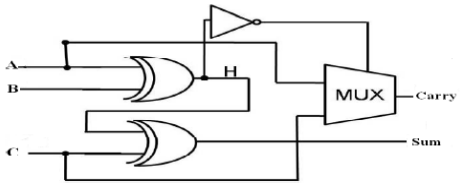


Fig.(a)

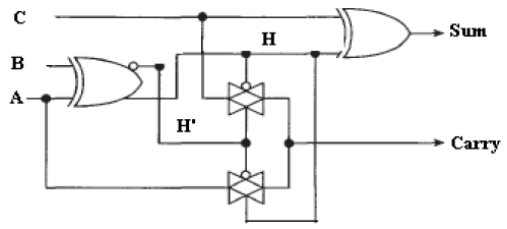


Fig.(b)

Fig.3 General Structure of proposed XOR-XNOR Adder[13].

In this proposed adder the two transmission gates are used as multiplexer and the sum can be generated by XOR gates and output carry can be generated by XOR /XNOR gates shown in the above figure and output of XOR gate can be used as the selection line for multiplexer or as the control for the transmission gate which we will get output as the carry. The proposed adder circuit is designed by the combination of the two logic styles in order to get lower power consumption, high speed and good energy efficiency. We know that supply voltage variations will leads to the greater reduction in the power and also in the circuit delay.

IV. EXPERIMENTAL RESULTS

All the circuits presented in this paper are designed by using Cadence VIRTUOSO environment by using CMOS process design kit. The range of supply voltage we have employed was The proposed adder circuit is designed and simulated for different ranges of supply voltages is 1.3V-1.8V. The results of this proposed adder circuit can be compared with the different conventional adder circuit designs. Totally 16 transistors are needed to design the proposed adder circuit. By this we can clearly decide that the proposed circuit can have lower area overhead than the other conventional adder circuits. The delay values of conventional adder circuits and proposed adder circuit are compared and tabulated in below in table.1and table.2. and from the results it is clear that the proposed adder can have very less delay. The proposed circuit can have the lower power values and also lower PDP values as compared to other conventional adder circuits

Table 1 Simulation results for Full adder at V_{DD}=1.3V

Type	Power(µW)
C-CMOS	5.521
CPTL	3.52
XOR	3.265
XNOR	2.985
XOR-XNOR	1.295

Table 2 Simulation results for Full adder at 1.3V

Type	Delay(ps)	PDP	# of transistors
C-CMOS	1.65	9.10	28
CPTL	1.257	4.424	32
XOR	0.825	2.64	8
XNOR	0.785	2.345	8
XOR-XNOR	0.653	0.832	16

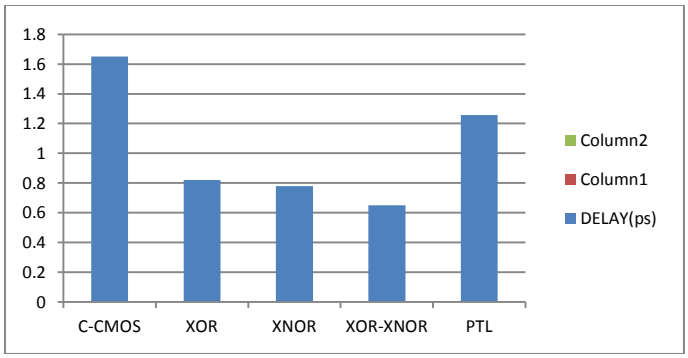


Fig.4 (a): Delay comparison for different adders

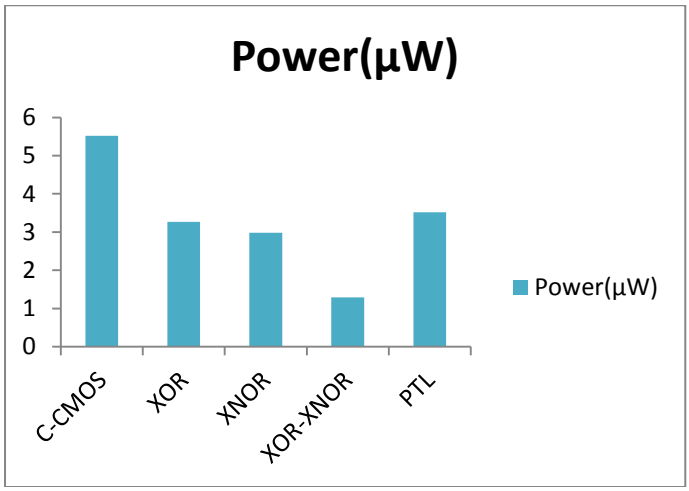


Fig 4(b): Power Comparison results for different adders

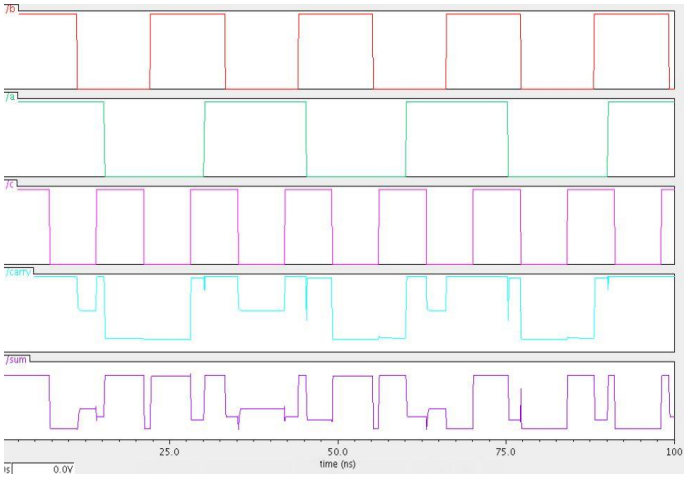


Fig.4(c) Simulation input and output results for proposed adder

V. CONCLUSION

This paper includes the Implementation of different adder logic styles includes Complimentary CMOS, XOR-XNOR, Complementary Pass Transistor Logic and Simulated by using Cadence Environment .The Comparison of power, delay, PDP are tabulated. From the table it is clear that Complimentary CMOS Adder design having more power consumption and delay so more PDP. This paper includes a new adder design of XOR-XNOR based adder cell with less power, delay, and power delay product (PDP). Cadence simulations results can show that the new adder design have very less PDP when compared with all other designs.

The new full adder design can provide good voltage swing at low supply voltages and provides best performance with respect to all other conventional full adder designs in terms of both speed and power.

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