Design and Simulation of Sigma Delta ADC Using VHDL AMS

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***Abstract*- There is two main parts of Sigma-delta ADC: analog modulator and digital filter, the performance of modulator determines the performance of sigma-delta ADC, so the design of modulator is very important. This paper introduces the principle of sigma-delta ADC modulator with high accuracy and the applied over sampling technique, noise shaping technique and multi-bit quantize technique. This paper determines the design scheme of modulator—second orders CIFF (Cascade of integrators, feed forward form) structure and it makes the behavior level verification for this scheme by VHDL AMS.**

***Index Terms*— Sigma-delta ADC; modulator; over sampling; noise shaping**

I. INTRODUCTION

The bridge linking the analog world and the digital world is ADC (Analog to Digital Converter), it can covert the analog signal to the digital signal, and benefits to the storage, processing and transmission of the data [1]. With the development of electronic technique, ADC provides wider application, data conversion accuracy is much higher, for example, in high fidelity system, it puts forward the very high requirement to ADC, and namely, the resolution of A/D converter must be more than 16-bit. However, when compared to other traditional A/D converter, such as parallel comparison A/D converter, double integral A/D converter and successive approximation A/D converter, they can't gain very high accuracy[2-3].

One superior way to get the high accuracy converter is Oversampling sigma-delta modulation method, this method adopts the over sampling technique and the noise shaping technique of sigma-delta modulator, so it will provide dual suppression for quantization noise in signal frequency band. Finally digital decimation filtering used for down sampling purpose.

Compared to other converters with the different structure, sigma-delta ADC has many advantages, such as high accuracy, high linearity and large dynamic range and so on [4].

According to the digit capacity of quantizer in modulator, sigma-delta is classified as 1-bit quantization and multi-bit quantization. With the wider application of sigma-delta ADC, the requirements to it become higher. The uppermost parameter to measure performance is the SNR, and SNR can be improved largely by changing the modulator order, over sampling rate and quantization bits. Even though by increasing the modulator order can also improve the SNR, the attendant problems have emerged, such as the stability and complexity of circuit, and so on [5]. These problems are also much serious in low voltage and low power circuits at present. Therefore, the multi-bit sigma-delta modulator will be the market because of the performance advantage and wide application prospect [6].

A new mixed-signal HDL standard VHDL-AMS was approved in March 1999 first time. This standard allows the utilization of VHDL-AMS to construct complex analog and mixed-signal models by combining differential equations, logical controls and algebraic constraints.

A VHDL-AMS behavioral model of a Continuous-Time Delta-Sigma Modulator is presented in this paper.

II. CONTINUES-TIME DELTA-SIGMA MODULATOR ARCHITECTURE

ΔΣ *Converters: An overview*

The ΔΣconverter is a 1-bit sampling system. The input of the converter is an analog signal needs to be relatively slow so the converter can sample it multiple times, by a technique known as oversampling. At the output port the sampling rate is hundreds of times faster than the digital results. Each individual sample is accumulated over time and averaged with the other input-signal samples through the digital/decimation filter.

The primary internal cells of the ΔΣ converter's are theΔΣ modulator and the decimation filter. The ΔΣ modulator is shown in Figure 1 which samples the input signal at a very high rate into a 1-bit stream. The decimation filter takes this sampled data and converts it into a high-resolution, slower digital code. Most converters have one sample rate; the ΔΣ converter has two—the input sampling rate (fS) and the output data rate (fD).

*The*ΔΣ*modulator*

The ΔΣ modulator is the heart of the ΔΣ ADC. ΔΣ Modulator is responsible for digitizing the analog input signal and reducing noise at lower frequencies. The architecture implements a function called noise shaping in this stage that amplifies low frequency noise up to higher frequencies where it is outside the band of interest. The ΔΣ converters are well-suited for low-frequency, high accuracy Measurements due to the feature of Noise shaping of sigma delta modulator.

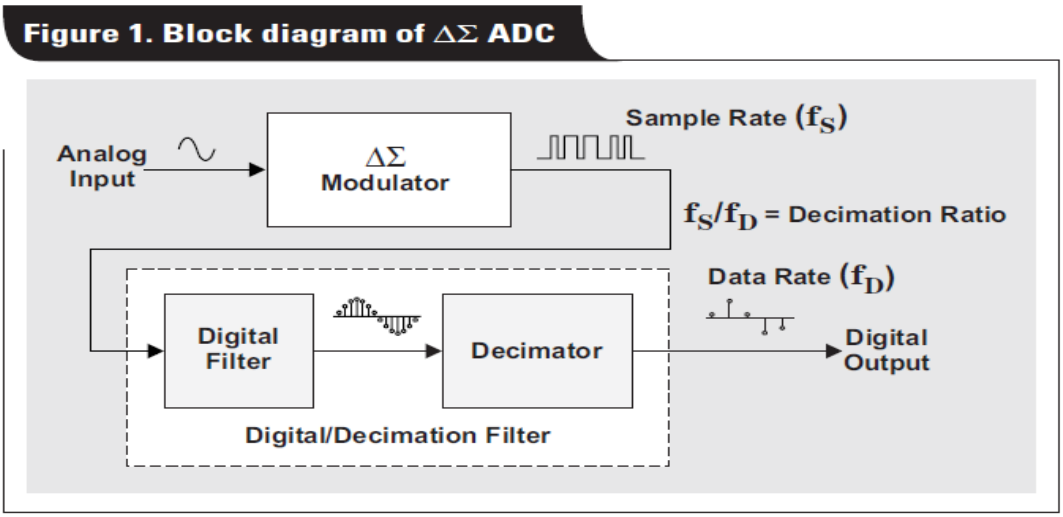


Fig 1 Block Diagram of sigma delta ADC

Figure 1 shows the basic block diagram of ΔΣADC. The input signal to the ΔΣ modulator is a time-varying analog voltage signal. The input-voltage signal was primarily for audio applications where AC signals were important in the earlier ΔΣ ADCs. Now a days that attention turned to precision applications, conversion rates include DC signals. So for This discussion single cycle of a sine wave is used for illustration.

The ΔΣ modulator can be presented by two ways—in the time domain (Figure 2) or in the frequency domain (Figure 3). Figure 2 shows the mechanics of a first-order ΔΣ modulator in the time domain. The modulator converts the analog input signal to a high-speed, single-bit, modulated pulse wave. The frequency analysis in Figure 3 shows how the modulator removes the noise in the system and facilitates the production of a higher-resolution result.

The ΔΣ modulator which is shown in Figure 2 acquires many samples of the input signal to produce a stream of 1-bit codes. The sampling speed, **fS**, can be implemented by the system clock in conjunction with the modulator's 1-bit comparator. The quantizing action of theΔΣmodulator is produced at a high sample rate that is equal to that of the system clock in this manner. The ΔΣ modulator produces a stream of digital values that represent the voltage of the input, in this case a 1-bit stream like all other quantizers. The ratio of the number of ones to zeros represents the input analog voltage as a result,. Unlike most quantizers, the ΔΣ modulator also includes an integrator, which has the effect of shaping the quantization noise to higher frequencies.

Architecture of sigma delta modulator

The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, in the time domain; provide an analog voltage at **x2**. This voltage is inputted to the integrator, whose output is in a negative or positive direction. The slope and direction of the signal at **x3** is dependent on the sign and magnitude of the voltage at **x2**.

When the voltage at **x3** equals the comparator reference voltage, the output of the comparator becomes from negative to positive, or positive to negative, depending on its real state. The output value of the comparator, **x4**, is clocked back into the 1-bit DAC, as well as to the digital filter stage, **yi**. When the output of the comparator switches from high to low or low to high, the 1-bit DAC responds by changing the analog output voltage of the difference amplifier. This will create a different output voltage at **x2**, make the integrator to progress in the opposite direction. This time-domain output signal is a pulse-wave representation of the input signal at the sampling rate (**fS**). If the output pulse train is averaged, it equals the value of the input signal as its original form.

Figure 2 also shows the time-domain transfer function. The 1-bit ADC digitizes the signal to a coarse, 1-bit output code that produces the quantization noise of the converter in the time domain. **ei – ei – 1** is the output of the modulator which is equal to the input plus quantization noise. This formula shows that the quantization noise is the difference between the current quantization error (**ei**) and the previous quantization error (**ei – 1**).

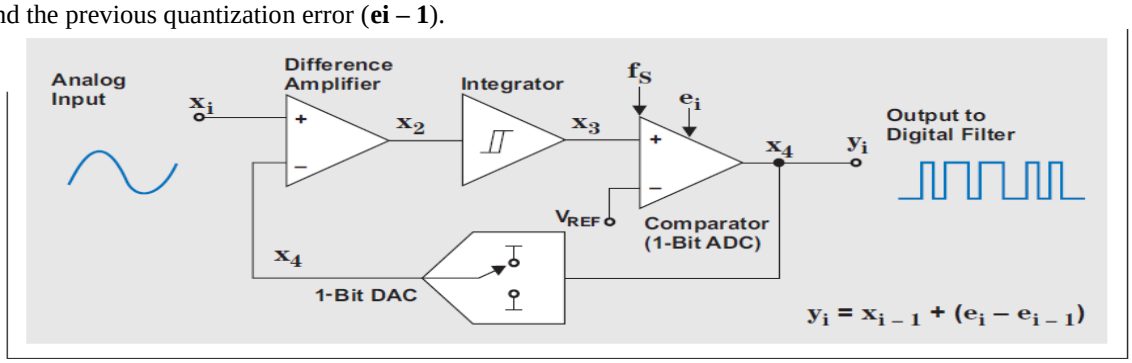


Fig 2 First order sigma delta modulator in time domain

Location of this quantization noise is illustrated in Figure 3. The combination of the integrator and sampling strategy implements a noise-shaping filter on the digital output code in Figure 3. In the frequency domain, the output of time domain pulses appears as the spur and shaped noise. The noise characteristics in Figure 3 are the key to understanding the modulator's frequency operation and the ability of the DS ADC to achieve such high resolution. the quantization noise for a first- order modulator starts low at zero hertz, rises rapidly, and then levels off at a maximum value at the modulator's sampling frequency (**fS**) is shown in Figure 3. A great way to lower the modulator's in-band quantization noise is to integrates twice instead of once.

Some of the disadvantages of the second- or multi-order modulators include increased complexity, multiple loops, and increased design difficulty.

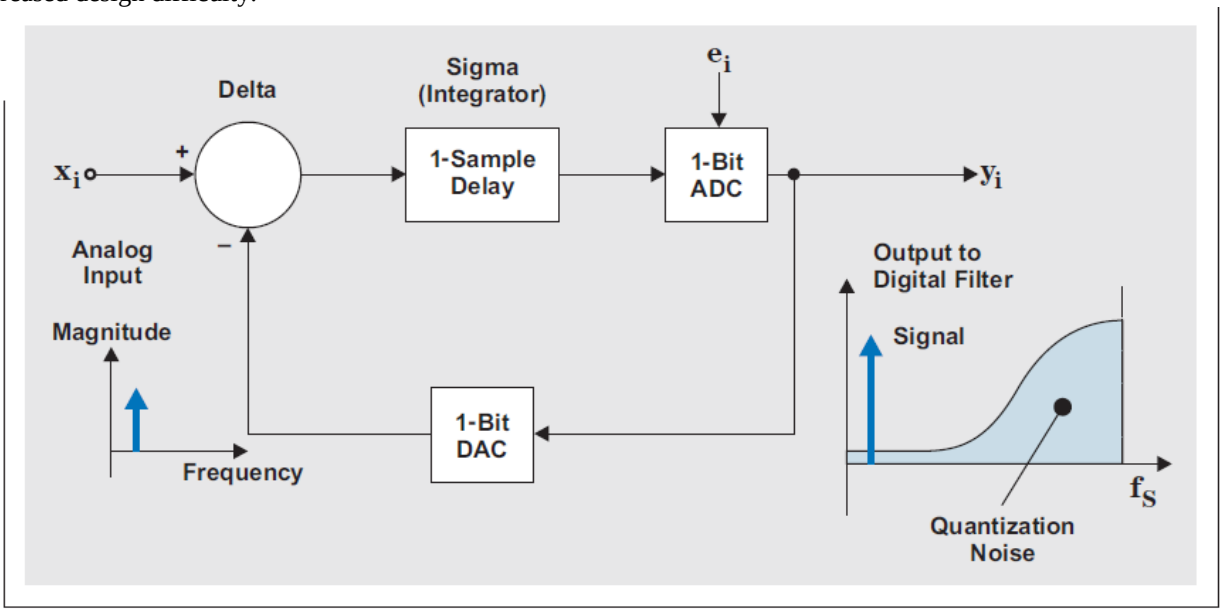
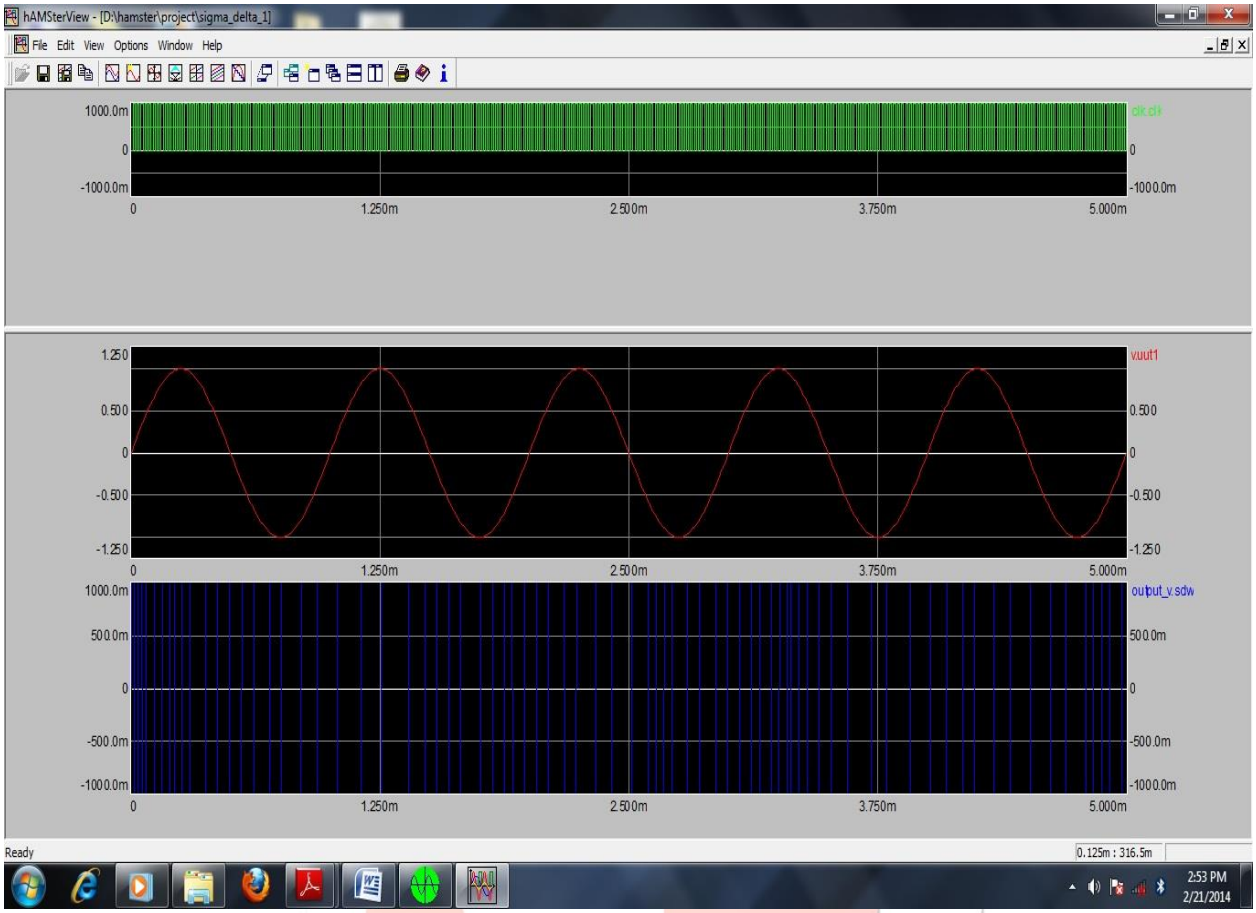


Fig 3 First order sigma delta modulator in Frequency Domain

III. OVERVIEW OF VHDL-AMS LANGUAGE

A derivative of the hardware description language VHDL (IEEE standard 1076-1993) is VHDL-AMS. Analog and mixed-signal extensions (AMS) are included in order to define the behavior of analog and mixed-signal systems (IEEE 1076.1-1999). The VHDL-AMS standard was created with the intent of enabling designers of analog and mixed signal systems and integrated circuits to create and use modules that encapsulate high-level behavioral descriptions as well as structural descriptions of systems and components. An industry standard modeling language for mixed signal circuits is VHDL-AMS . It provides both continuous-time and event-driven modeling semantics, and so is suitable for analog, digital, and mixed analog/digital circuits. VHDL-AMS is particularly well suited for verification of very complex analog, mixed-signal and radio frequency integrated circuits.

IV. IV. SIMULATION RESULTS



V. CONCLUSION

A VHDL-AMS behavioral model of a Continuous-Time Delta-Sigma Modulator is presented in this paper. An advanced design methodology using a combination of behavioral models and transistor level models is used in order to reduce the simulation time and to improve the design flexibility. The Continuous-Time Delta-Sigma modulator is able to directly digitize a 1KHz input signal in a 20MHz bandwidth, with OSR of 5.5.

VI. REFERENCES

[1] X. Jiaqing, "Research and Design of A 16Bit Sigma-delta Modulator", Jin Lin: Jin Lin University, (2012), pp. 1-5.
[2] N. Tan, S. Ericsson and L. Wanhammar, "Over-sampling A/D Converters and Current-mode Techniques", Link ping: Link ping University, (1994).
[3] Y. Hui-min and Q. Min-jun, "A Novel Sigma-Delta and Its Architecture Design", Journal of Circuits and Systems. (2004), pp. 54-57.
[4] W. Louis, "Modeling and Design of High-resolution Sigma-Delta Modulators", PhD. Dissertation: Stanford University, (1993), pp. 4-8.
[5] L. Lim and D. Johns, "Time-interleaved Oversampling A/D Converters", IEEE Transactions on Circuit and System, (1997), pp. 634-645.
[6] W Stewart, "Oversampling and Sigma-Delta Strategies for Data Conversion", IEEE Journal of Electronics and Communication Engineering, (1998), pp. 37-47.