Single Electron Transistor and its Simulation methods

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***Abstract* - Single-electron transistor (SET) is a key element of current research area of nanotechnology which can offer low power consumption and high operating speed. Single electron transistor [SET] is a new nanoscaled switching device because single-electron transistor retains its scalability even on an atomic scale and besides this; it can control the motion of a single electron. The goal of this paper is to discuss about the basic physics of nanoelectronic device 'Single electron transistor [SET]' which is capable of controlling the transport of only one electron and focuses on some basic device characteristics like Orthodox theory ,tunneling effect ,Coulomb blockade ,Quantum Dot & 'Coulomb staircase' on which this Single electron transistor [SET] works. Various simulation methodology of the single electron transistor is discussed along with the tools available like Spice, SIMON, SECS etc . The physics underlying the operation of SET is explained, a brief history of its invention is presented.**

***Keywords* - Quantum Dot; Columbic blockade; orthodox theory; SET; PSPICE; SIMON**

I. INTRODUCTION

Single-electron transistors (SETs) hold great promise for future nanoelectronic circuits due to their small size, low power consumption, and ability to perform fast and sensitive charge measurements [1]. SET is a highly charge-sensitive device, capable of detecting charges far less than that of one electron. This remarkable property makes SET a very useful tool in experiments where very high charge sensitivity is required. They are increasingly being used and proposed as measurement devices for quantum systems, including quantum computers and quantum dot, cellular automata, and as logic elements in their own right as replacements for MOSFETs.

1.1 History of SET

In his famous 1911experiments, Millikan [2] observed the effects of single electrons on the falling rate of oil drops. The effects of charge quantization were first observed in tunnel junctions containing metal particles as early as 1968[3].Soon after the idea of overcoming the Columbic Blockade can be prevail with the use of gate electrode came to many scientist [4-7]. And later Kulik and Shekhter [8] they came up with the theory of Coulomb-blockade oscillations, which is the periodic variation of conductance as a function of the applied gate voltage. In the year 1987 Fulton and Dolan successfully made the first SET [9] which was entirely made up of metals ,and they obtained the same result as predicted earlier by Fulton and Dolan i.e. they observed the periodic oscillation. They used Metal particle which is connected to two metal leads by the tunnel junction. Which is mounted on the insulator and Gate was underneath it. Shortly thereafter Meiravet al.[11] made controlled devices of the kind depicted in Fig. 1, albeit with an unusual heterostructure with AlGaAs on the bottom instead of the top. In these and similar devices the effects of energy quantization were easily observed. During the year 1989 first Semiconductor SET was accidentally fabricated by Scott-Thomas in a narrow Si field effect transistor [12], for this case tunnel barrier was obtained by interface charge in this case the tunnel barriers were produced by interface charges .

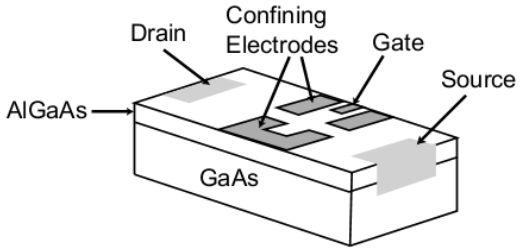


Fig 1. Schematic drawing of a SET. Wires are connected to source and drain contacts to pass current through the 2DEG at the GaAs/AlGaAs interface.

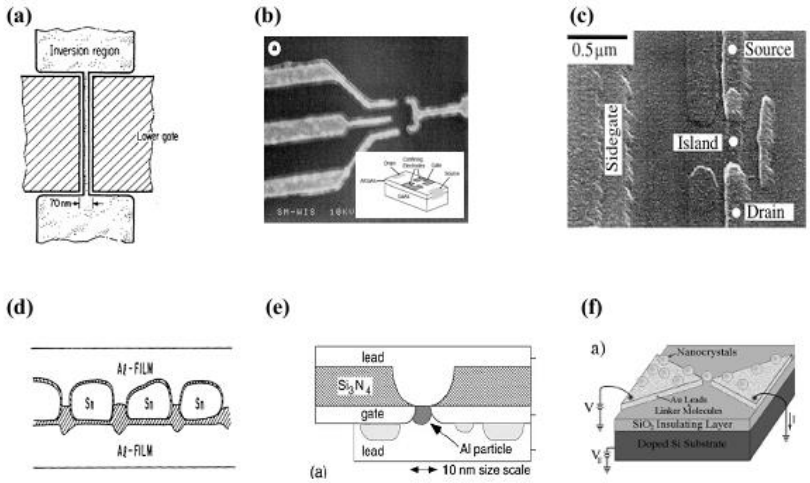


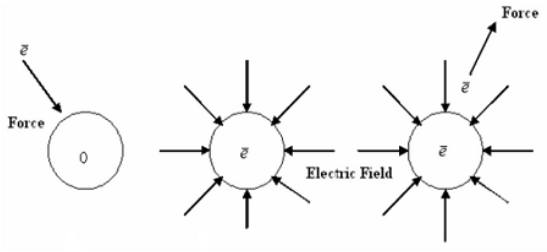
Fig 2. Previous approaches to SETs. (a) Si SETs [13].(b)2DEG SETs [14]. (c) SETs fabricated by angle evaporation technique [15]. (d) SETs incorporating the ensemble of small metallic islands [16]. (e) Nanopore SETs [17].(f) SETs fabricated by electron beam lithography and self-assembly of nanoparticles [18].

Table 1.Timeline for Single electron transistor

Year	Development in SET
1911	Millikan oil drop experiment
1968	Gortner studied the effect of charge quantization on grains
1977	Kulik and Shekhter introduced theory of Coulomb-blockade oscillations
1987	Fulton and Dolan successfully made the first SET
1989	Semiconductor SET was fabricated accidentally by Scott-Thomas
1999	M A Kaster developed hetero junction SET
1999	Likhrov proposed Orthodox theory

1.2 Theory for Single electronics

Single electronics is the fundamental concept behind single electronic devices like single electron transistors (SETs) that can be explained by assuming a small metallic sphere, as shown in fig 2. , which is initially electro-neutral i.e. the net charge on this sphere is zero because of the same number of electrons and protons in it. Now, consider that a single electron is positioned close to the sphere. In this situation, it gets attracted by the sphere. Thus, this single electron joins the sphere and leaves a negative charge of –e on it. Now, due to the presence of this negative charge, an electric field is created around the sphere so that if any other electron comes close to this sphere, it will face a strong repulsive force exerted by the electric field created around the sphere.



(a) (b)

Fig 3.a) an electron feeling a small attractive force as it approaches a sphere. b) Once sphere gets charge by a single electron; other electrons will feel a strong repelling force.

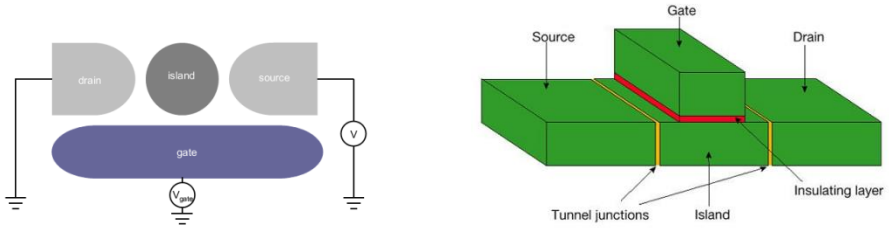
The concept behind the single electronics shows that the more accurate measurement of the strength of this tunneling effect is charging energy or electrostatic energy, which is given by: $E_c = e^2/2C$. From the above given equation, it is clear that if capacitance is very small, the charging energy may be dominating. if a tunnel junction is placed in an ordinary conductor, the flow of electrons penetrating this thin insulating barrier will be restricted by it. Thus, the current through a conductor may be quantized in this situation. The electric charge may be moved by both continuous and discrete process due to the application of tunnel junction as an insulating barrier in an ordinary conductor. Now, if discrete electrons can tunnel through the junction, the charge will be accumulated at the tunnel junction. When a high bias voltage is applied across this junction, one electron gets transferred.

Two important condition are required for the tunneling process :-

- Coulomb energy must be greater than the thermal fluctuations ,$E_c = e^2/2C > k_B T$. Where kB is Boltzmann's constant and T is temperature in Kelvin.
- Electrons should be localized only on the island and all tunnel junctions should be opaque for electrons to confine them to the islands , $R_T = h/e^2 = 25.813\ K\Omega$.

1.3 Single Electron Transistor

A SET consists of one small island connected to two electrodes (a "source" and a "drain") through two



(a) (b)

Fig 4. (a) Representation of SET.(b)Schematic diagram of a single-electron transistor.

tunnel barriers and capacitively coupled to a nearby third electrode ("gate" electrode) [19-21].A Small Island is there between the source and the drain called as quantum dot. The resistance between the island and each of the electrodes must be larger than the quantum resistance. In this case, the number of electrons on the island is well defined. Therefore, the current flowing through the island can only occur by successive addition and removal of single electrons to and from the island a single electron would tunnel from the source to the island and subsequently from island to drain. The tunneling of electrons can be blocked at low bias voltage due to the Coulomb repulsive interaction until enough energy is provided by applying a voltage difference between the source and drain electrodes. A gate voltage is applied to the gate electrode and tunes the electrostatic potential of the island. Controlling the gate voltage regulates the number of electrons tunneling on or off the island, one at a time.

1.4 Fabrication

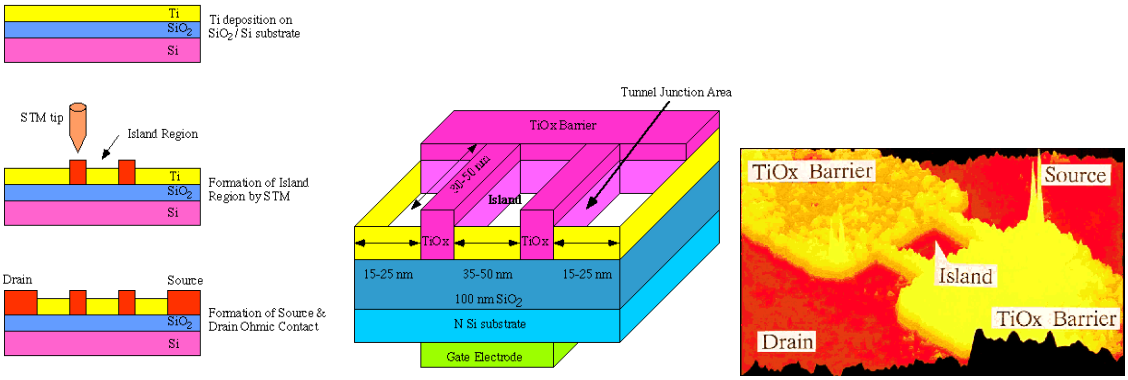
As of now we have gone through physics governing single electronics, One of the main requirements to fabricate single electronics is to achieve capacitance in atto farad or less, which can be achieved by making structure less than 100nm. Optical lithography is being used in industries for mass fabrication of semiconductors is limited to feature sizes greater than 100nm if we use very sophisticated aligners. Christoph Wasshuber [23] mentioned two approaches as top down and bottom up. In former, one starts with wafer, define structures using lithography, etch, deposit layers if required. This is the conventional approach used in semiconductor industry and we process complete wafer at one time. Most widely used approach is top down. Bottom up approach involves building of small molecules and then assembling them on top of the substrate. These molecules include nanoparticles of gold or quantum dots ,this is a slow step but we can achieve high precision.

1.5 Simulation

A simulator is a collection of hardware and software systems which are used to mimic the behavior of some entity or phenomenon. Typically, the entity or phenomenon being simulated is from the domain of the tangible ranging from the operation of integrated circuits. Simulators may also be used to analyze and verify theoretical models which may be too difficult to grasp from a purely conceptual level. Simulators provide a crucial role in both industry and academia. Conventional circuit simulators based on Kirchhoff's law can be used when the electronics charge is assumed continuous, but all single electron circuits exhibit tunneling and therefore the charge transport is discrete. There are fundamentally three different approaches for simulation of single electron circuits, namely Monte Carlo, SPICE macro-modeling, Master Equation.

II. FABRICATION

Recently, single electron transistors (SETs) have come to be considered candidates as elements for future low power, high density integrated circuits because of their potential for ultra-low power operation involving only a few electrons. In order to be useful in practical applications, however, SETs must be operable at room temperature. Capacitance and thermal fluctuation limitations require that the island size of the SET be no larger than ~10 nm, a feature size out of the range of present conventional microfabrication processes. Room temperature operation of single electron memory has been realized by the use of self-organized, small-size structures on thin poly-silicon films [24]. However, it is difficult to control the size and structure of the SET island with the spontaneous size formation fabrication method. Earlier, it was demonstrated an artificial pattern formation method based on the scanning tunneling microscope (STM) which avoids the control problems in self- organized structures [25]. Using this technique, we have succeeded in fabricating an SET. The SET operates at room temperature, showing a clear Coulomb staircase with a ~150 mV period at 300 K. A description of the STM nano-oxidation process [26] is shown in figure 5(a). A 3 nm thin titanium (Ti) metal film is deposited on a 100 nm thermally oxidized SiO_2/n-Si substrate. The Ti surface was oxidized by anodization through the water adhered to the surface of the Ti from the atmosphere, using the STM tip as a cathode, forming nanometer size Ti oxide (TiOx) lines. The barrier height of the TiOx/Ti junction has been found to be 285 meV for the electron from the temperature dependence of the current. The relative permittivity of the TiOx has been determined as $e_r = 24$ from the electric field dependence of the TiOx barrier height [27]. Figure 5(b) shows a schematic illustration of the SET made by the STM nano- oxidation process. At both ends of the 3 nm thick Ti layer we formed the source and drain ohmic contacts, and on the back side of the n-Si substrate, we formed the gate ohmic contact. At the center region of the Ti layer, we formed the island region, surrounded by two parallel, narrow TiOx lines, that serve as tunneling junctions for the SET, and two large TiOx barrier regions. Figure 5(c) is an atomic force microscopy (AFM) image of the island region of a fabricated SET.



(a) (b) (c)

Fig. 5 (a) Fabrication of the Ti/TiOx SET by the STM nano-oxidation process.(b)Schematic of a single electron transistor (c)AFM image of a single electron transistor made by the STM nano-oxidation process.

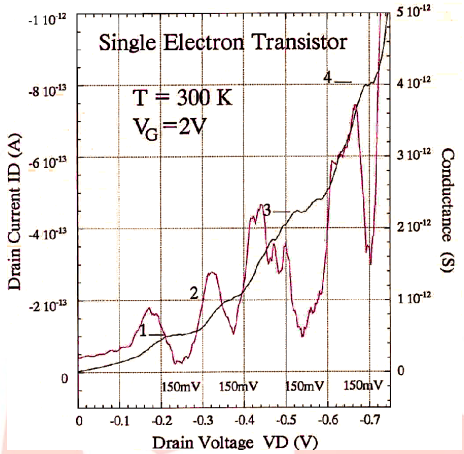
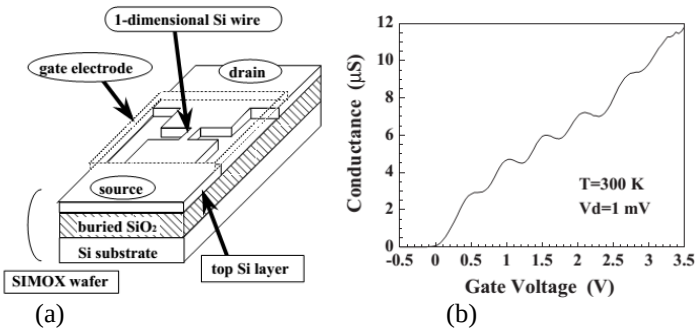


Fig 6. Drain current v. drain voltage characteristics of the SET at 300 K .

The drain current-voltage characteristics of the SET were measured at room temperature and are shown in fig 6. The gate bias was set to 2 V. In the figure, the solid lines shows the current of the SET, and the dashed line shows the conductance of the SET. Between the drain bias of 0 V and -0.75 V, four clear Coulomb staircases with a ~150 mV period are observed. The conductance oscillates with the increase of the drain bias with almost the same 150 mV period. The lower peaks of the conductance oscillation correspond to the flat regions of the current of the Coulomb staircase .So the fabricating a room temperature operable single electron transistor using the STM nano-oxidation process. The SET shows a Coulomb staircase with periods of 150 mV at a temperature of 300 K. The Coulomb gap and staircase observed at high temperatures are attributed to the small tunneling junction area made by the STM nano- oxidation process. The fabrication process is quite easy and could be applicable to many kinds of devices.

Yasuo Takahashi developed two novel methods of fabricating very small Si single-electron transistors (SETs), called Pattern Dependent Oxidation (PADOX) and Vertical Pattern-Dependent Oxidation (V-PADOX). These methods exploit special phenomena that occur when small Si structures on SiO2 are thermally oxidized. Since the size of the resultant Si island of the SET is about 10 nm, we can observe the conductance oscillations in the SET even at room temperature. The controllability and reproducibility of these methods are excellent because of the stability of the thermal oxidation process. We are using PADOX and V-PADOX to integrate single electron devices (SEDs) for sophisticated functions.

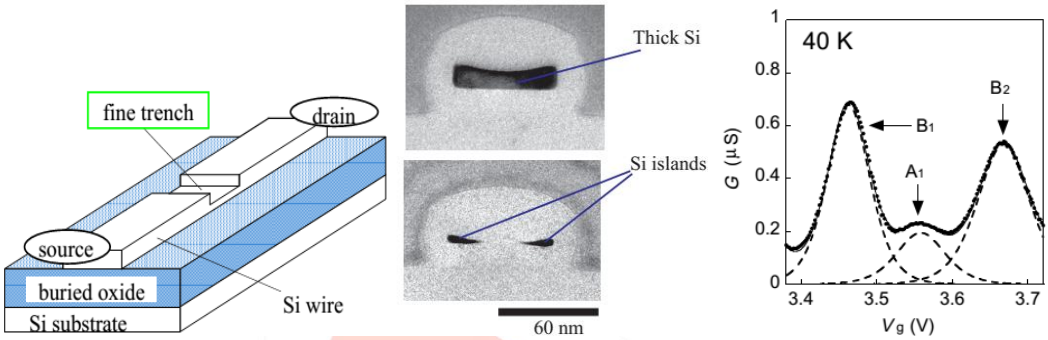
PADOX (Pattern-Dependent Oxidation) realized that a small Si pattern could be converted into a small SET when we observed that the amount of oxidation at particular point can be modulated in a way that depends on the initial pattern. This is the reason why we call this method Pattern Dependent Oxidation (PADOX) [28-29]. The structure fabricated on a thin SOI (Silicon On Insulator) wafer contains a narrow and short Si wire as shown in Fig 7.



(a) (b)

Fig 7(a).Initial device structure of the SET. We used a SIMOX (Separation by IMplanted OXygen) wafer, which is a type of SOI wafer.(b) Conductance oscillations as a function of the gate voltage measured at 300 K (room temperature) and at a drain voltage of 10 mV. Initial wire width, length and height were all 30 nm

PADOX converts the wire into a small island with a small tunnel capacitor at each end. The basic mechanism of this conversion is that the oxidation in the middle of the wire is suppressed due to stress accumulated during thermal oxidation while oxidation at the ends of the wire is enhanced due to both the supply of oxygen from the back and less accumulation of stress. The constrictions formed at both ends of the wire function as tunnel barriers. The SET is completed by forming a poly-Si gate over the island region, as shown in Fig.7(a). The advantages of this method are that an island smaller than the initially defined size can be made and that tunnel barriers are automatically formed at both ends of the wire. The characteristics of a SET fabricated by PADOX as in Fig. 7(b) indicate that the total capacitance of the SET island is as small as 1 aF [30, 31].
V-PADOX (Vertical Pattern-Dependent Oxidation) an alternative pattern-dependent oxidation method that can form twin SET islands. As shown in Fig. 8(a), the initial structure has a fine trench in the middle of a Si wire.

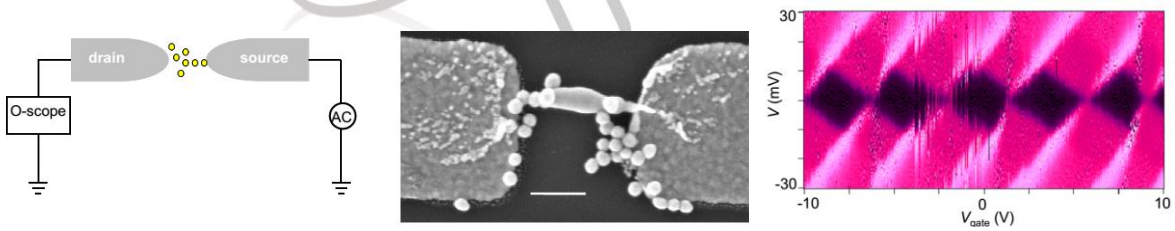


(a) (b) (c)

Fig 8. (a) Initial structure of the twin SETs before V-PADOX .(b) Cross-sectional TEM image of the Si wire after VPADOX. Initial thicknesses of the wire were 22 nm and 14 nm . Conductance oscillations of a twin-island SET.

Oxidation converts the edge regions of the thin Si layer under the trench into two small islands of about the same size; these islands are embedded in SiO_2 and are connected to the initially thicker Si layers by tunnel barriers that are formed automatically during oxidation.8(b) show cross-sectional TEM images of a thick and a thin Si wire, respectively. At both edges of the thin Si layer, small Si islands are formed in a self-aligned manner and the rest of the thin region is converted into SiO_2. This is because stress accumulation causes less oxidation to occur around the edges. It is noteworthy that the two tiny Si islands are formed without the need for lithographic definition of the islands themselves. As a result, two SETs connected in parallel to each other can be obtained by forming a gate electrode over the islands. Since the starting pattern of Si is vertically modulated, we call this method V-PADOX. Fig. 8(c) shows the gate voltage dependence of the conductance, measured at 40 K with a drain voltage of 10 mV, for a twin-island SET with a trench length L of 30 nm and a wire width W of 80 nm.

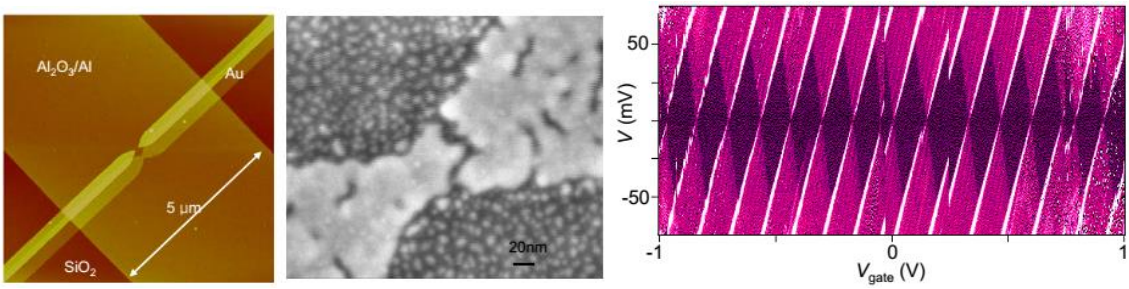
Several techniques have been developed to realize the fabrication of metallic SETs, such as high resolution electron-beam lithography [32,33], nanopore technique [34 , 35]. Electrostatic trapping of gold nanoparticles contains three steps [36] In the first step, gold nanobridge is formed by assembling gold nanoparticles between the electrodes with hundreds nanometer separation by AC electric field. Then, DC voltage is ramped up across the nanobridge; the bridge is broken due to current induced electromigration. This process consistently produces stable electrodes with sub-10 nanometer spacing.



(a) (b) (c)

Fig 9. Electrostatic trapping method to fabricate gold nanoparticle SETs in combination with electromigration technique. (a) A schematic diagram of electrostatic trapping experimental setup. (b) HRSEM image of a pair of electrodes with 400 nm gap bridged by a chain of 50 nm gold particles.(c) Two-dimensional plot of differential conductance as a function of bias voltage and gate voltage of a gold nanoparticle SET fabricated by using electrostatic trapping method. The dark (light) color corresponds to low (high) conductance.

To improve the yield of devices and gate coupling, the physical deposition method is introduced. This method consists of two steps. The first step is to fabricate the electrodes with sub-10 nm spacing by applying the electromigration process to the prefabricated Au nanowires [37, 38].

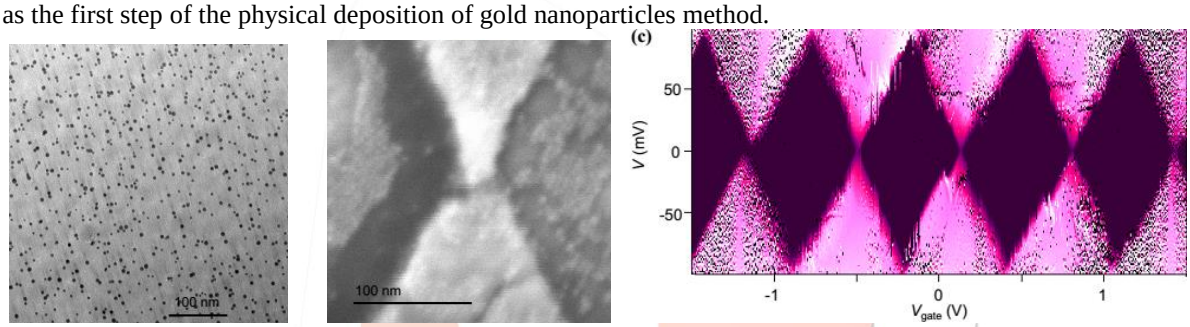


(a) (b) (c)

Fig 10. Gold nanoparticle SETs fabricated by using the physical deposition of gold nanoparticles. (a) AFM image of an gold nanowire on top of Al gate electrode. (b) HRSEM image of an SET with gold nanoparticles deposited into the nanogaps.(c) The conductance plot dark (light) color corresponds to low (high) conductance.

Then the SETs are realized by physical deposition of gold nanoparticles into the nanometer gaps between two electrodes. With this method, we can get gold nanoparticle SETs with relatively high yield. But the shape and size of gold nanoparticles are not well controlled.

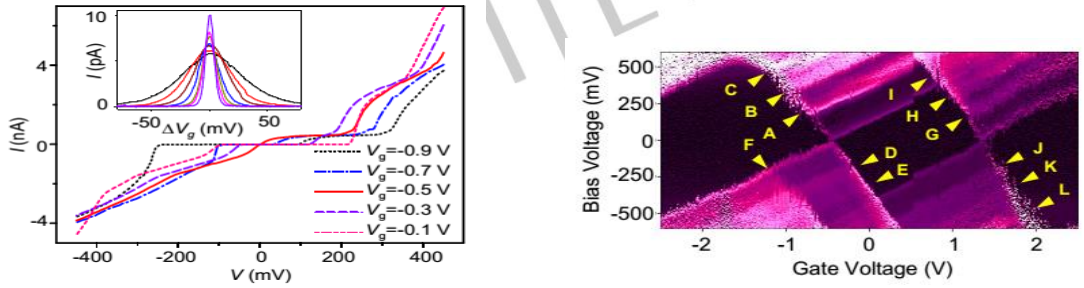
The third method is based on the self-assembly of colloidal gold nanoparticles within the gaps between two electrodes. Colloidal gold nanoparticles have well defined shape and uniform size distribution. They constitute a standard model to study the "electron-in-box" quantum states. This method contains two steps. The first step is to fabricate electrodes with nanometer scale separation. The process in this step involves applying electromigration to the gold nanowires at liquid helium temperature and is the same as the first step of the physical deposition of gold nanoparticles method.



(a) (b) (c)

Fig 11.Nanoparticle SETs fabricated by using the self-assembly of colloidal gold nanoparticles. (a) TEM image of 6 nmdiameter colloid gold nanoparticles. (b) HRSEM image of gold nanoparticles near the pre-created nanogap by electromigration of nanowires. (c) Two-dimensional plot of differential conductance as a function of bias voltage and gate voltage of agold nanoparticleSET fabricated by using self-assembly of gold nanoparticles.

Here discuss a simple method for the fabrication of room-temperature SETs based on the self-assembly of alkanedithiol molecules. Devices consist of spontaneously formed ultrasmall Au nanoparticles linked by alkanedithiols to nanometerspaced Au electrodes created by electromigration, devices are fabricated on oxidizedsilicon substrates.



(a) (b)

Fig 12.(a)Representative I–V characteristics from a device incorporatingC6 molecules at different gate voltages measured at 4.2 K. The inset shows the current as a function of gate voltage measured with a bias voltage of 0.5 mV at temperatures of 39.0, 25.1, 18.0, 12.3, 7.8, 6.2, and 4.2 K. A higher (lower) and narrower (wider) peak corresponds to lower (higher) temperature. The gate voltage is measured relative to the center of the current peak, which occurs at Vg = −0.5 V.(b) Two-dimensional color plot of differential conductance as a function of bias voltage and gate voltage measured at 4.2 K from the same C6 device.

III. SIMUALTION METHODS AND THEORY

3.1 How it is simulated?

There are three fundamentally different approaches to the simulation of single electron circuits: SPICE macro-modeling, Monte Carlo based and Master Equation based. One can distinguish between three fundamentally different approaches to the simulation of single-electron circuits: SPICE macro-modeling, Monte Carlo based and Master Equation based.

3.2 SPICE macro-modeling

One can model the IV characteristic ofa single-electron transistor the same way a bipolar or MOSFET transistor is modeled in SPICE[39]. The advantage is that SPICE is significantly faster than the typical single-electron simulator based on the Monte Carlo method or the Master Equation. This opens the potential to simulate very large single-electron circuits. The big disadvantage is that it does not capture any Coulomb interaction between adjacent transistors, which in many cases is very important for a correct circuit analyses. This deficiency could be remedied with a pre-processing step, which resolves all global dependencies before the actual single-electron simulation is performed [40].

3.3 The Monte Carlo approach

The Monte Carlo approach starts with all possible tunnel events, calculates their probabilities, and chooses one of the possible events randomly, weighted according to their probabilities. This is done many times to simulate the transport of electrons through the network. Tunnel events are considered to be independent and exponentially distributed. The orthodox single-electron theory yields a tunnel rate equation for any junction in a large circuit [41]

$$\Gamma(\Delta F) = \frac{\Delta F}{(e^2 R_T (e^{(\Delta F/Tk_B)-1})} \tag{3.1}$$

where ΔF is the change in free energy when an electron passes through the tunnel junction. R_T is the tunnel resistance and Γ the tunnel rate. The change in free energy which can be loosely understood as the change in system energy, has to be taken from the entire circuit. The calculation of ΔF can be efficiently done through the system capacity matrix. If this tunnel rate is coupled into a Poisson process the fundamental building blocks for a Monte Carlo based simulation are assembled. The Poisson distribution can be rearranged to yield

$$\tau = \frac{-\ln(r)}{\Gamma} \tag{3.2}$$

Where *r* is an evenly distributed random number from the interval [0,1] and t is the time at which an electron tunnel through the junction. The Monte Carlo procedure is then as follows. Starting from a list of all possible tunnel events with their particular tunnel rates under present biasing conditions, concrete random tunnel times $\tau\tau_i$ are computed for all events. The event with the smallest τ will happen first and is taken as the winner of the Monte Carlo step. Charges and voltages are updated on all circuit nodes. New tunnel rates are calculated and a new winner is determined through stochastic sampling. If this procedure is done many times, the macroscopic behavior of the circuit can be calculated.

3.4 Master's Equation Approach

The Monte Carlo method achieves its results by stochastic integration. Many events taken together in average yield the correct result. Alternatively one can find a set of equations to describe the charge transport processes in single-electron circuits, which can be solved deterministically

$$\frac{dP_i(t)}{dt} = \sum [\Gamma_{ij} P_j(t) - \Gamma_{ji} P_i(t)] \tag{3.3}$$

where Γ_{ij} denotes the transition rate from charge state j to state I and $P_i(t)$is the time dependent occupation probability of state i. This equation system is referred to as the Master Equation.The solution of above Master Equation is formally very easy. It is a matrix exponential. However, numerically it is quite difficult to evaluate a matrix exponential accurately for a general case. Since the number of possible states is infinite one has to find the ones that matter most. And this is for most circuits impossible to do a priory, either because any simple scheme would yield too many states making the matrix too large, or the few states which matter are unknown. One has to apply an adaptive scheme where one starts with a set of states or just one state and progressively searches the state space for more relevant states. For very small circuits the Master Equation has its advantages over the Monte Carlo method.

Table 2 Comparison between different method of simulation of SET.

Parameters	Spice Macromodel	Master's Equation	Monte Carlo Method
Simulation time	Low	High	High
Accuracy	Low	High	High
Columbic Blockade	Can not handle	Can handle	Can handle
Size of the circuit	Large	Very Small	Medium
Simulator	PSpice,HSPICE	Matlab, Spice	
SIMON,MOSES			

3.5 Simulators

The commonly used simulators are MOSES, SIMON, and KOSEC. These simulators have procedures to calculate the charge states of all the Coulomb islands altogether to take into account of the interaction between neighboring Coulomb islands. These procedures are usually based on the Monte Carlo technique and require a huge amount of computation time because the Monte Carlo method requires the calculation of the average charge states in each step and complete bookkeeping of all the steps are essential. Other simulators include SENECA,SPICE, etc.

3.5.1 MOSES Simulator

MOSES (Monte-Carlo Single-Electronics Simulator) is a single-electron tunnel device and circuit simulator that is based on a Monte Carlo method. It allows transient and stationary simulation of arbitrary circuits consisting of tunnel junctions, capacitors, and voltage sources of three kinds: constant, piecewise linearly time dependent, and voltage controlled. Co-tunneling can be simulated either with a half Monte Carlo method or with a full Monte Carlo method. MOSES is freely distributed in the Internet.

3.5.2 SIMON Simulator

SIMON is a single-electron tunnel device and circuit simulator that is based on a Monte Carlo method. It allows transient and stationary simulation of arbitrary circuits consisting of tunnel junctions, capacitors, and voltage sources of three kinds: constant, piecewise linearly time dependent, and voltage controlled. Cotunneling can be simulated either with a plain Monte Carlo method or with a combination of the Monte Carlo and master equation approach. SIMON tackles the problem of long simulation time taken when simulation uses Monte Carlo method by providing the option to simulate the cotunnel using a combination of Monte Carlo and Master Equation approach.

3.5.3 KOSEC Simulator

KOSEC (Korea Single Electron Circuit simulator) is developed in Nanoelectronics Laboratory, Korea University, Seoul, Korea. KOSEC employs the Monte Carlo methodas well. KOSEC is among the widely used simulator. However, not much information could be found on the web, which most probably is because its literature is in Korean language.

3.5.4 SENECA Simulator

SENECA is another important simulator for single electron circuits. SENECA directly solve the master equationfor the population probability of Coulomb islands.

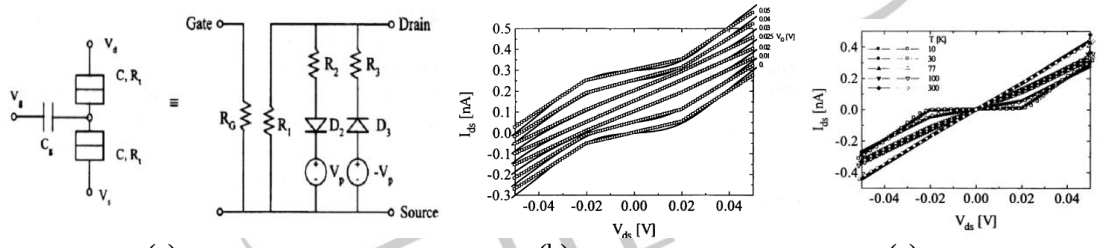
3.5.5 SPICE Simulator

SPICE stands for Simulation Program Integrated Circuits Especially. The program originates from the University of California, Berkeley. SPICE is used to provide a reasonably detailed analysis of circuits containing active components such as bipolar transistors, field effect transistors, diodes and lumped components such as resistors, capacitors and inductors. SPICE simulation of SET circuits is possible by the macro modeling of SETs. The macro modeling scheme is compatible with the standard method of SPICE simulation, consisting of the device modeling using an equivalent circuit, parameter extraction and subsequent circuit simulation.

IV. SIMULATION RESULTS

4.1 Model based on PSpice

Year – 1998: Author- Y.S.Yu [42]

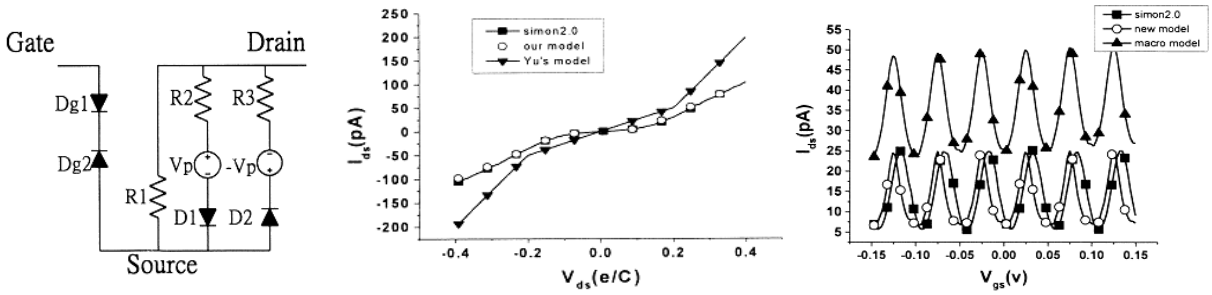


(a) (b) (c)

Figure 13: Macro-modeling of an SET (a) the equivalent circuit of an SET (b) The current-voltage characteristics of an SET at various gate biases. The solid lines are Monte-Carlo results and the empty symbols are obtained from the pro-posed macromodel.(c) The current-voltage characteristics of the SET of above figure at various temperatures.

An equivalent circuit of the SET and its macromodel code are successfully made and they are used for the simulation. But does not efficiently reprints the Monte Carlo method result. Simple model based on fitting and adjustment method and simulation times is very less by CPU.

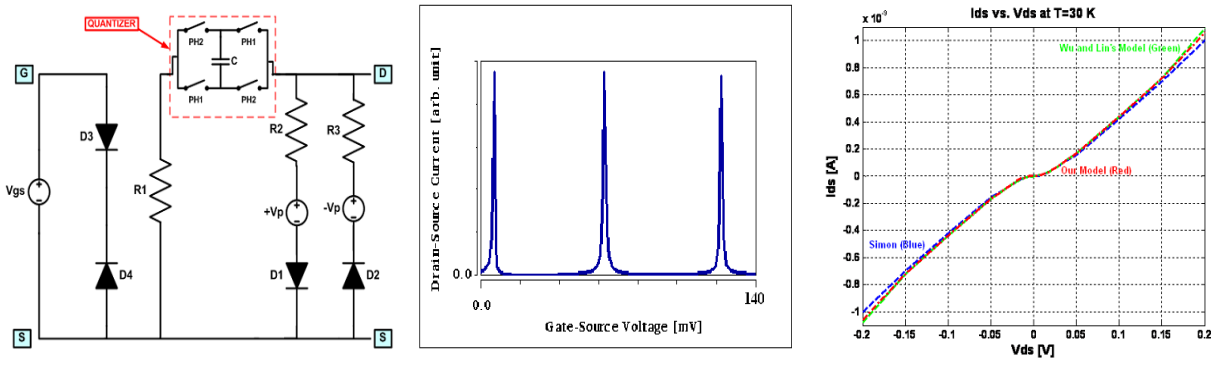
Year – 2003: Author - You-Lin Wu[43].



(a) (b) (c)

Figure 14. (a) Proposed new macro model for SET (b) Drain current vs Drain Voltage for the proposed model (c) Drain current vs the Gate voltage.

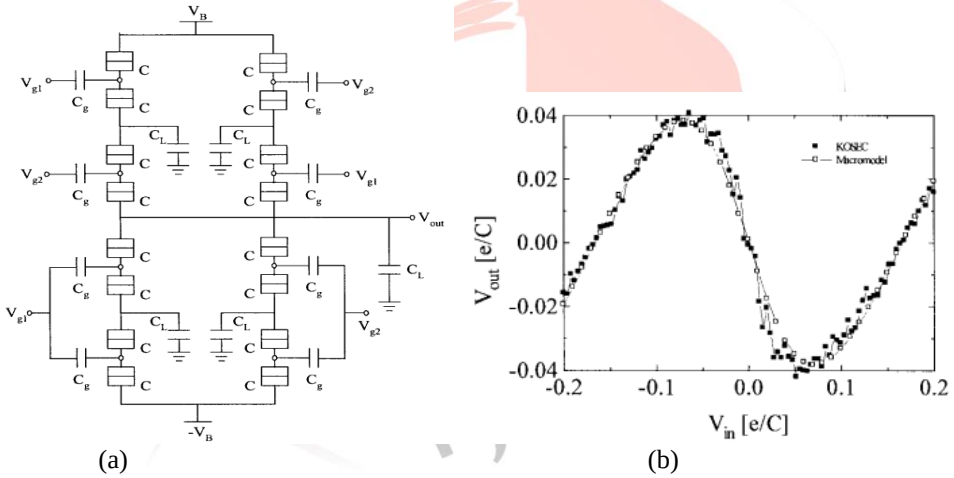
New proposed improved macromodel of SET the Gate should be capacitively coupled to Island is taken in the account .So the R_G is replaced by diode (face to face) to block all the possible current in the SET. when compared to Yu model I_{ds} is increased as because of the large resistance R_G so some amount of current was flowing which accounts for increased I_d.
Year – 2010: Author - Mohammad Reza Karimian and Massoud Dousti[44].



(a) (b) (c)

Fig.15. (a) SET SPICE Macro-model with quantizer block (b) Simulation result for the Coulomb oscillation of I_{ds} as function of V_{gs} (c) I_{ds} Vs V_{ds} characteristics.

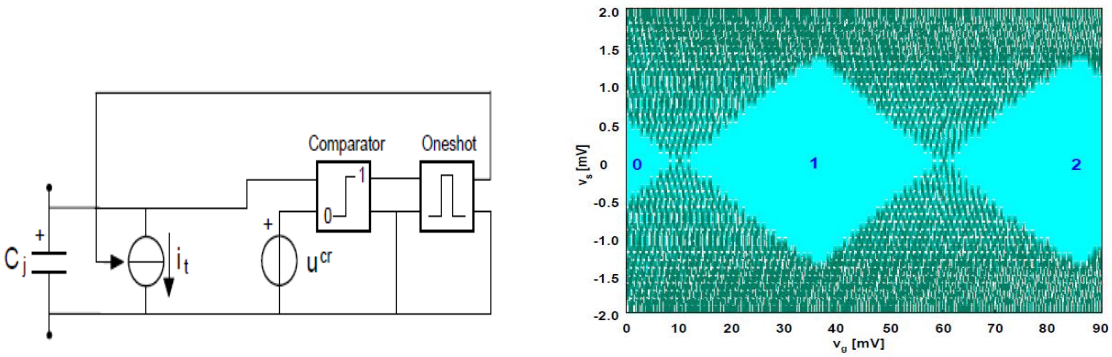
The concept of proposed model [17] is based on the phenomenon that the circuit, including SET junctions, can be described by a discrete charge transfer through the tunnel junctions. During this discrete charge transfer, the tunnel event is modeled as a quantizer block to obtain a quantified output signal on the island and the tunneling timeevaluation can be achieved with reasonable accuracy.
Year – 1999: Author - Yun SeopYu,Sung Woo Hwang,and Doyeol[45].



(a) (b)

Fig. 16. (a) Circuit diagrams for single-electron NOR gate consisting of eight SET's. (b) Voltage transfer characteristics obtained from the SPICE macromodel of the single electron NOR gate.

The basic circuit is based on the Yo Lin-Wu model of the SET in SPICE.SPICE macromodeling of single-electron transistors can be used for efficient circuit simulation like shown in fig. 16 for NOR gate. The developed macromodel produces simulation results with reasonable accuracy and with orders of magnitude smaller CPU time than usual Monte Carlo simulations.
Year – 2002: Author - Rudie van de Haar [46]

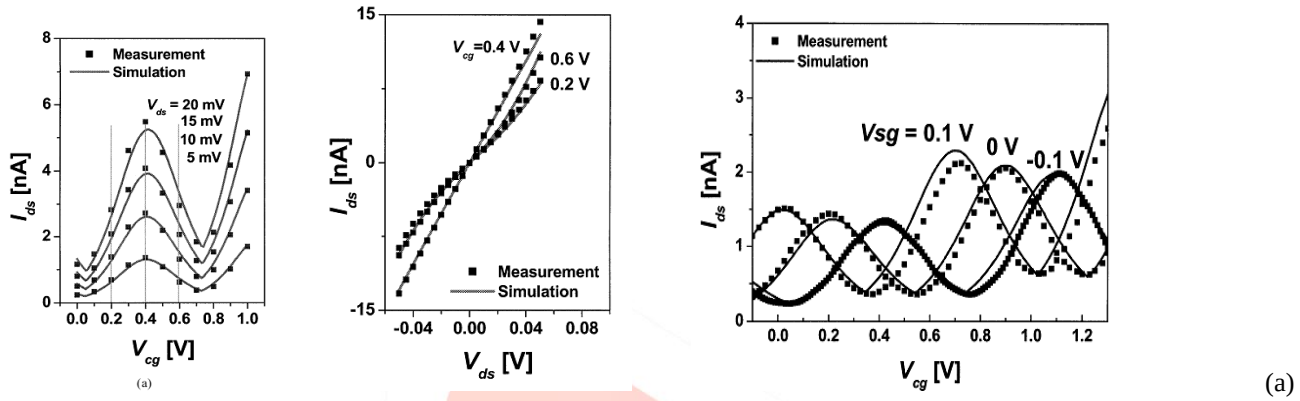


(a) (b)

Fig.17. Impulse model of the SET junction:(a) Complete SPICE model of a SET junction.(e) State diagram simulation result of the SET.

This model gives a description of the SET junction behavior in local variables and is therefore suitable for standard network theory applications. Because the model parameters are expressed in local variables, it is possible to model the SET junction itself instead of looking at a whole SET circuit, as the case for the Orthodox Theory of single electronics. This model is capable of simulating SET circuits in the single electronics current regime. In this current regime the low power properties of SET circuits are fully utilized.

Year – 2002: Author - Lee Kim and Yang[47]



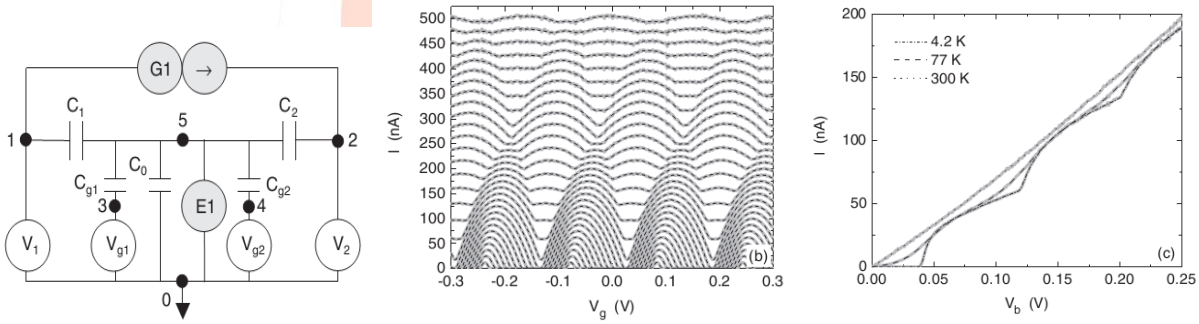
(a)

(b) (c)

Fig.18 (a)V_{CG} –I_{DS} curves and (b)V_{DS} –I_{DS} curves.(c)SET I–V characteristics of at various sidewall gate biases at 77 K ,V_{DS} =5mV,here C_G=0.24 aF.

A practical model for a single-electron transistor (SET) was developed based on the physical phenomena in realistic Si SETs, and implemented into a conventional circuit simulator. In the proposed model, the SET current calculated by the analytic model is combined with the parasitic MOSFET characteristics, which have been observed in many recently reported SETs formed on Si nanostructures , In terms of the bias, temperature, and size dependence of the realistic SET characteristics, an extensive comparison leads to good agreement within a reasonable level of accuracy. This SPICE model will be very useful for estimating the realistic performance of CMOS/ SET hybrid circuits or SET logic circuits.

Year – 2003: Author - Gunther Lientsching,IrekWeymann and Peter Hadley[48]



(a) (b) (c)

Fig.18 (a) The model of a SET in SPICE. The white voltage sources are external to the SET model and the gray sources are internal to the model.E1 is a voltage source that fixes the voltage of the island of the SET(node 5) and G1 is a current source that specifies the source-drain current.(b)Current voltage characteristics are plotted for three different temperatures (c) The current through the SET transistor is plotted against the gate voltage for bias voltages in step of 5mV.

A model was developed that uses the orthodox theory of single-electron tunneling and determines the average current through the transistor as a function of the bias voltage, the gate voltage, and the temperature in SPICE.

Year – 2004: Author – Cheng Jia's , Hu Chaohong, Sorin Dan Cotofana, and JiangJianfei[49].

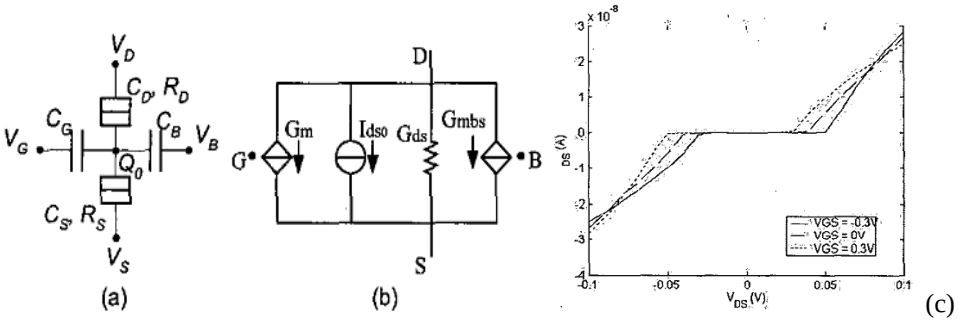


Fig.19 (a) SET Schematic (b) SET SPICE equivalent circuit (c) I_{DS} - V_{DS} curves of three-state simulation of SET with different V_{GS}.

This SPICE implementation is based on an analytical model derived from a simplified full master equation model .Besides of being able to accurately capture the SET behavior under various circuit and temperature conditions our proposal can also evaluate background charge effects in SET circuits. This is achieved by associating random seeds that model the random background charge noise effect to each SET in the circuit. Due to the simplicity of the compact current model we use our proposal leads to reduced simulation time and this makes it applicable for large-scale circuit simulation.
Year – 2005: Author - Y.S. Yu, S.W. Hwang and D. Ahn[50].

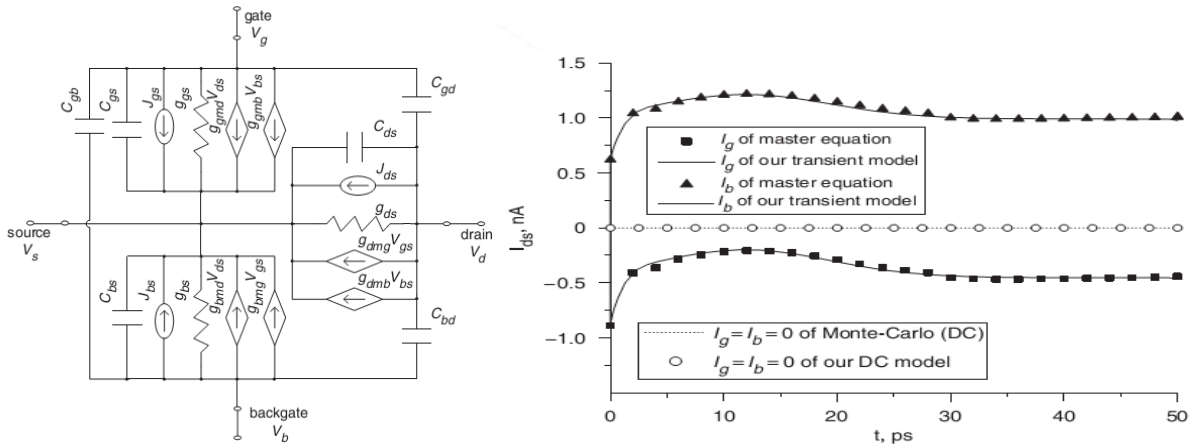


Fig .20 (a) Linearized equivalent circuit of the SET for SPICE implementation (b) show the terminal currents $I_d(t)$,$I_s(t)$,$I_g(t)$ and $I_b(t)$ of the SET when gate-source voltage V_{gs} varies linearly from 0 to 0.1V within the rising.

The developed model is based on a linearized equivalent circuit and the solution of a master equation is done by the programming capabilities of the Smart Spice. Exact delineation of several simulation time scales and the physics-based compact model make it possible to accurately simulate hybrid circuits in the timescales down to several tens of picoseconds.
Year – 2006: Author - A.Venkataratnam and A. K. Goel[51] .

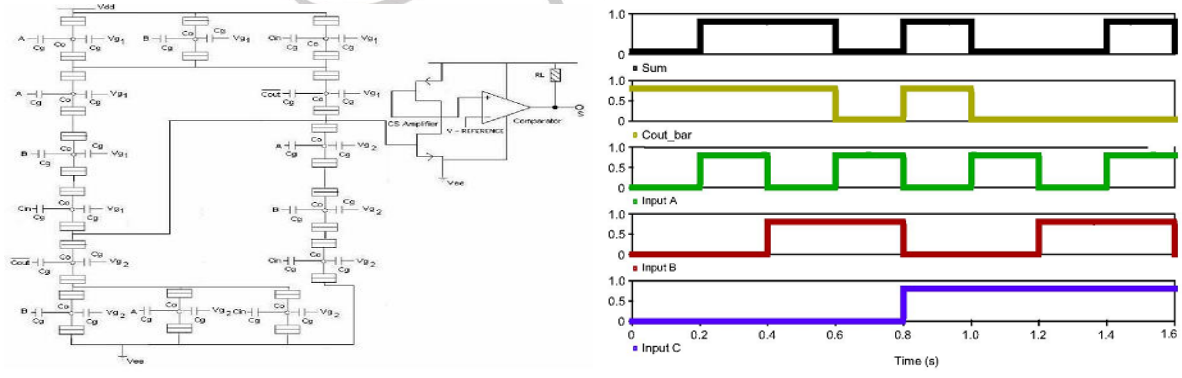
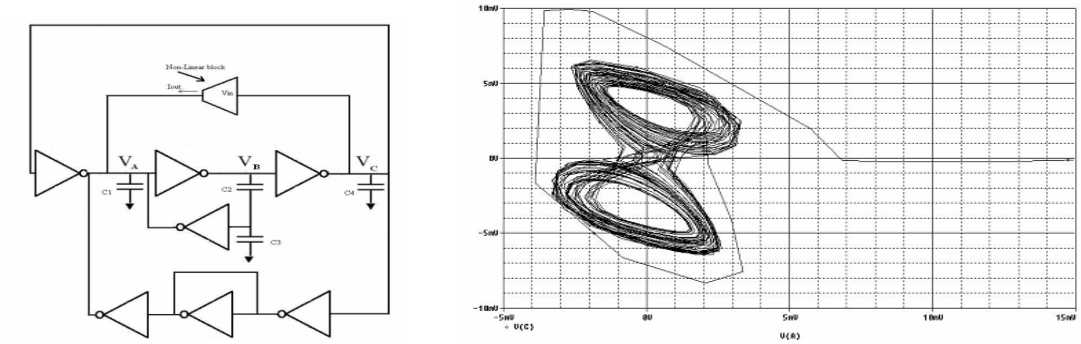


Fig. 21.(a) A SUM bit for a full adder based on this hybrid architecture is shown (b) I/O waveform of a Full Adder based on Hybrid Circuit with SET logic stage combined with a common source amplification stage and comparator.

Here author demonstrated hybrid architectures that combined SET's with conventional devices to perform logic operations. These hybrid architectures improve the voltage level at the output and thus improve the fan-out. SET circuits were simulated with a SPICE circuit simulation package using a text based SET-SPICE model developed by researchers at the Delft University in Netherlands (Lientschnig et. al., 2003). This model uses the orthodox theory to predict tunneling and it determines the average current through the transistor as a function of the bias voltage, the gate voltage and the temperature.

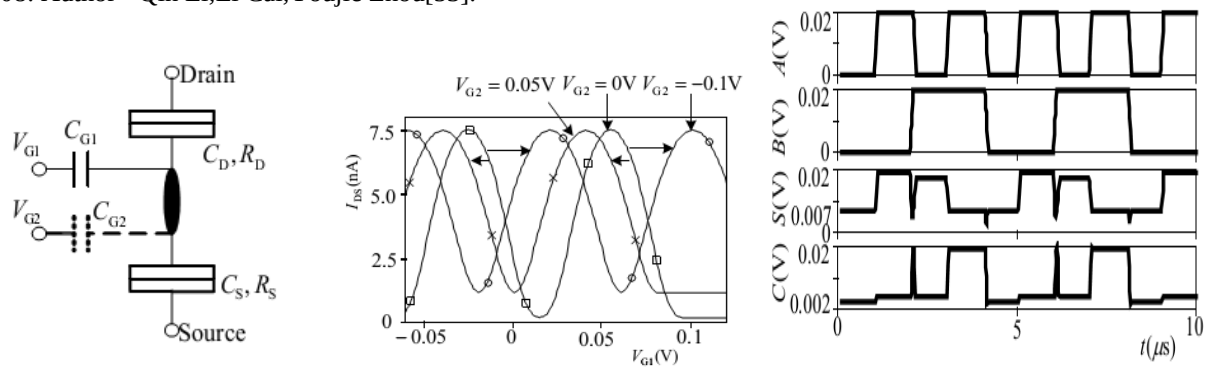
Year – 2007: Author - . Gaurav Gandhi, Tamás Roska and Árpád Csurgay[52].



(a) (b)

Fig. 22(a) The proposed Chua type chaotic double scroll circuit designed using SETs (b) Strange Attractor: Phase Plot between voltage at node A (X axis; 1 unit = 1mV) and Voltage at node C (Y axis; 1 unit = 1mv).

Year – 2008: Author - Qin Li,Li Cai,Youjie Zhou[53].



(a) (b) (c)

Fig.23: (a) Equivalent circuit of SET; (b) SET I-V characteristic (c) Input and output voltage signals of half adder.

Single-electron transistors and the MOS digital integrated circuit design concept, a good combination of single-electron transistors with MOS transistors is advanced to create a novel inverter, which, compared with the pure SET circuit, is considerably augmented in its voltage gain and drive capability. Then a close analysis was conducted of the inverter, on the basis of which other logic gates were presented. These logic gates are applied to the half adder circuit. The simulated result shows that these hybrid circuits share the merits with both SET circuits and MOS circuits. Compared with the traditional circuits, the two combinational logic circuits use fewer electronic components and are lower in power dissipation These make the proposed circuits have potential application in future digital circuit implementation.

Year – 2008: Author - A. Boubaker, A. Kalboussi [54].

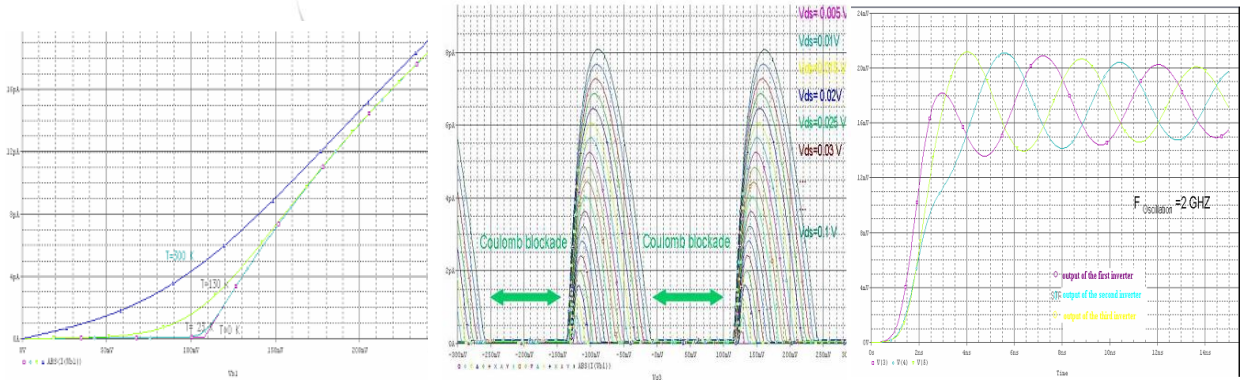


Fig.24 (a) Curves I_d-V_d at 0K, 23K, 130K and 300K (b) Ids current through the SET transistor is plotted against the gate voltage at T=0K (c) The voltages at the outputs of the inverters as a function of time.

The SET model based on the orthodox theory and solving the Master equation. it proposes a compact, physically based, analytical single-electron transistor (SET) circuits. One of the advantages of the model SET proposed in this paper was that it can be used to perform simulations of circuits where single electron transistors are combined with any other circuit elements.

Year – 2012: Author - Seed Sajjad Mosavi[55].

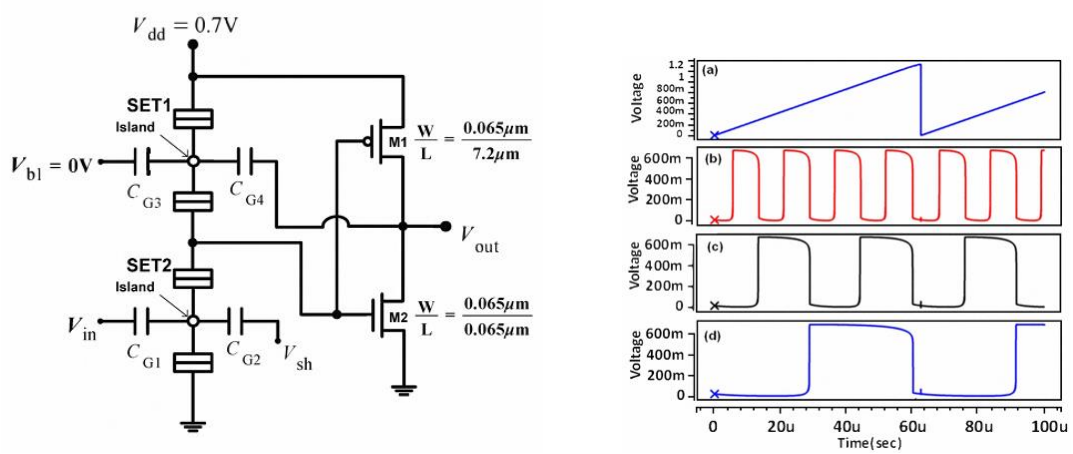
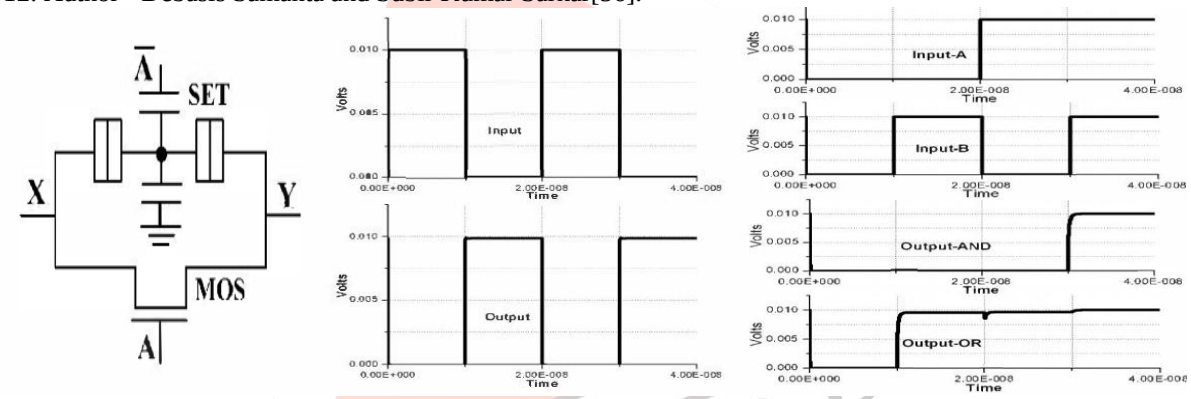


Fig 25. SET/MOS cell , simulation result of the SET/FEED cell for 3-bit ADC. (a)analog input voltage,(b)output digital DO,(c)output digital D1, (d) output digital D2 .

A new model of SET cell Hybrid of single electron transistor (SET) and MOS transistor called SET/FEED cell is proposed. In this new cell with connecting output to one of the single-electron transistors, the output voltage range is improved .All simulations were done at 65-nm technology and with O.7V power supply using MID model for the SET and 3-bit ADC circuit transistors by using H-SPICE simulator.

Year – 2012: Author - Debasis Samanta and Subir Kumar Sarkar[56].

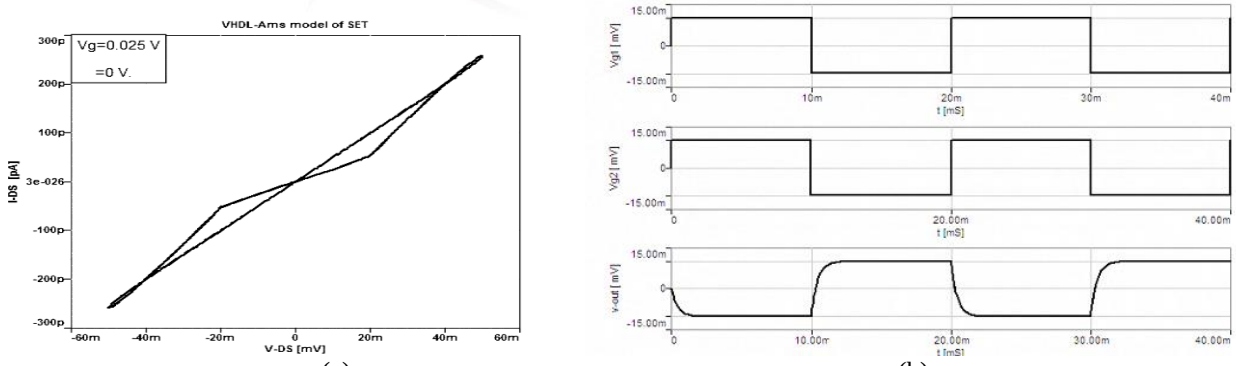


(a) (b) (c)

Fig. 26 (a) Basic structure of SET-MOS logic(b) Input- output waveforms of NOT gate.(c) Input - output waveforms of AND gate and OR gate.

4.2 VHDL Model

Year -2009: Author - A. M.EI-Shaerand A.A.A.Nasser[57].



(a) (b)

Fig.27 (a) Current-Voltage characteristics at various gate biases (b) Timing diagram of SET NOR.

The model is derived from a SPICE macro-model that was designed by Yu's. The SPICE macro-model was analyzed and simple equations were derived without complicated integrations used to calculate tunneling rates. These equations define the relation between voltages across and current through the island of an SET.A VHDL-AMS model is designed to describe these equations and the (I-V) characteristics are drawn and compared to the corresponding ones obtained by the SPICE macro-model.

4.3 SIMON Simulator .

Year – 1997: Author - Christoph Wasshuber [58].

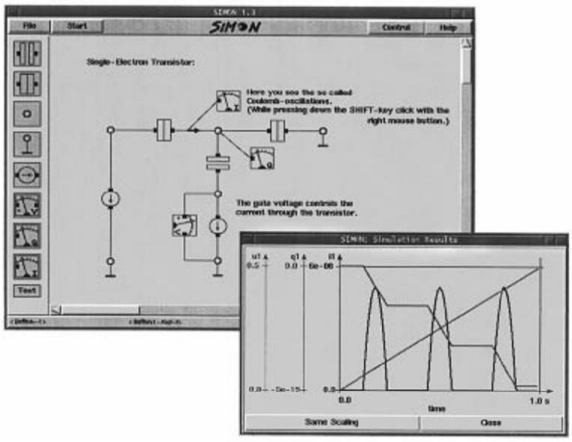
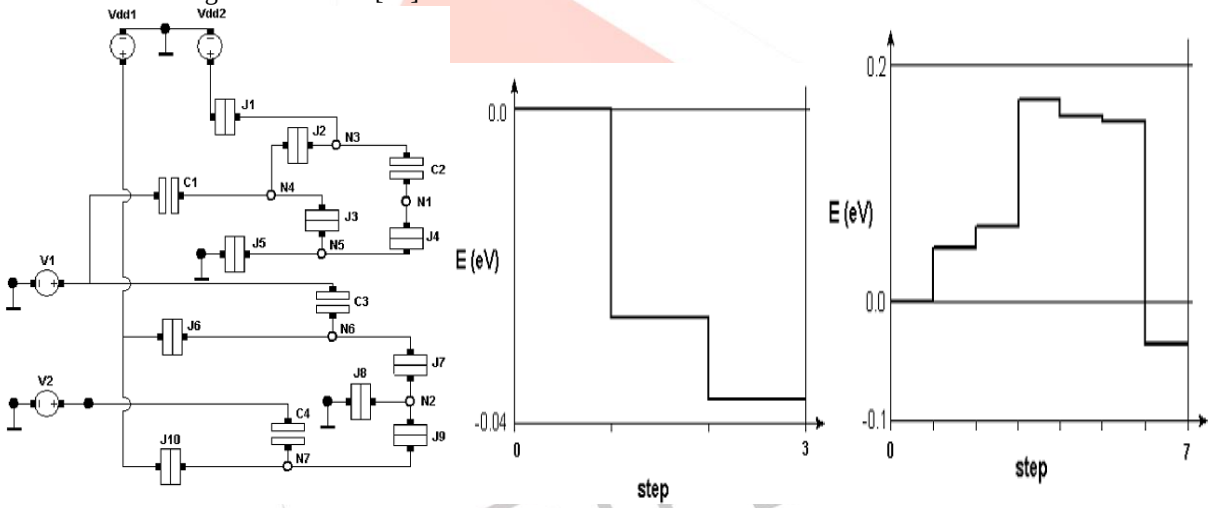


Fig. 28: Screenshot of SIMON software.

SIMON simulator a multipurpose SET device and circuit simulator capable of simulating transient and static behavior with and without co-tunneling. Co-tunneling can be accounted for with a plain Monte Carlo method or with a combination of the Monte Carlo method and master equation method. Simulator is implemented with a graphical user interface and a graphical circuit editor. It is currently used to test new circuits, and to understand the underlying fundamental phenomena and behavior, like Coulomb blockade and SET oscillations.

Year – 2006: Author - George T. Zardalidis[59].

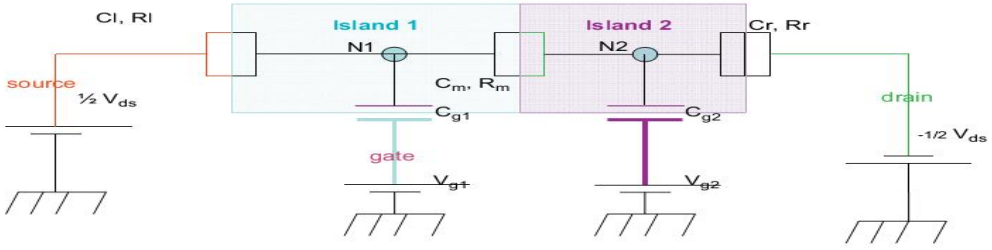


(a) (b) (c)

Fig.29 Free energy history of the circuit for the output transition from"0" to " 1". (b) Output node N2 to Vddl through N7 or N6, (c) Ground to output node N1 and ground to Vdd2 through N5,N4, N3.

Real time simulation of a single electron transistor and a single-electron control - not gate are presented. The logic operation of the control - not gate is verified using SIMON simulator. Bits of information are represented by the presence or absence of single electrons at conducting islands. The change in circuit free energy during the outputs transition from "0" to "1" has been calculated and the free energy history of the circuit, as it is provided by SIMON, as shown in the figure 29.

Year – 2009: Author - A. Boubaker[60]



(a)

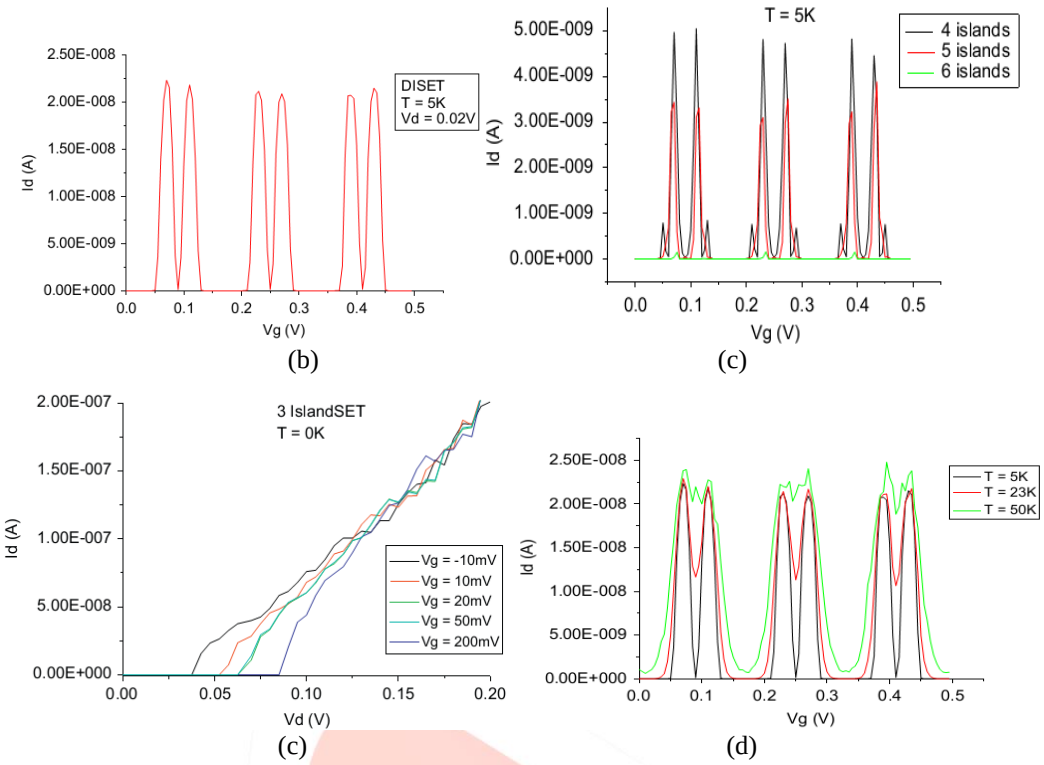


Fig.30: (a) Schematic circuit diagram of a DISET.(b) Coulomb oscillations obtained on DISET at T = 5K for V_d = 0.02V.(c) I_d–V_g characteristics of MISET, respectively, for 4, 5 and 6 islands simulated at T = 5K (d) Simulated I_d–V_d characteristics of the SET. (e) Coulomb oscillation of DISET for different temperatures (T=5, 23 and T=50K).

Using SIMON simulator, investigate the electrical characteristics of single-electron transistors (SETs) based on multiple islands and show the temperature dependence of the Coulomb oscillation of the SET with one to six islands as a function of gate voltage V_g in the temperature range from T=5 to 50K. Values of current tend to increase proportionally with temperature .For a high drain voltage, the MISET behaved as a single-island device. This is probably because the multiple islands were electrically enlarged and merged into a single island owing to the high applied drain voltage.
Year – 2010: Author – Aïmen Boubaker[61].

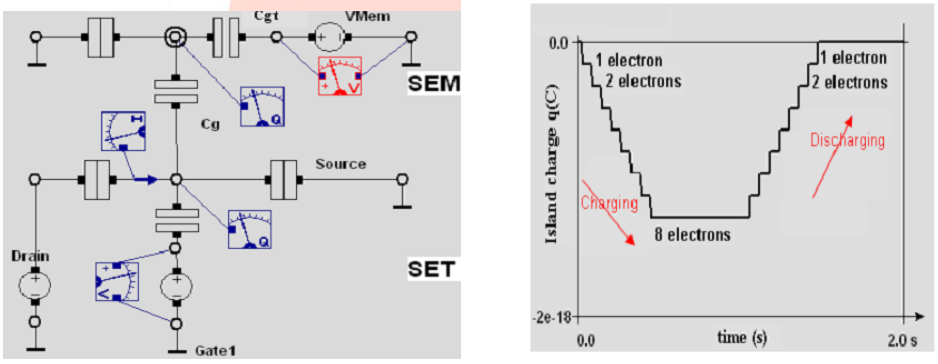
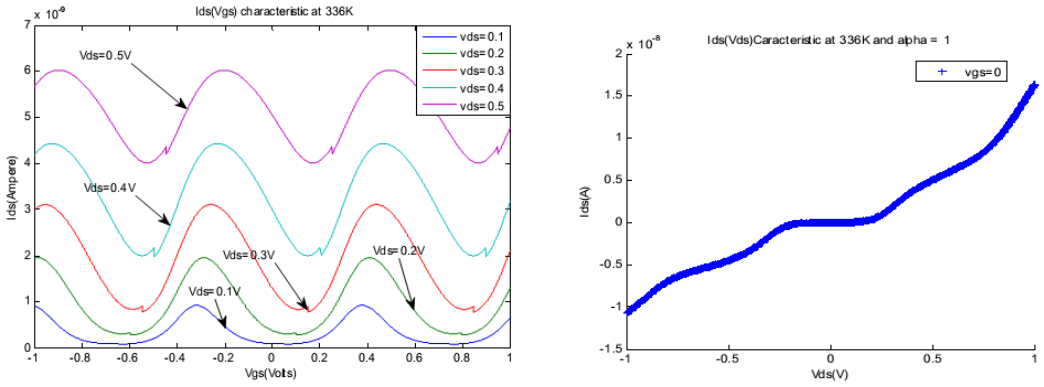


Fig.31 (a) Electrical model of the physical architecture using SIMON of SET/SEM (b) Quantization of the electric charge in the write /erase phases as a function of time.

A memory bloc, with a voltage source V_{Mem}, a pure capacitor connected to a tunnel junction through a metallic memory node coupled to the second bloc which is a Single Electron Transistor "SET" through a coupling capacitance.They verified the design of the SET/SEM cell by the SIMON tool, Above figure presents the SIMON simulation result and shows that there are 8 electrons in the memory node after the charging. Since energy levels are discrete, each state of charge or energy level is associated with an addition of an electron. For a shaft with 8 energy levels, each equal to one bit.
Year – 2012: Author - Amine Touati[62].



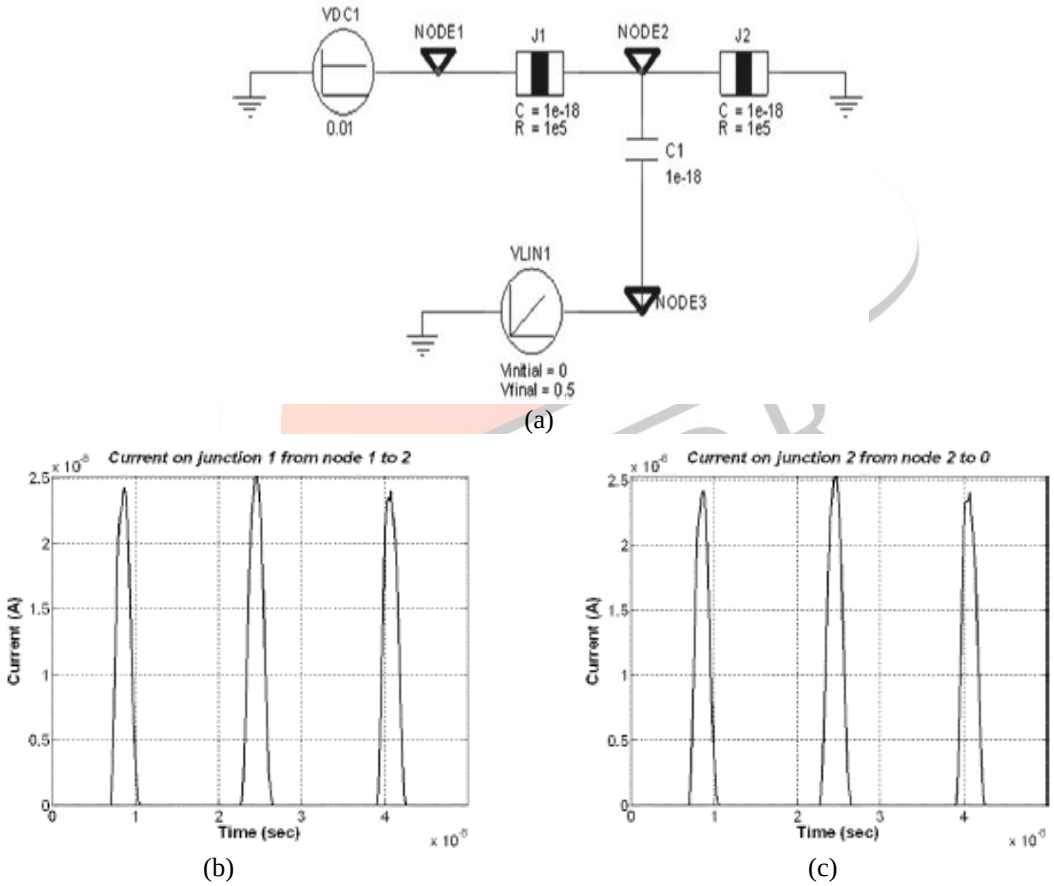
(a) (b)

Fig.32 : (a) Coulomb oscillations of SET obtained by Amine model at T = 336 K for different V_{DS} voltages.(b) I_{DS}-V_{DS} empirical model validation for T = 336 K .

The drain-source current as well as gate-source of single-electron transistors (SETs) at high temperature. model consists on summing the tunnel current and thermionic contribution. The model is base on the Master's Equation approach and simulated in SIMON. For high temperature operation both Tunnel Current (I_{DS}) and Thermionic contribution $I_{DS,thermionic}$ is taken into account. Proposed Model gives an accurate result when compared the experiments ones at high temperature .

4.4 SECS

Year – 2008: Author - George Zardalidi[63].



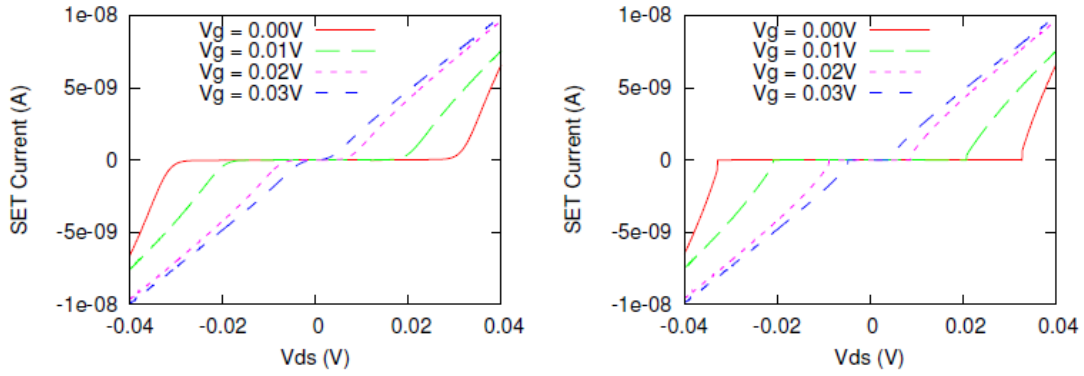
(a) (b) (c)

Fig.33 (a) Single electron transistor designed with the SECS simulation system (b)Current of junction J1 (c)Current of junction J2.

The operation of single electron circuits is based on the tunneling effect. The stochastic nature due to tunneling is incorporated in the simulation of single electron circuits using the Monte Carlo method. The novelty of the SECS system is that it provides the behavior of single electron circuits in an actual time scale, making thus easier and more complete the study of the phenomena that take place at an arbitrary single electron circuit.

4.5 SEMSIM

Year -2008: Author – Nicoloas Allac[64].



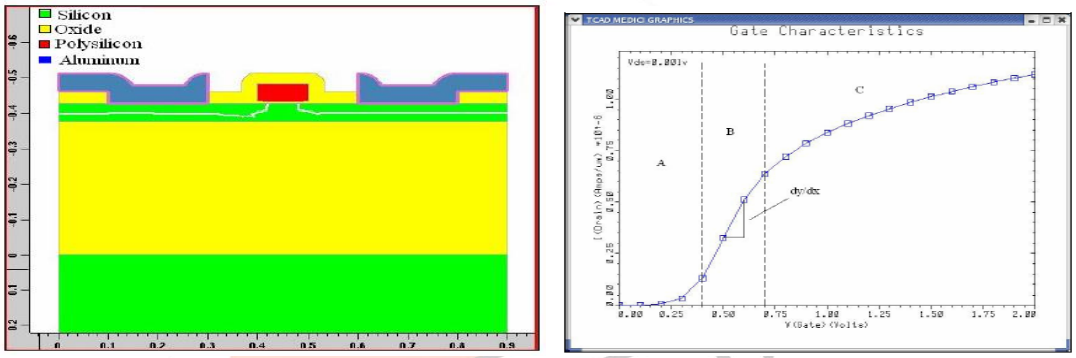
(a) (b)

Fig. 34. SEMSIM simulation result at T=5K for various gate voltages of the SET. The Columbic blockade region can be seen as the suppression of current nearV_{ds} =0V(b)SEMSIM simulation results at T= 50 mK for various gate voltages of a superconducting SET The suppressed current region is enlarged due to the superconducting gap.

Nicholoas introduced a adaptive technique for Monte Carlo simulation of single-electron devices. The proposed adaptive technique was validated against non-adaptive Monte Carlo and SPICE simulations using 15 logic benchmarks, which contain from 38 to 3494 devices. Simulation times, compared to the non-adaptive approach, were reduced by up to 40 times while the average error was 3:3%. They propose an adaptive algorithm, which reduces simulation time significantly by reducing the number of calculations that are carried out after each tunneling event.

4.6 TCAD

Year – 2006: Author - Uda Hashim, Amiza, Rasmi[65].



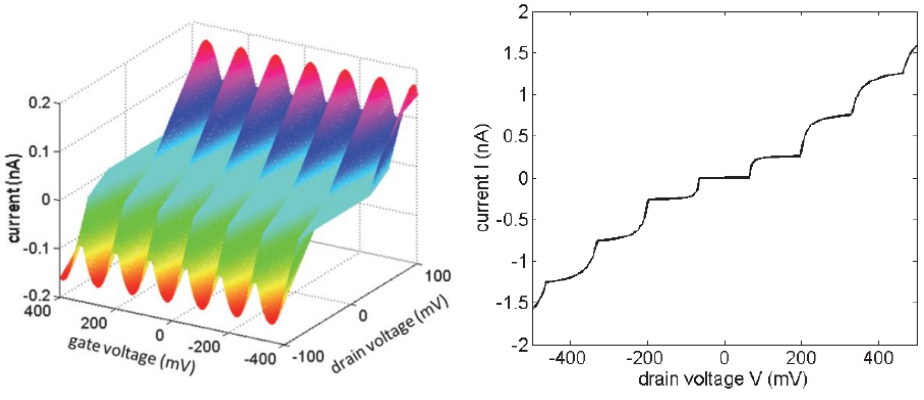
(a) (b)

Fig.35: (a) Cross-section view of the device structure after completion of metallization process (b) Drain current, I_D as a function of the gate voltage V_G

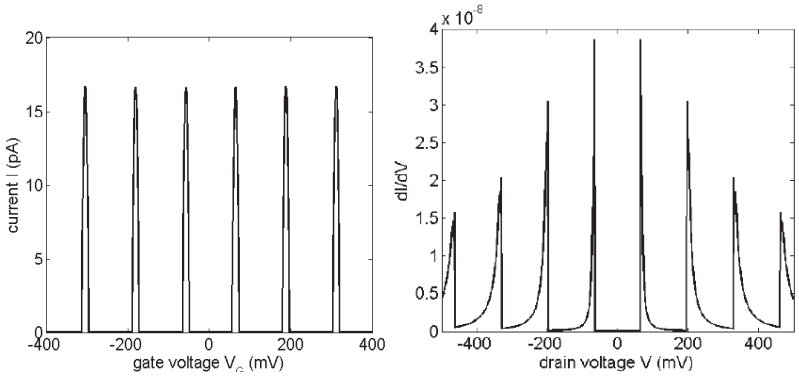
The power, *P* of this SET device is obtained from the I_D-V_G graph with fixed the resistance, *R*. The resistance, *R* is 0.4190 x 10^6 W. The value of capacitance that obtained in this simulation is smaller and the charging energy is higher than the previous reported.

4.7 MATLAB

Year -2006: Author - Ratno Nuryadi [66].



(a) (b)



(c) (d)

Fig. 36:3D current – voltage characteristics for the SET. The range of source-drain voltage is from -100 mV to 100 mV and gate voltage is from -400 mV to 400 mV.) (b) The current – drain voltage characteristics for SET (c)The current – gate voltage characteristics for SET (d) dI/dV curve

Simulated results produce the staircase behavior in the current-drain voltage characteristics and periodic oscillations in current-gate voltage characteristics. These results reproduce the previous studies of the SET, indicating that the simulation technique achieves good accuracy.

V. CONCLUSION

Single Electronic Transistor (SET) has proved their value as tool in scientific research. Resistance of SET is determined by the electron tunneling and the capacitance depends on the size of the nanoparticle. A SET is a three terminal device in which electrons are transferred one by one using columbic blockade effect. The current starts to flow through the junction when applied voltage is just sufficient to raise the energy of electron above the coulomb blocked. Modeling and simulation of SET are very important to understand the behavior and characteristics of electron before start designing and fabrication of device. SPICE is significantly faster than the typical single-electron simulator based on the Monte Carlo method or the Master Equation but big disadvantage is that it does not capture any Coulomb interaction between adjacent transistors, Monte Carlo method can be traded for accuracy with simulation time, Master's Equation is bit slow but gives high accuracy result. In this work the macro model, Monte Carlo method are reviewed for further investigation.

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