Design and Verification of Asynchronous Five Port Router for Network on Chip

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Abstract—**Multiprocessor system on chip is rising as a replacement trend for System on chip style however the wire and power style constraints square measure forcing adoption of recent style methodologies. Researchers pursued a ascendable answer to the current downside i.e. Network on Chip (NOC). Network on chip design higher supports the combination of SOC consists of on chip packet switched network. so the thought is borrowed from massive scale multiprocessors and wide space network domain and envisions on chip routers primarily based network. Cores access the network by means that of correct interfaces and have their packets forwarded to destination through multichip routing path. so as to implement a competitive operative design, the router ought to be expeditiously style because it is that the central element of operative design .Design and simulation of five Port Router was designed and its simulation was through with ModelSim6.5e and synthesis victimization Xilinx Ise10.1i.**

***Index Terms*—NOC, SOC**

I. INTRODUCTION

The challenge of the confirmative an oversized style is growing exponentially. There's a necessity to outline new strategies that creates practical verification straightforward. Many ways within the recent years are projected to realize smart practical verification with less effort. Recent advancement towards this goal is methodologies. The methodology defines a skeleton over that one will add flesh and skin to their necessities to realize practical verification. OVM (open verification methodology) is one such economical methodology and smartest thing regarding it's, it is free. This ovm is made on system Verilog and used effectively to realize maintainability, reusability, speed of verification etc. This project is geared toward building a reusable check bench for confirmative eight Port Router Protocol Bridge by exploitation system Verilog and ovm.

In this document the utilization of ovm and system Verilog to verify a style and to develop a reusable check bench is explained in step by step as outlined by verification principles and methodology. The check bench contains totally different parts and every element is once more composed of subcomponents, these parts and subcomponents may be reused for the longer term comes as long because the interface is same.

II. ROUTER

System on chip may be a complicated interconnection of varied practical parts. It creates communication bottleneck within the gigabit communication attributable to its bus based mostly design. so there was would like of system that express modularity and correspondence, network on chip possess several such engaging properties and solve the matter of communication bottleneck. It primarily works on the thought of interconnection of cores exploitation on chip network. The communication on network on chip is meted out by suggests that of router, therefore for implementing higher intelligence agent, the router ought to be with efficiency style. This router supports four parallel connections at identical time. It uses store and forward sort of flow management and FSM Controller settled routing that improves the performance of router. The shift mechanism used here is packet shift that is usually used on network on chip.

In packet shift the info the info transfers within the sort of packets between cooperating routers and freelance routing call is taken. The shop and forward flow mechanism is best as a result of it doesn't reserve channels and therefore doesn't cause idle physical channels. The arbiter is of rotating priority theme so each channel once gets likelihood to transfer its information. During this router each input and output buffering is employed so congestion is avoided at each side.

A router could be a device that forwards information packets across pc networks. Routers perform the info "traffic direction" functions on the net. A router could be a microprocessor-controlled device that's connected to 2 or additional information lines from completely different networks. Once a knowledge packet comes in on one in all the lines the router reads the address info within the packet to work out its final destination. Then, victimization info in its routing table, it directs the packet to following network on its journey.

III. ROUTER STYLE CONSIDERATION

For most home users, they will wish to set-up a local area network (local space Network) or WLAN (wireless LAN) and connect all pcs to the net while not having to pay a full broadband subscription service to their ISP for every computer on the network.

In several instances, associate ISP can enable you to use a router and connect multiple pcs to one web association and pay a nominal fee for every further computer sharing the association. This is often once home users can wish to seem at smaller routers, usually known as broadband routers that alter 2 or additional computers to share an online association. Inside a business or organization, you ought to connect multiple computers to the net, however conjointly wish to attach multiple personal networks not all routers are created equal since their job can take issue slightly from network to network. To boot, you'll consider a chunk of hardware and not even comprehend it could be a router.

Broadband or ICS routers can look to a small degree completely different betting on the manufacturer or whole, however wired routers are usually a tiny low box-shaped hardware device with ports on the front or into that you plug every pc, alongside a port to enter your broadband electronic equipment. These association ports enable the router to try and do its job of routing {the information |the info| the information} packets between every of the computers and also the data attending to and from the net.

Depending on the kind of electronic equipment and web association you've got, you may conjointly select a router with phone or fax machine ports. A wired local area network broadband router can generally have a constitutional local area network switch to permit for enlargement. These routers conjointly support NAT (network address translation), that permits all of your computers to share one IP address on the net. Web association sharing routers also will give users with a lot of required options like associate SPI firewall or function and a DHCP Server.

IV. FIVE PORT ROUTER DESIGN

The router could be a" 5 Port Network Router" incorporates a one input port from that the packet enters. It's seven output ports wherever the packet is driven out. Packet contains three elements. They Header, information and frame check sequence. Packet dimension is eight bits and also the length of the packet is between one bytes to sixty four bytes. Packet header contains 3 fields DA and length. Destination address (DA) of the packet is of eight bits. The switch drives the packet to individual ports supported this destination address of the packets. Every output port has 8-bit distinctive port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the information is of eight bits and from zero to sixty three. Length is measured in terms of bytes. Knowledge ought to be in terms of bytes and may take something. Frame check sequence contains the safety check of the packet. It's calculated over the header and knowledge.

Router could be a packet primarily based protocol. Router drives the incoming packet that comes from the input port to output ports supported the address contained within the packet

The router incorporates a one input port from that the packet enters. it's 3 output ports wherever the packet is driven out. The router has a full of life low synchronous input reset n that resets the router.

Data packet moves in to the input channel of 1 port of router by that it's forwarded to the output channel of different port. Every input channel and output channel has its own decryption logic that will increase the performance of the router. Buffers area unit gift in the slightest degree ports to store the information quickly.

The buffering methodology used here is store and forward. Management logic is gift to create arbitration selections. Therefore communication is established between input and output ports... In step with the destination path of information packet, management bit lines of FSM area unit set. The movement of information from supply to destination is named switch mechanism the packet switch mechanism is employed here, within which the flit size is eight bits .Thus the packet size varies from zero bits to eight bits. An in depth rationalization of style is as follow.

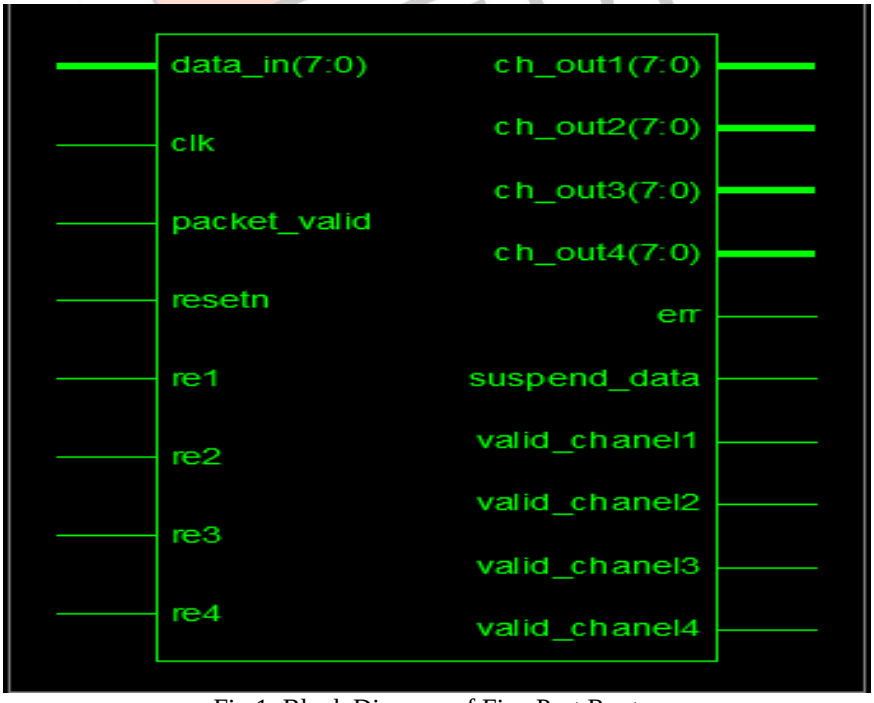

Fig 1: Block Diagram of Five Port Router

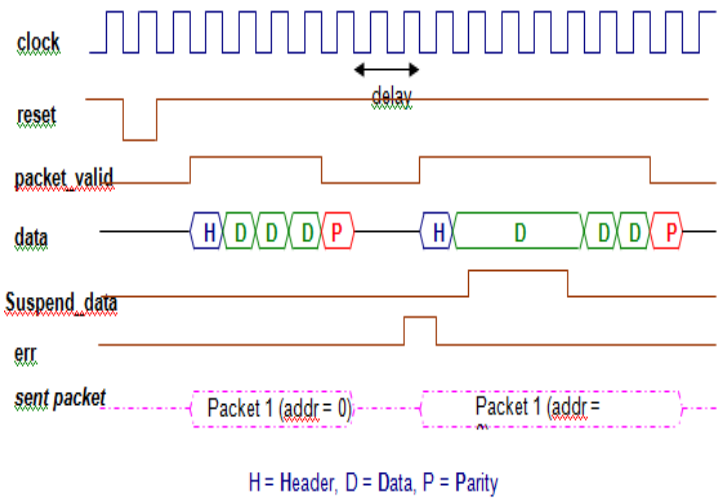

Fig 2: Router Input Protocol

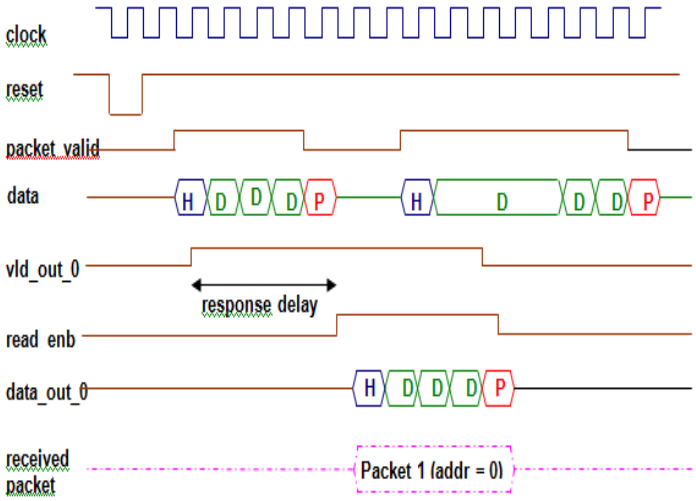

Fig 3: Router output Protocol

V. ROUTER ANCHITECTURE

The Five Router Design is done by using of the three blocks .the blocks are 8-Bit Register, Router controller and output block. the router controller is design by using FSM design and the output block consists of Four FIFO's combined together the FIFO's are store packet of data and when u want to data that time the data read from the FIFO's. In this router design has three outputs that is 8-Bit size and one 8_bit data port it using to drive the data into router we are using the global clock and reset signals, and the err signal and suspended data signals are output's of the router .the FSM controller gives the err and suspended_data_in signals .this functions are discussed clearly in below FSM description.

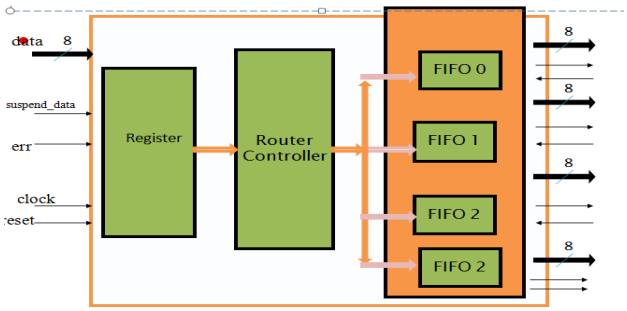

Fig 4: Five port Router Block Diagram

VI. REGISTER BLOCK

This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock.

Data registers latches the data from data input based on state and status control signals, and this latched data is sent to the FIFO for storage. Apart from it, data is also latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. An error signal is generated if packet parity is not equal to the calculated parity

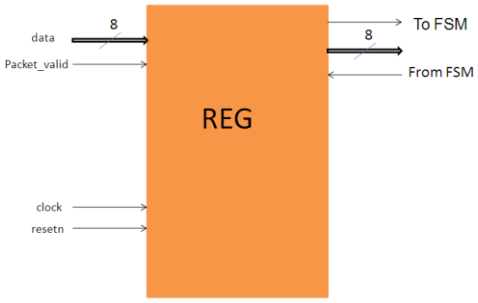

Fig 5: Router Output Block

There square measure seven fifos employed in the router style. Every FIFO is of eight bit dimension and sixteen bit depth. The FIFO works on system clock. it's synchronous signaling reset. If reset n is low then full =0, empty = one and data_out = zero. The FIFO has doing seven regardful operations

- Write Operation
- Read operation

Read and Write Operation

The practicality of FIFO justify below

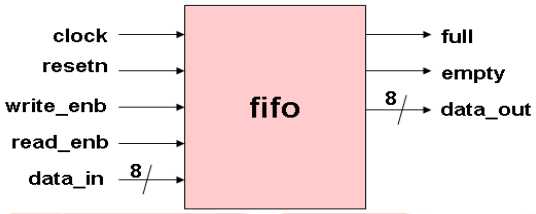

Fig 6: Four port Router FIFO

1. Write Operation - The FIFO write operation is completed by once the information from input data_in is sampled at rising fringe of the clock once input write_enb is high and FIFO isn't full. in this condition only FIFO Write operation is completed.

2. Read Operation - The FIFO browse Operation is the information is browse from output data_out at rising fringe of the clock, once read_enb is high and FIFO isn't empty. Read and Write operation are often done at the same time.
   Full – it indicates that everyone the locations within FIFO have been written. Empty – it indicates that everyone the locations of FIFO area unit empty.

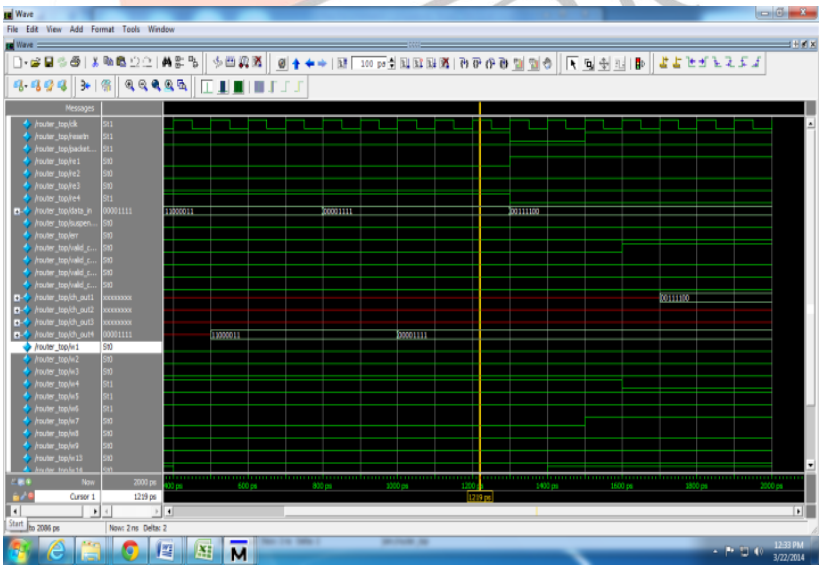

Fig 7: 5 Port Router Output

VII. CONCLUSION

In this paper awe planned a5 Port router style for effective knowledge transfers its simulation and synthesis was done victimization the Verilog secret writing.

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