Reduction of Leakage Power of Full Adder using Variable Body Biasing with sleep insertion

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***Abstract* - Reduction of leakage Power is the major problem in digital circuits. There are various techniques that are used to reduce the leakage power. Variable Body Biasing technique is discussed in this paper. Variable body biasing technique with sleep insertion technique is one of the efficient technique for designing combinational digital circuits which significantly cuts down the leakage current without increasing the dynamic power dissipation, sleep insertion technique is also added along with variable body biasing technique so that there is no loss of state as in sleep stack technique. This thesis proposed a technique that reduces both power dissipation and glitches. This technique is based on two methods first is variable body biasing and the other is sleep insertion technique. Pass transistor is also added in the circuitry in order to eliminate glitches if any. The existing leakage reduction techniques like sleepy keeper and stack technique are having drawbacks like increased area and delay. Other delay elements that are used for reduction in glitches takes larger area when compared with pass transistor. This new proposed approach eliminates leakage power along with glitches keeping in mind all the drawbacks of all the earlier techniques. All the performance has been investigated using 90nm Technology at 1 voltage and evaluated by the comparison of the simulation result obtain from TSPICE.**

***Keywords* - VBBT, Delay, leakage power, sleep insertion technique**

I. INTRODUCTION

Complementary metal oxide semiconductor (CMOS) technology is used in all modern digital logic circuits. The power spent in CMOS can be classified as dynamic power consumption and leakage or static power consumption. Dynamic power consumption is due to the low impedance path between the rails formed through the switching devices. When input is given to the gate, there would be occurrence of one or more transitions at the output. At the output of the gate there are two types of transitions occurs, one which is due to actual transmission of the input signal resulting in desired functioning of the logic gate, is also called as functional transition Second, is due to transmission of unnecessary pulses through the logic gate resulting in undesired functioning of the gate, this is called as spurious transition. These spurious transition at the output of a logic gate is an outcome of difference in arrival time of various inputs. These unnecessary signals at the output of logic gate are known as glitches. Glitch power in modern circuits account for 20 to 70% [1] and it is 7 to 43% [2] of the dynamic power consumption. There are various published techniques to eliminate glitches in the logic circuits to accompany desired functioning of the logic circuit.

However, low-power design usually involves making tradeoffs such as timing versus power and area versus power. Increasing performance, while the power dissipation is kept constant, is also considered to be a low-power design problem. In fact, higher performance-per-watt is the new technique for micro-processor chip manufacturers today. In order to achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this trend, transistor leakage power has increased exponentially. The reduction of the supply voltage is dictated by the need to maintain the electric field constant on the ever shrinking gate oxide.

II. CONVENTIONAL FULL ADDER

It is a combinational circuit which results in arithmetic sum of three bits. The Full adder has three input terminals and single output terminal. The Two inputs are denoted by A and B, and they denotes the two significant bits on that the addition function to be performed. The last i.e, third input Cin, denotes the carry from previous lower significant position.

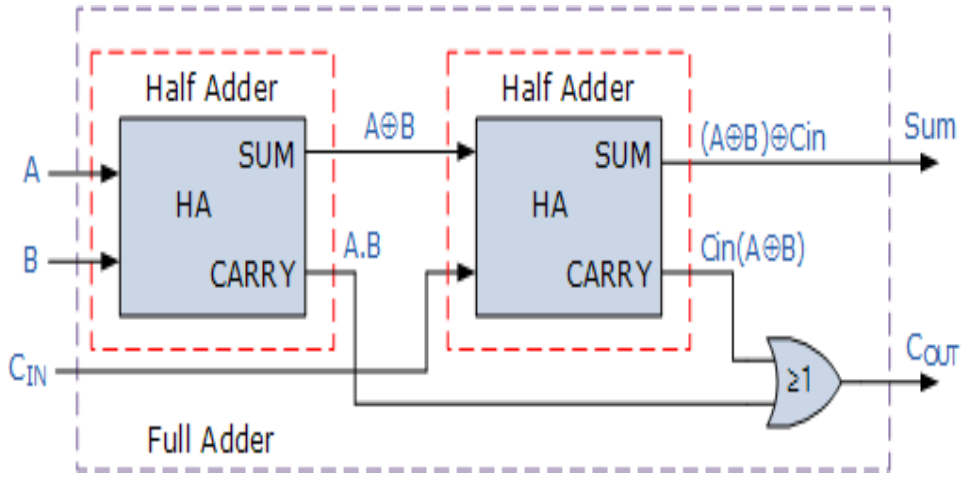

Fig 1: Full Adder Block diagram

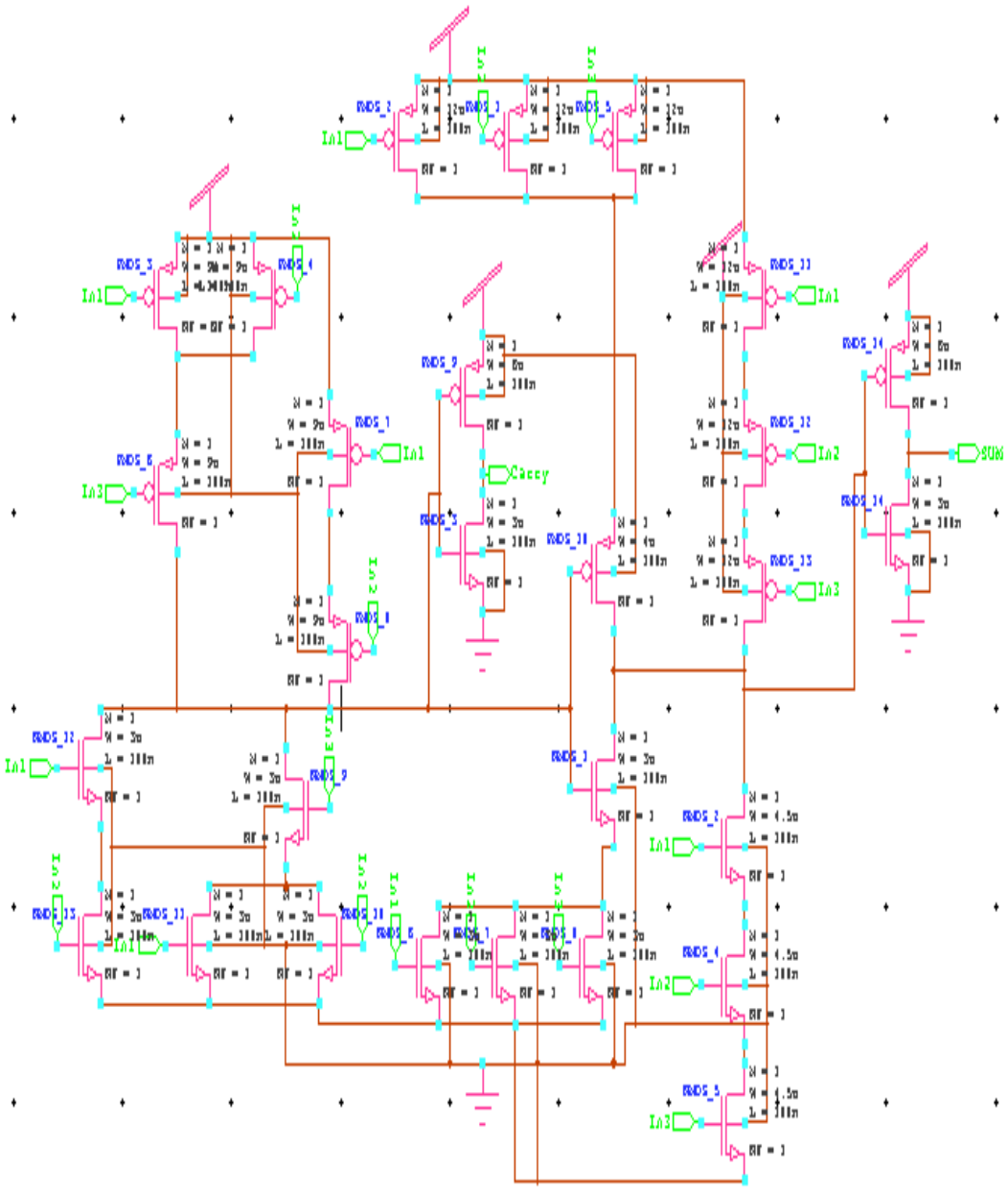

Fig 2: Schematic Diagram of Full adder

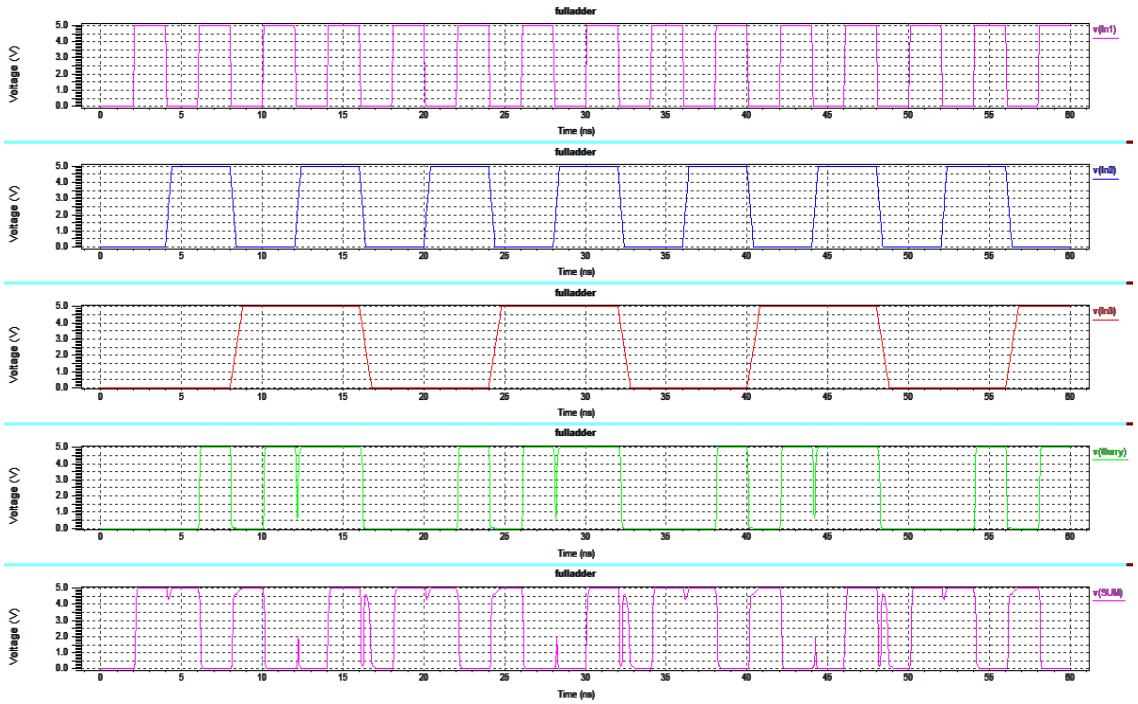

Fig 3: Waveform of the Schematic diagram of Conventional Full Adder

III FULL ADDER IMPLEMENTATION USING VARIABLE BODY BIASING WITH SLEEP INSERTION TECHNIQUE

Proposed VBBT with Sleep insertion Technique

This new sleep variable body biasing technique reduces both leakage power and glitch in the logic circuit. This design includes both-

(i) Variable body biasing and
(ii)Sleep insertion technique

Sleep insertion technique is a state destructive technique that cuts off either pull-up or pull-down or both the networks from the supply voltage or ground or both using sleep transistors. This technique is an extension to MTCMOS, which adds down networks and ground while for fast switching speeds, low-vth transistors are used in logic circuits, this process reduces leakage power during sleep mode.

The source of one of the sleep transistor is connected to the body of other sleep transistor in order to have a variable body biasing effect. Due to this connection the threshold voltage of the sleep transistors increases due to variable body biasing during sleep mode.

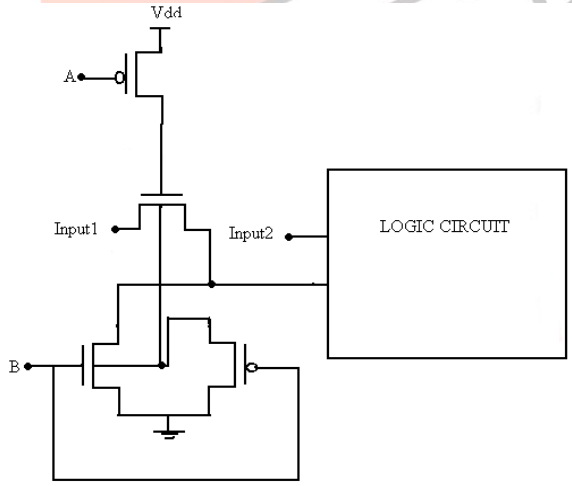

Figure 1 Variable Body Biasing with Sleep Insertion Technique

Application of VBBT along with sleep insertion technique on Full Adder to calculate the amount of leakage power reduced in VBBT technique.

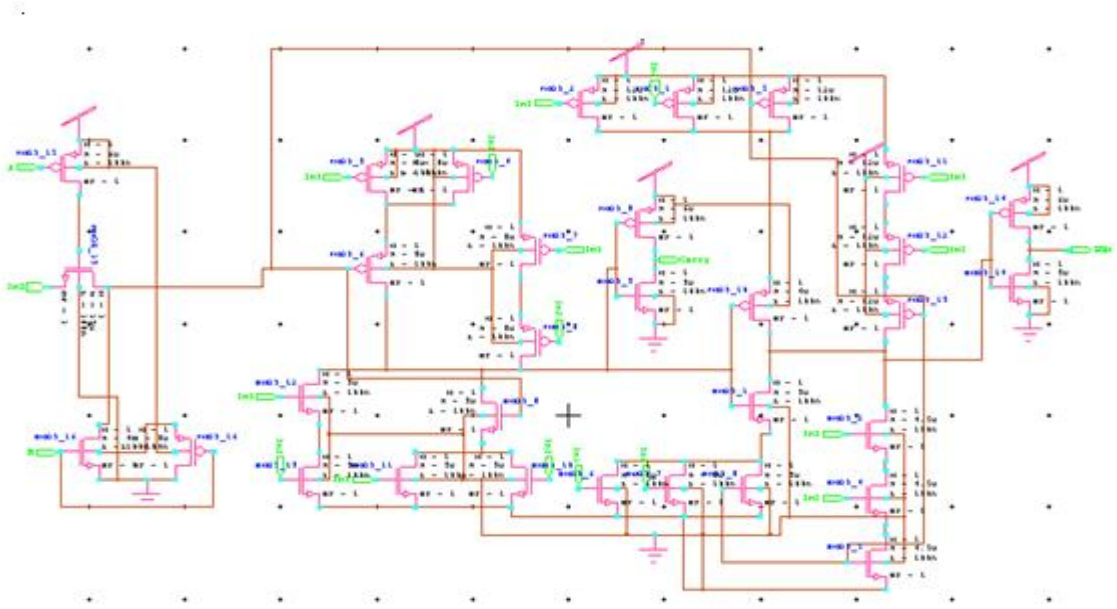

Fig 5: Schematic Diagram of Full Adder Implemented by using Variable Body Biasing with sleep insertion technique

The VBBT based Full Adder is shown in Figure5 with the two transistors used as variable body biasing and one transistor is added in order to add stack approach so that the disadvantage of state destructive stage is overcome. The simulation waveforms of VBBT AND gate from Figure4 show that the basic characteristics of AND are retained by VBBT AND gate.

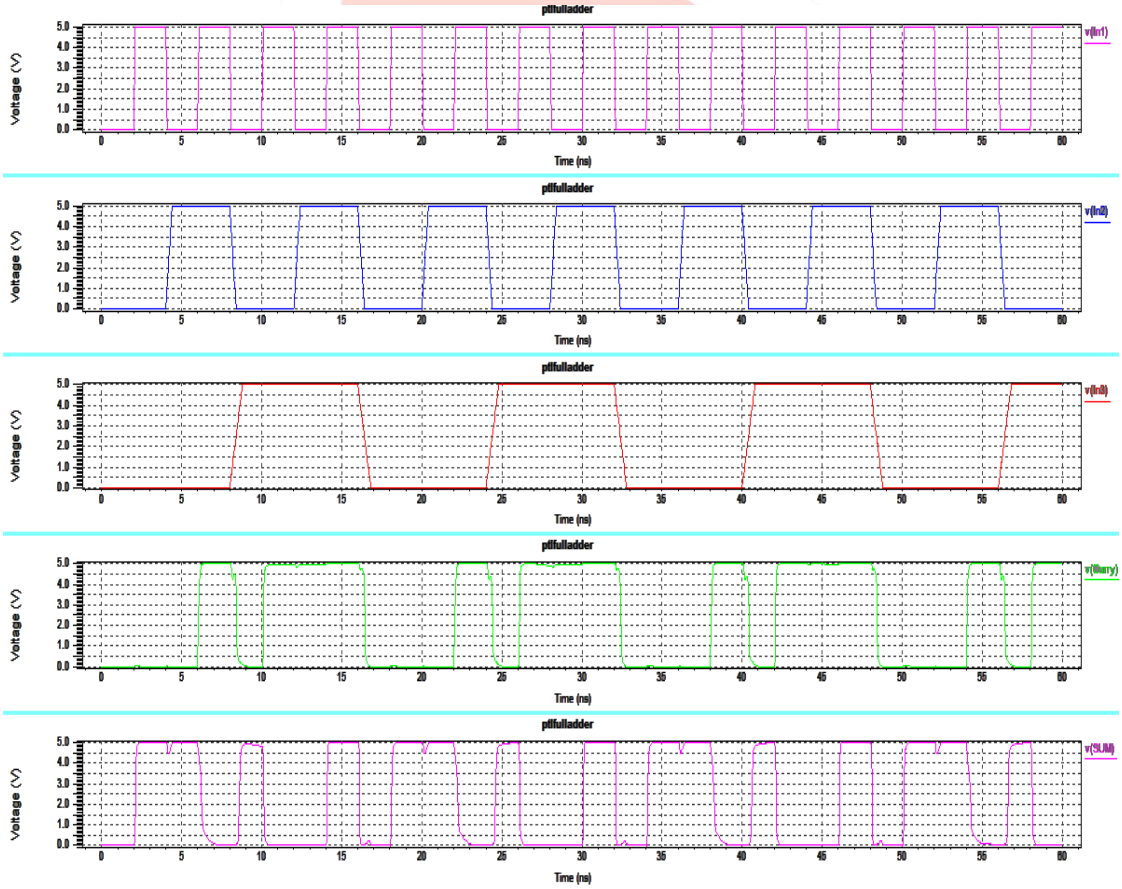

Fig 6:Waveform of Schematic diagram of Full Adder implemented along with Variable Body Biasing with Sleep Insertion Technique

IV Layout of full adder implemented using variable body biasing with sleep insertion technique

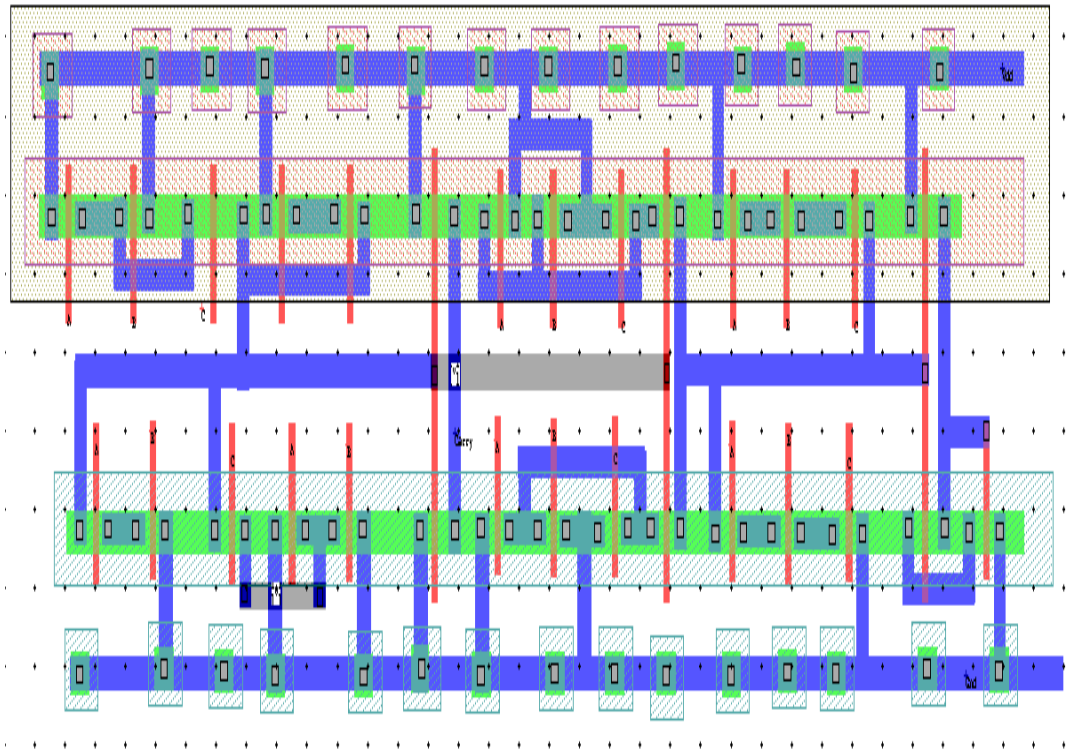

Fig 7:Layout of Full Adder Implemented by using Variable Body Biasing with Sleep Insertion Technique

V EXPERIMENTAL RESULTS

The leakage power is measured using the Tanner Tool S-EDIT simulator. The results obtained through the technique for Full Adder are shown in Table 1. Simulation for Full Adder are performed by taking process parameter, 90nm CMOS Technology.

Table-1

Gate Type	Glitch %		Power consumption(pw)		%age reduction in power consumption
	Conventional	VBBT	Conventional	VBBT	
FULL ADDER	40	0	7.29	6	20

VI.CONCLUSION

In this paper we have presented leakage power reduction VBBT technique along with sleep insertion technique. It becomes a great challenge to tackle the problem of leakage power. In this technique two individual techniques are combined one is sleep insertion technique and the other is variable body biasing technique. VBBT achieves the reduction in leakage power compared to other leakage reduction techniques, such as sleep transistor, sleepy keeper, etc. The performance has been investigated using 90nm Technology and evaluated by the comparison table 1 of the simulation result obtain from TSPICE.

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