Design of Ultra Low Voltage SRAM in Corporating Novel Capacitor Based Boosted Word Line

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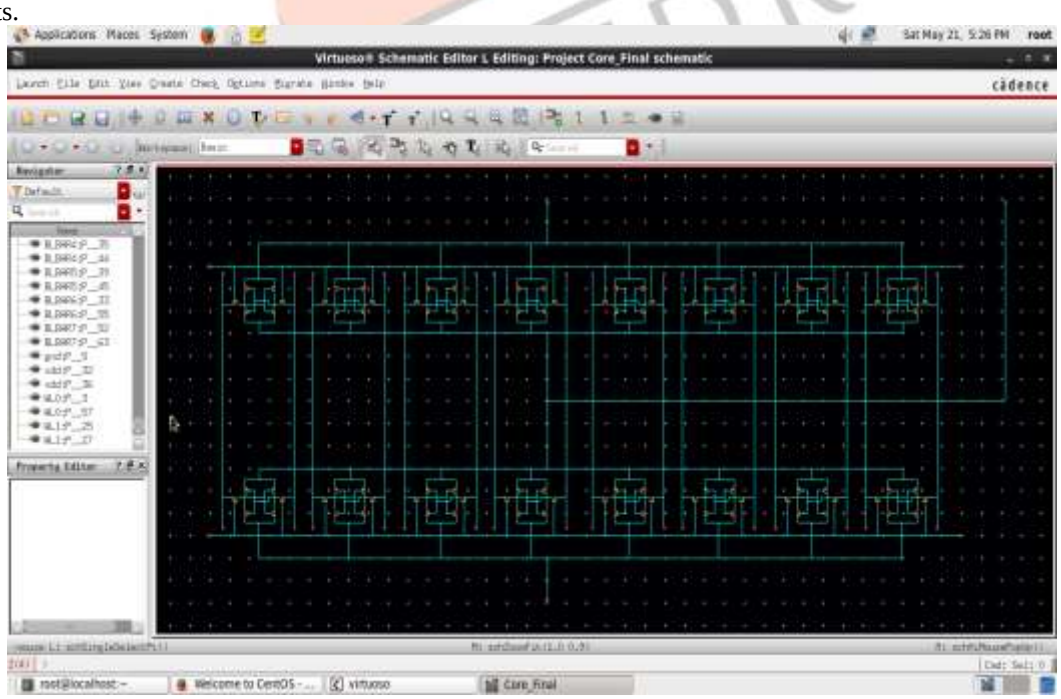
Abstract **- Design techniques to realize input/output circuits used to access six-transistor (6T) Static Random Access Memory (SRAM) cell based memory array in Ultra Low Voltage (ULV) applications. The main thrust of this work is to optimize access speed and power consumption- static & switching of SRAM based high width memories in ULV applications. A novel design for capacitor based voltage boosting technique is introduced in the input/output circuits of high density ULV SRAM. Capacitor based voltage boosting technique compensates for high capacitance of lengthy access routes, encountered in large capacity memories and inadequate gate drive owing to supply power scaling. Other low voltage techniques, such as pre-decoding, are realized in conjunction with boosting capacitor technique to overcome the SRAM cell's variations and thus achieve fast, low power SRAM operation .The capacitor based boosting technique also reduces chip area occupancy by doing away with large inverter circuits required to drive large capacitance access paths.**

Key words **- Ultra low voltage, multi stage decoding, voltage boosting, capacitor based voltage boosting ,**

I. INTRODUCTION

The electronics industry and specifically the semiconductor industry have continued to define supply voltage of decreasing magnitudes. This continuing trend thus expects present day integrated circuits to provide efficiently, high on chip voltages despite being fed by lower off chip supply voltages as certain integrated circuit applications require internally generated secondary voltage source that is often larger in magnitude than the primary externally supplied power source. For example, some non-volatile memory circuits, such as electrically erasable programmable read only memories (EEPROMs), that may use a single power supply voltage of, for example, 3.5 volts, also require a programming or erase voltage that is much larger in magnitude such as of the order of 12 volts. Apart from such specific scenarios there are also generic functional reasons such as compensation for voltage drops due to the threshold voltages of transistors, to ensure required switching speeds for the transistors which warrant the need for special circuits which can try to restore the operating voltage levels at those instances where it is desired. Therefore such special circuits used for restoration and elevation of the supply voltage signal levels are functionally known as internal boosting circuits.



II. DATA PATH

In the SRAM data path, switching of the Bitlines and I/O lines and biasing the sense amplifiers consume a significant fraction of the total power, especially in wide access width memories. Therefore Chapter 3 investigates the technique to reduce SRAM power without disturbing the performance by using tracking circuits to limit Bitline and I/O line swing and aid in the generation of the sense clock so that clocked sense amplifiers is enabled.

III. LARGE SIZED INVERTER CHAINS AS LAST MILE CONNECTIVITY

Although the techniques mentioned above and some other techniques like divided word line & memory segmentation have been developed and are being used, a common problem that has been observed is the decoder delay. The decoder delay consists of the gate delays in the critical path and the interconnect delay of the pre-decoder and word line wires. As the wire RC delay grows proportion to the square of the wire length, the wire delays within the decoder structure, especially of the word line, becomes significant in large SRAMs. The decoder sizing problem is complicated further due to the presence of intermediate interconnect from the pre-decoder wires as well as ever falling supply voltage range that is now reaching almost equal to the threshold range of single transistor. Sizing of gates in the decoder allows for trade offs in the delay and power i.e. they all realize the last stage of the decoder block through large dimensioned inverter or buffer chains. This reduces the packing density of the memory core.

IV. VOLTAGE BOOSTING USING CAPACITORS

To circumvent the usage of large sized inverter chain as the last mile connectivity, voltage boosting using capacitors was introduced . Multiple capacitors configured to generate word/row line with voltage level more than the feeble supply voltage have been suggested.

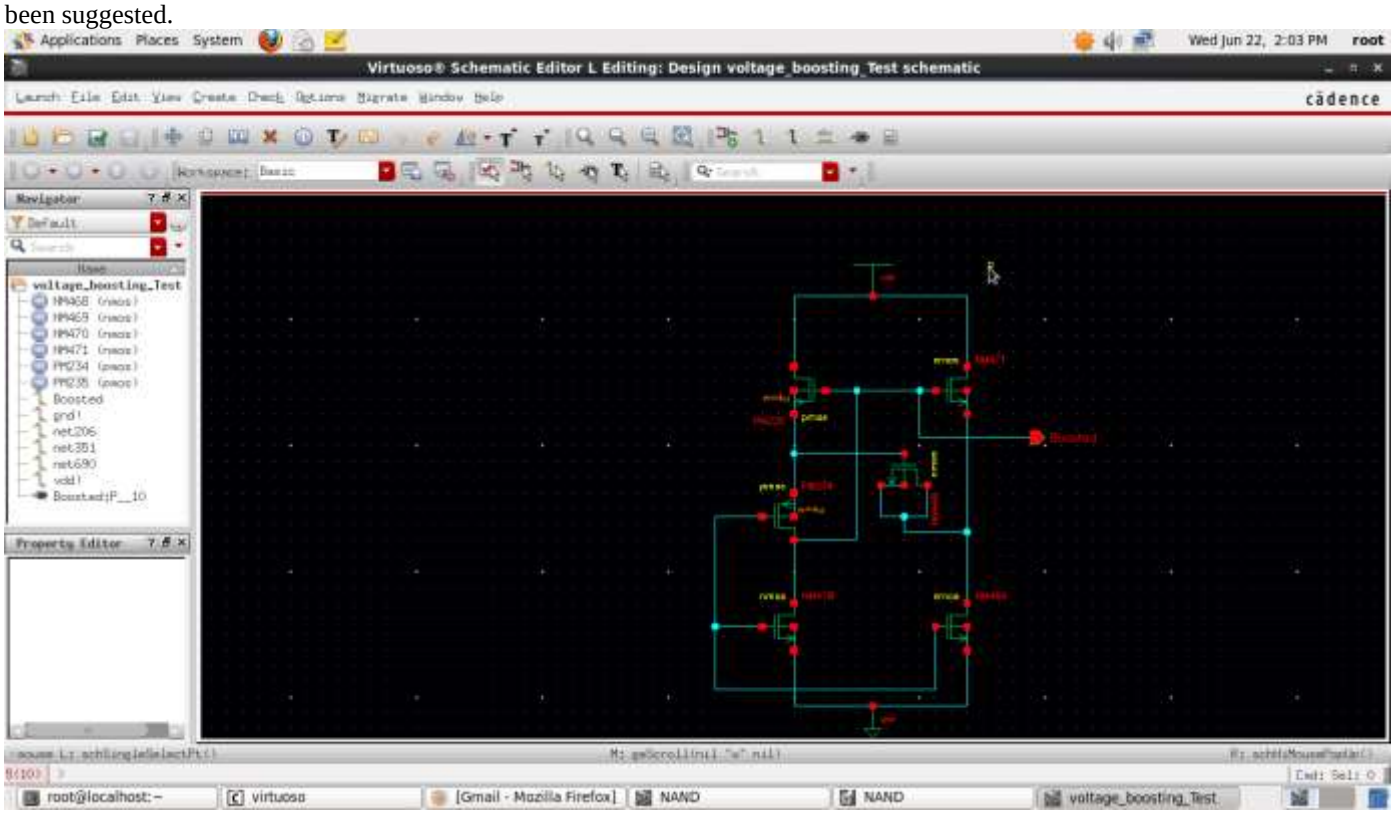


Fig : Capacitor based Voltage boosted Word/Row Line Decoder Circuit Last Mile Connectivity.

V. NOVEL WORD/ROW LINE VOLTAGE BOOSTING TECHNIQUE USING A SINGLE CAPACITOR

The proposed work we intend to carry out will use only a single capacitor and that too with self-control circuitry to achieve voltage boosting in ULV SRAM Word/Row Line decoder modules. We intend to configure and place the capacitor such that it itself will act as both the pre-charge and the boosting capacitor and also avoid inclusion of any circuitry to maintain V_{DD} during stand-by mode of operation of SRAM.

VI. CONCLUSION

We achieved at-least 25-30% boosted voltage above and over supply voltage V_{DD} and also reduce static as well as dynamic power consumption. Usage of single capacitor and self control circuitry will also save chip area and reduce complexity associated with fabrication of capacitors in silicon. Parallel boosting resembles series boosting in analysis but the latter has the advantage of having a lower stored energy, hence lower capacitor voltage rating, for the same value of capacitance. Usage of single capacitor and that too with self-control circuitry to achieve voltage boosting in ULV SRAM Word/Row Line decoder modules. We also intend to configure and place the capacitor such that it itself will act as both the pre-charge and the boosting capacitor and also avoid inclusion of any circuitry to maintain V_{DD} during stand-by mode of operation of SRAM.

VII. REFERENCES

[1] A. P. Chandrakasan, et. al., "Low-Power CMOS Digital Design", *IEEE Journal of Solid State Circuits*, vol. 27, no. 4, pg 473-484, April 1992.

[2] Janm Rabaey , Anantha Chandrakasan , Borivoje Nikolic . "Digital Integrated Circuits", Second Edition 2004.

[3] Tegze P.Haraszti "CMOS memory circuits", Kluwer Academic Publishers", 2000, pg 165-

[4] Vishwani D. Agrawal. CMOS SRAM Circuitry Design and Parametric Test in Nano-Scaled Technologies, edited by Pavlov, Andrei and Sachdev, Manoj. Location: Springer, January 01, 2008.

[5] Yuh-Kuang, Tseng *Industrial Research and Technology Institut,* Chapter 49.

[6] Meixner and J. Banik. Weak write test model: An SRAM cell stability design for test technique. In Proc. IEEE International Test Conferrence (ITC), pages 1043- 1052, November 1997.

[7] James B Kuo, Jea-Hong Lou, "Low-Voltage CMOS VLSI Circuits", pg 235-343

[8] P.J. Lawrenson, 'Switched reluctance drives: A perspective', International conference on Electrical Machines (ICEM), Manchester, UK, 1992, pp 12-21